M243XL

Magnetic Tape Subsystem Formatter Theory of Operation

FUJITSU

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2-4	01A	4-29	01	4-72	01A	4-115	01	5-4	01		
2-5	01	4-30	01A	4-73	01A	4-116	01A	5-5	01A		
2-6	01A	4-31	01A	4-74	01A	4-117	01	5-6	01A		
2-7	01	4-32	01A	4-75	01A	4-118	01A	5-7	01A		
2-8	01	4-33	01A	4-76	01A	4-119	01A	5-8	01A		
3-1	01	4-34	01A	4-77	01A	4-120	01A	5-9	01A		
3-2	01A	4-35	01A	4-78	01A	4-121	01A	5-10	01A		
3-3	01A	4-36	01	4-79	01A	4-122	01	5-11	01A		
3-4	01A	4-37	01	4-80	01A	4-123	01A	5-12	01A		
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3-7	01A	4-40	01	4-83	01A	4-126	01A	5-15	01A		
3-8	01A	4-41	01	4-84	01A	4-127	01	5-16	01A		
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3-11	02A	4-44	01A	4-87	01A	4-130	01	5-19	01A		
BLANK		4-45	01A	4-88	01A	4-131	01A	5-20	01A		
4-1	01A	4-46	01A	4-89	01A	4-132	01A	5-21	01		
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4-3	02A	4-48	01A	4-91	01A	4-134	01A	5-23	01		
4-4	01A	4-49	01A	4-92	01A	4-135	01A	5-24	01A		
4-5	01A	4-50	01A	4-93	01A	4-136	01	5-25	01A		
4-6	01A	4-51	01A	4-94	02A	4-137	02A	5-26	01A		
4-7	01A	4-52	01A	4-95	02A	4-138	01A	5-27	01A		
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CHAPTER 1 INTRODUCTION

1.1 Functions

The M243XL magnetic tape subsystems are used as an external storage of the data processing unit. This manual describes only the magnetic tape formatter in the magnetic tape subsystem. Refer to the other manual for the magnetic tape unit. The magnetic tape control unit and tape unit are referred to after this as "FMT" and "MTU".

An FMT logically located between the Controller and the MTUs, receives and decodes control signals, commands, MTU addresses, etc. from the Controller. It also controls read and write operation, rewind, erase and other operations for a specified MTU.

An FMT can control up to eight MTUs.

1.2 Unit Types

Table 1.1 Types of units

Unit name	Configuration
M2434L1	FMTx1 + MTU (6250/1600 RPI, 75/125 IPS)x1
M2434L2	FMTx2 + MTU (6250/1600 RPI, 75/125 IPS)x1 for device cross-call feature
M2430L	MTU (6250/1600 RPI, 75/125 IPS)x1
M2431L	MTU (1600/800 RPI, 75/125 IPS)x1
M2435L1	FMTx1 + MTU (6250/1600 RPI, 125/200 IPS)x1
M2435L2	FMTx2 + MTU (6250/1600 RPI, 125/200 IPS)x1
M2432L	MTU (6250/1600 RPI, 125/200 IPS)x1
M2433L	MTU (1600/800 RPI, 125/200 IPS)x1
M2436L1	FMTx1 + MTU (6250/1600 RPI, 200 IPS)x1
M2436L2	FMTx2 + MTU (6250/1600 RPI, 200 IPS)x1
M2436L8	MTU (6250/1600 RPI, 200 IPS)x1

* Each FMT/MTU contains its own power supply unit.

1.3 Characteristics

Table 1.2 Shows the characteristics of each unit type

Item \ Unit type		M2436 L1/L2	M2436L8	M2435 L1/L2	M2432L	M2433L	M2434L	M2430L	M2431L
Number of built-in FMTs (CH)		1/2	None	1/2	None		1/2	None	
Recording density (RPI)		6250/1600				1600/800	6250/1600		1600/800
Tape speed	Normal	200		125			75		
	High	None		200*			125*		
Data transfer rate (KB/S)	Normal	1250/320		781/200		200/100	469/120		120/60
	High	-		1250/320		320/-	781/200		200/-
IBG Length (inch.)		6250 RPI; 0.4 1600 RPI; 0.6		6250 RPI; 0.3 1600/800 RPI; 0.6					
Tape load time (sec.)		12							
Tape rewind time (sec.)		55							
Unload time (sec.)		65							
Tape length (feet)		2400 (full reel)							
Loading feature		Auto-loading							
Reel locking feature		Auto-hub							
Window mechanism		Auto-window							
Cartridge		Usable							
Error marker		Preset							
Maximum configuration		Up to 8 tape units							
Unit address		Fixed							
MTU cross-call		Available for a 2 FMT system							

* THE 800 RPI model does not have a high speed function.

1.4 Configuration

Figures 1.1 and 1.2 show the subsystem configuration with a single FMT and dual FMTs, respectively.

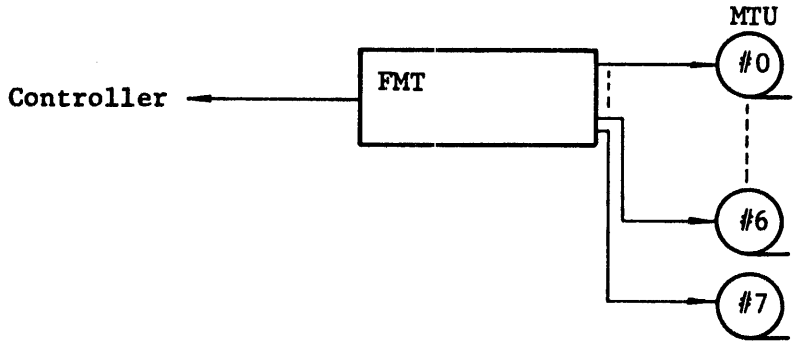


Figure 1.1 Single formatter system

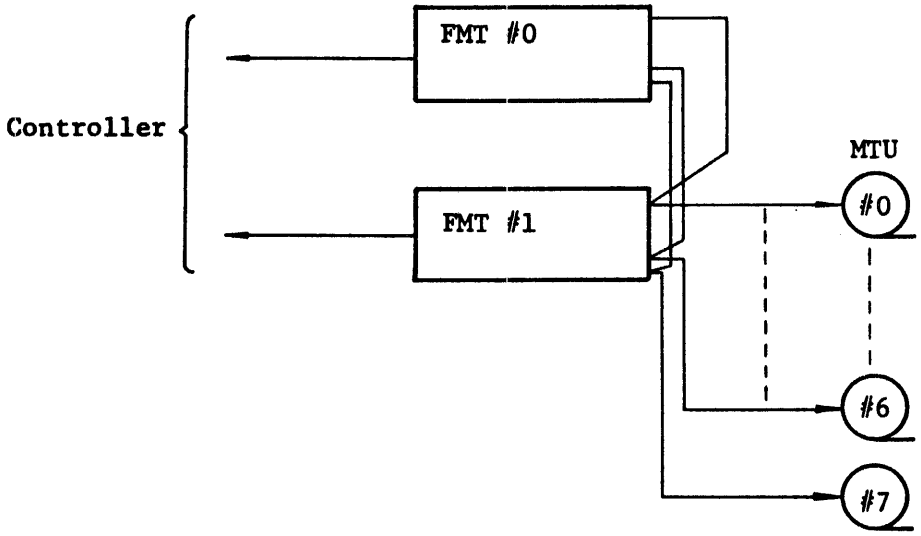


Figure 1.2 Dual formatter system

CHAPTER 2 COMMAND OPERATION

2.1 Outline

This chapter explains the logical specifications of command operations, status, and Drive Sense Bytes in the FMT.

2.2 Commands

Table 2.1 outlines the types, codes and operations of commands.

(1) Command initiation

All commands are initiated by the START signial set by the controller while the formatter is not in a busy or offline status. When the formatter acknowledges START signal assertion, the formatter accepts the instruction data on TU Address lines AD 0-2, Density select lines DS 0 and 1, and Command Select lines CMDE, CMD 0-3. It then responds with a BUSY signal. While the formatter is in a busy or offline status, the START signal assertion has no effect on the formatter.

(2) Command execution

When any command is issued to the formatter, the formatter checks the validity of the command code. If the command code is invalid, the command operation is immediately terminated with REJECT signal. When any command except NOP, CLR, DMS, SNS and LWR is issued, the formatter checks the status of the specified MTU. If the MTU is in a not-ready status or the MTU status is such that it cannot perform the command, the command operation is immediately terminated with a REJECT signal. When a NOP, CLR, DMS, SNS or LWR command is issued, the command operation will be executed regardless of the MTU status. These commands have no effect on the error status and the Drive Sense Bytes. Other commands will be executed after the error status and the Drive Sense Bytes are reset.

(3) Command termination

Termination of commands other than REW, DSE, FSF and BSF is reported when the BUSY signal is reset by the formatter. In the case that the MTU does not have the skip file function, the FSF and BSF commands are executed in the same manner as the other commands.

The result of the command operation is indicated by formatter status signals and is classified as follows:

- The command operation completed normally
  No error status
- The command was invalid or was issued to the MTU in a status that could not execute the command operation.
  'REJECT'
- The command operation was interrupted by an abnormality.
  'REJECT', 'OP-INC'
- BOT (Beginning of Tape) was detected during a backward operation.
  'DATA CHK', 'ID-BRST'
- Incorrect data were detected during a read or write operation.
  'DATA CHK'
- A parity error of the transferred data was detected during a WRT or LWR operation.
  'BUSER'
- An overrun error was detected during the data transfer operation.
  'DATA CHK', 'OVRNS'

On a REW, DSE, FSF or BSF command, the formatter resets BUSY signal and becomes free when the MTU starts the command operation.
The command termination is reported by SSC signal assertion when the operation is completed by MTU itself.
In the case of a FSF or BSF command, the result of the command operation is reported by a CLR command issued after SSC signal assertion.

Table 2.1 Command operation (1/3)

Name	Mnemonic	Command Code(Hex.)	Command Type	Operation
Write	WRT	06	Burst	To write data on the tape in the density mode of the MTU. When a WRT command is issued at BOT. The write operation is executed in the density mode specified by Density Select lines.
Read Read Backward	RD RDB	04 05	Burst	To read data forward (RD) or backward (RDB) and to transfer data read from the tape. If a tape mark block is read, no data is transferred.
Loop-Write-to-Read	LWR	07	Burst	To write and check data in order to diagnose the data path of the FMT with no tape motion.
Set Diagnose	SDIA	17	Burst	To transfer the diagnostic flag byte (4 bytes) in order to execute the diagnostic operation or modify the subsequent command.
No Operation	NOP	00	No motion control	To execute no operation and terminate regardless of the MTU status.
Drive Clear	CLR	01	No motion control	To clear the error status of the MTU and the FMT regardless of the MTU status. This is also used to post the result of FSF or BSF command operation.
Diagnostic Mode Set	DMS	02	No motion control	To set the FMT to the special status and terminate regardless of the MTU status.

Table 2.1 Command operation (2/3)

Name	Mnemonic	Command Code(Hex.)	Command Type	Operation
Sense Drive Status	SNS	03	No motion control	To indicate detail information of the FMT error or status information of the MTU as DSBs (Drive Sense Bytes) via Error Multiplex Bus. This command is normally excuted regardless of the MTU status.
Back Space File Space File	BSF FSF	08 0A	Motion control	To feed a tape backward (BSF) or Forward (FSF) until the first tape mark is detected. When the MTU has a skip file function, this command is performed by the MTU same as a rewind operation. In this case, the termination of this command is posted by the SSC signal assertion. When the MTU does not have a skip file function, this command is performed by the FMT.
Back Space Space	BSP FSP	09 0B	Motion control	To feed a tape backward (BSP) or forward (FSP) until STOP signal is issued or the first tape mark block is detected.
Write Tape Mark	WTM	0C	Motion control	To write a tape mark block after running a tape forward and erasing the specified length.
Erase	ERS	0D	Motion control	To erase the specified length of a tape in forward direction.

Table 2.1 Command operation (3/3)

Name	Mnemonic	Command Code(Hex.)	Command Type	Operation
Rewind	REW	0E	Motion control	To rewind a tape till BOT position. The MTU executes the rewind operation after the rewind command is instructed by the FMT. The termination of this command is posted by the SSC signal assertion.
Unload	UNL	0F	Motion control	To unload a tape until all the tape is wound onto the supply reel. After the unload command is instructed by the FMT and the MTU turns to offline status, the MTU executes the unload operation.
Set High Speed Mode Set Normal Speed Mode	SHSP SNSP	19 1B	Motion control	To change the tape speed mode of the MTU and correct the STOP position to meet the tape speed mode.
Data Security Erase	DSE	1D	Motion control	To erase a tape until the EOT (End of Tape) marker is detected. The MTU executes the DSE operation as same as the rewind operation. The termination of the command is posted by the SSC signal assertion.

2.3 Drive Status Bytes

The Drive Status Bytes (DSBs) consist of 16 bytes of DSB 0-15 and indicates the detail error and status informations of the FMT and MTU. After the command operation terminates, DSBO is indicated as MUX Byte 3. The number of the DSB is increased by the SNS command execution. The contents of the DSBs are shown in Table 2.1.

TUC (Tape Unit Check; DSB3, placed in an off line bit 7) causes REJECT and OP-INC, and in this case the MTU status. The detail information of TUC are indicated in DSB5 AND DSB6. ANY BIT OF DSB11 OR BIT 3-0 of DSB12 causes MISC DATA ERR (MUX Byte 1, bit 3). DSB14 and DSB15 and Field Replaceable Units and indicate the detail information of the error.

Table 2.1 Drive sense bytes (1/2)

Bit / Byte	P	7	6	5	4	3	2	1	0
DSB0	WRTS	EOTS	BOTS	NSPM	FPS	BWDS	HDNS	RDYS	ONLS
1	"0"	"1"	"1"	D1	D0	"0"	M2	M1	M0
2	"0"	"0"	"0"	S1	S0	"0"	"0"	"0"	"0"
3	"0"	TUC	Reset key	DSE	Test Mode	"F or E"	SAGC Count "D or C"	"B or A"	"9 or 8"
4	"0"	UERS	UACT	UBWD	UWCON	U64S	TOVR	UPE	TM
5	"0"	MISC Error	TLA Left	TLA Right	ROM Parity Error	Write Circuit Alarm	"0"	Air Bearing Alarm	Load Failure
6	"0"	2^7	2^6	2^5	MTU Error Code 2^4	2^3	2^2	2^1	2^0
7	LWR TUIF	Streaming Function	Skip File Function	High Speed Mode	Low Slice Mode	LVC0	Slice Level LVC1	LVC2	LWR RW
8	"0"	2^{15}	2^{14}	2^{13}	TU Unique ID High order 2^{12}	2^{11}	2^{10}	2^9	2^8
9	"0"	2^7	2^6	2^5	TU Unique ID Low order 2^4	2^3	2^2	2^1	2^0

Table 2.1 Drive sense bytes (2/2)

Bit / Byte	P	7	6	5	4	3	2	1	0
DSB10	"0"	FMT Function ID							
11	"0"	IBG Detect	Start Read check	CRC III check	Early Begin Read Back	SAGC check/ Noise Error	Slow Begin Read Back Check	Slow End Read Back Check	PCMP
12	"0"	X-Call	800BPI Feature	LWR FMT	Velocity Retry	Skew Error	WEC Overflow	Envelope Check	Write Trigger VRC
13	"0"	2^7	2^6	2^5	Write Error Count 2^4	2^3	2^2	2^1	2^0
14	"0"	FRU 1							
15	"0"	FRU 2							

CHAPTER 3 INTERFACE

3.1 Controller/Formatter Interface

This section outlines the interface for Host Controller.

3.1.1 Signal lines

Table 3.1 lists the Controller/Formatter interface signal lines.

Table 3.1 Interface signal lines (1/4)

Interface Signal		No. of lines	Direction User FMT	Meaning
Name	Mnemonic			
TU Address 0-2	AD0-2	3	⟹	To select one of the eight MTUs which should execute the command or should indicate its status.
Command Select 0-3 Command Extend	CMD0-3 CMDE	5	⟹	To cause the FMT to execute the command operation.
Density Select 0,1	DS0,1	2	⟹	To select the recording density of the MTU. These lines are valid when the MTU is positioned at BOT during WRT, WTM or ERS command operation or a LWR FMT command is initiated.
Bi-directional Data Bus	DB0-7,P	9	⟺	To be used to transfer the data for read or write operation or diagnostic flag bytes. Odd parity is maintained for all data transfer operation. The transfer direction is controlled by the Expecting Data (RECV) signal.
Initiate Command	START	1	⟶	To start the FMT to initiate the command. The FMT responds to START by asserting BUSY.
Formatter Busy	BUSY	1	⟵	To indicate that the FMT is executing the command operation or the Power-on diagnostic operation.

Table 3.1 Interface signal lines (2/4)

Interface Signal		No. of lines	Direction User FMT	Meaning
Name	Mnemonic			
Expecting Data	RECV	1	←	To decide the data transfer direction of the bi-directional data bus. The data transfer direction is from the controller to the FMT during RECV assertion.
Terminate Command	STOP	1	→	To terminate the data transfer operation through the bi-directional data bus in response to TREQ signal. To terminate spacing over blocks in response to BLOCK signal.
Transfer Request	TREQ	1	←	To request data transfer via the bi-directional data bus.
Transfer Acknow-ledge	TRAK	1	→	In respond to TREQ, to tranfer data via the bi-directional data bus.
End of Data Pulse	ENDATP	1	←	To indicate the termination of the data transfer operation during a RD or RDB command operation.
System Reset	RESET	1	→	To reset the FMT to initial status.
Select Multiplex 0-2	SLX0-2	3	⟹	To select one of eight MUX Bytes on the Error Multiplex output lines.
Error Multiplex	ERRMXP-0	9	⟸	To indicate additional errors and reject status information as a part of the end status of the most recently completed command.
Slave Status Change	SSC	1	←	To indicate that one or more MTUs have either gone online, gone offline or gone from Not Ready to ready.

Table 3.1 Interface signal lines (3/4)

Interface Signal		No. of lines	Direction User FMT	Meaning
Name	Mnemonic			
Oscillator	OSC	1	←———	The internal control clock for the data path control circuits.
Ready Status	RDYS	1	←———	To indicate the addressed MTU is in a ready status.
Online Status	ONLS	1	←———	To indicate the addressed MTU is in an online status.
Rewinding Status	REWS	1	←———	To indicate the addressed MTU is rewinding.
Write Status	WRTS	1	←———	To indicate the addressed MTU is in a write status.
Beginning of Tape Status	BOTS	1	←———	To indicate the addressed MTU is positioned at BOT.
End of Tape Status	EOTS	1	←———	To indicate the addressed MTU is positioned on or past the EOT marker.
File Protect Status	FPS	1	←———	To indicate that a write enable ring is not on the file reel or the file protect switch of the MTU operator panel is pushed.
High Density Status	HDENS	1	←———	To indicate the density mode of the MTU in combination between HDENS and NRZI.
NRZI Status	NRZI	1	←———	
Identification Burst	ID-BRST	1	←———	To indicate that the FMT is performing ID burst and ARA burst procedure from BOT.
Block Sensed	BLOCK	1	←———	To indicate that a data block or a tape mark block is detected during a FSP or BSP command operation, or a tape mark block is detected during a RD, RDB, FSF or BSF command operation.

Table 3.1 Interface signal lines (4/4)

Interface Signal		No. of lines	Direction User FMT	Meaning
Name	Mnemonic			
Tape Mark Status	TMS	1	←	To indicate that a tape mark block is detected or a WTM command is correctly executed.
Operation Incomplete	OP-INC	1	←	To indicate that the command operation is initiated but incomplete because an error condition to interrupt the command operation is detected.
Command Reject	REJECT	1	←	To indicate that the command operation cannot be initiated or is initiated but interrupted by an error. The detail of the error condition is indicated in MUX Byte 2 with reject code.
Overrun Status	OVRNS	1	←	To indicate that the command operation has not been normally completed because TRACK response to TREQ was too late.
Data Check	DATA CHK	1	←	To indicate that data just written or read out is not or may not be correct.
ROM Parity Error	ROMPS	1	←	To indicate that a parity error in FMT ROM or a parity error in a register was detected.
Corrected Error	CRERR	1	←	To indicate that one or two track error corrections were performed during GCR or PE operation, or a reread to attempt a correction of the error block has been performed.
Data Bus Parity Error	BUSER	1	←	To indicate that a parity error in the received data was detected during a WRT, LWR or SDIA command operation.

3.1.2 Interface sequence

The interface sequence of the command initiation is shown in Figure 3.1. The interface sequence of the command termination is shown in Figure 3.2. The interface sequence of the data transfer operation is shown in Figure 3.3.

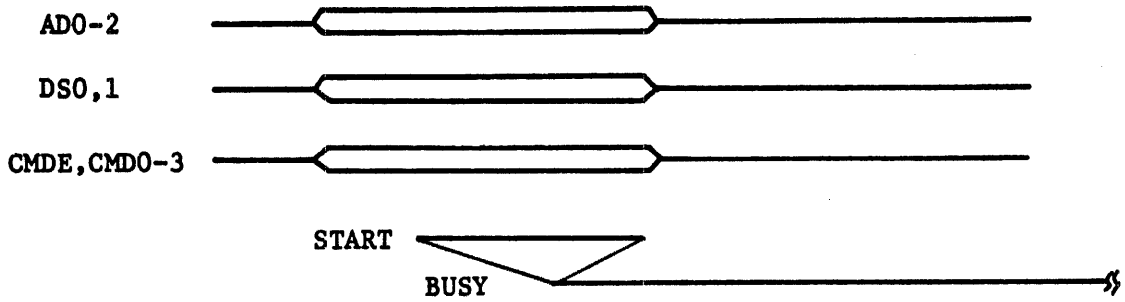


Figure 3.1 The interface sequence of the command initiation

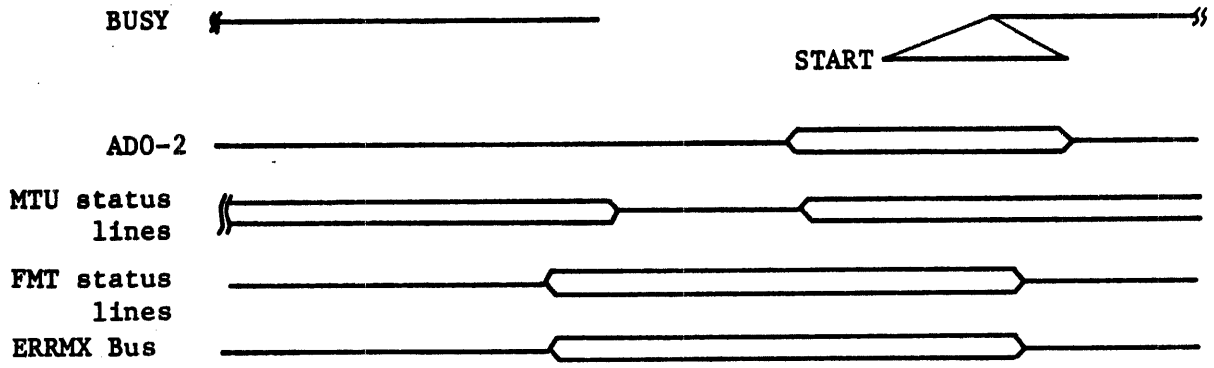
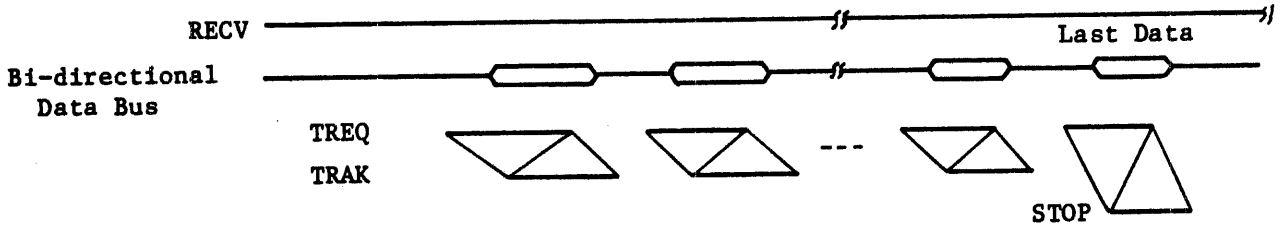


Figure 3.2 The interface sequence of the command termination

(1) WRT, LWR or SDIA command



(2) RD or RDB command

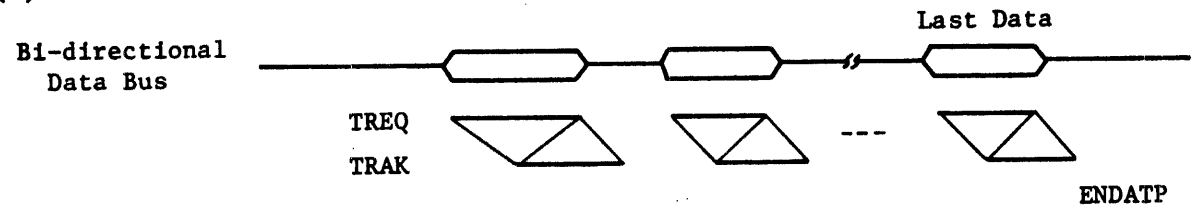
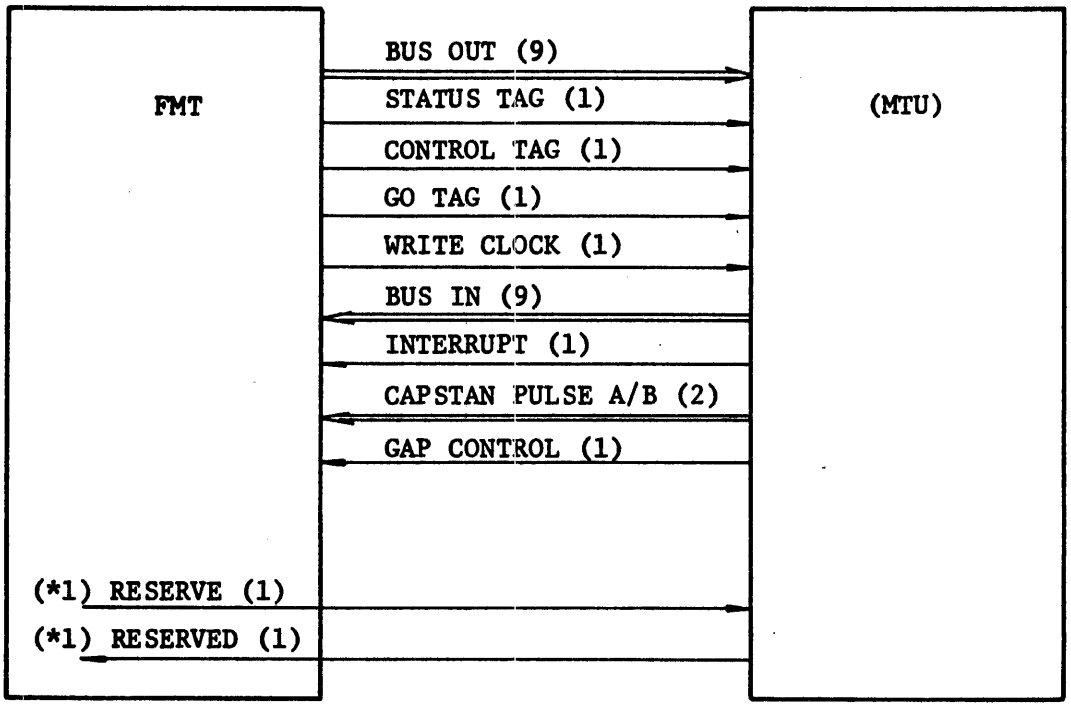


Figure 3.3 The interface sequence of the data transfer operation

3.2 FMT-MTU Interface

This section summarizes the definitions of logical signal lines between the FMT and MTU.

3.2.1 Interface signal lines



*1 The Reserve and Reserved signals are not used. However, the MTU must be terminated by a terminal resistor.

Figure 3.4 Interface signal lines

Table 3.2 MTU interface signal lines

Signal name	Meaning
Status Tag	Indicates that the Bus out data is the status information to be set, and directs the MTU to set the status information on Bus-in lines.
Control Tag	Indicate that Bus out data is the control information and direct MTU to set control information on Bus-in lines. If both the Control Tag and the Status Tag are '1', then it operates as the Command Tag.
Go Tag	Causes the MTU to drive the tape for reading or writing data.
Bus Out	Indicates the information controlled by the three tag signal lines. If the three Tag signal lines are set to all '0', a request to send the MTU sense bytes corresponding to the Bus Out bits is issued.
Bus In	If any one of the Status Tag, Control Tag, and Go Tag is '1' or both the Status Tag and Control Tag are '1', the respective information is set on the Bus In lines. If these three Tag signal lines are all '0', then each sense byte for each Bus Out bit is set on the Bus In lines.
Write Clock	Strobes the contents of the Bus Out, with the Write Clock as well as the Status Tag/Control Tag/Command Tag set to '1'.
Interrupt	Issues an interrupt to the FMT while the MTU is online
Capstan Pulse A/B	Conveys the tape driving information detected from the capstan to the FMT.
Gap Control	Conveys the block access enable signal from the MTU to the FMT.

Table 3.3 Bus Out/Bus In definitions

TAG / BIT	BUS OUT STATUS	BUS OUT CONTROL	BUS OUT COMMAND	BUS OUT GO	BUT IN STATUS	BUT IN CONTROL	BUT IN COMMAND	BUT IN GO
0	Set Erase	Level Test 0	BUS OUT 01234567 / COMMAND	WDT0/RDL0	ERS	Level Test 0	BUS IN CONTENT (BO / BUS IN) (OX)16	RD0
1	Set Read Forward	Level Test 1	0 2 Set Streaming Mode 0 3 Reset Streaming Mode	WDT1/RDL1	FWD	Level Test 1	0 STRMF (Streaming Feature) 1 SKIP (Skip File) Feature)	RD1
2	Set Read Backward	Level Test 2	0 4 Space File 0 5 Backspace File 0 6 Spare	WDT1/RDL1	FWD	Level Test 2	2 SPACE 3 LWSL (Low Slice)	RD2
3	Set Write Status	Set Test Mode	0 7 Spare 0 8 Set LWR RW 0 9 Reset LWR RW	WDT3/RDL3	Write Status	Test Mode	4 STRMD (Streaming Mode) 5 LWR RW	RD3
4	Reset	Set EMK	0 A Set Low Slice 0 B Reset Low Slice 0 C Tape Retension Action	WDT4/RDL4	TU Check	EMK	6 HACT 7 RDY (Ready)	RD4
5	Set 6250 & SAGC or Set NRZI	Set DSE	0 D Set GCR	WDT5/RDL5	SAGCON	DSE	BO / BUS IN: 8X AX CK EX / 9X BX DX FX	RD5
6	Set 1600	Set REW	COMMUNICATION REG 8 0-F Reg 0 high order 4 bits	WDT6/RDL6	1600	REW	0-7: Reg. 0 Reg. 1 Reg. 2 Reg. 3	RD6
7	Set LWR TUIF	Set UNL	9 " " low order 4 bits A " Reg 1 high order 4 bits	WDT7/RDL7	LWR TUIF	UNL		RD7
8	Parity	Parity	B " " low order 4 bits C " Reg 2 high order 4 bits D " " low order 4 bits E " Reg 3 high order 4 bits F " " low order 4 bits 8 Parity	WDT8/RDL8	TAG IN	TAG IN	TAG IN	RD8

Table 3.4 Communication registers

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Reg. 0	← WRITE ERROR COUNT MEMO →							
Reg. 1			Retry CNT0	Retry CNT1			LONG IBG0	LONG IBG1
Reg. 2	Valid Position CNT	← POSITION COUNTER UPPER →						
Reg. 3	← POSITION COUNTER LOWER →							

Table 3.5 TU sense bytes

SENSE BYTE	0	1	2	3	4	5	6	7	8
BUS OUT BIT / BUS IN	7(01) (8, all 0)	6(02)	5(04)	4(08)	3(10)	2(20)	1(40)	0(80)	3&5(14) (STS & GO TAG)
0	BWD	EXIF	MISC Error	VEL 0	Tape Unit Unique ID Low Order 2^7	SAGC COUNT 0	Read Data 0	Error Code 1 (Load RWD)	Unit Erase Current on
1	NOT FP	Reset Key	Tape Loop Alarm Left	VEL 1	" 2^6	SAGC COUNT 1	Read Data 1	Error Code 1 (LR turning)	Unit Action
2	TWA	DSE	Tape Loop Alarm Right	Ready Hold	" 2^5	SAGC COUNT 2	Read Data 2	Error Code 2 (RR turning)	Unit Backward Status
3	BOT	7 Track	ROM Parity Error	(Not use) 2^{12}	" 2^4	SAGC COUNT 3	Read Data 3	Error Code 2 (Tape present)	Unit Write current ON
4	Write Status	Test Mode	Write Circuit Alarm	(MD1 Conver-sion) 2^{11}	" 2^3	EC Level 2^3 ("1")	Read Data 4	Error Code 4 (Reel Loaded)	Unit 65% Slice
5	Online	Dual Density	(Fuse - Window Cartridge	Tape Unit Unique ID High Order 2^{10}	" 2^2	EC Level 2^2 (TUID2)	Read Data 5	Error Code 5 (Column Loaded)	Unit Over Run
6	TU Check	High Density	Air bearing Alarm	" 2^9	" 2^1	EC Level 2^1	Read Data 6	Error Code 6 (Search BOT)	Unit PE Mode
7	Ready	6250	Load Failure	" 2^8	" 2^0	EC Level 2^0	Read Data 7	Error Code 7 (Load CHK)	Tape Mark
8	TAG IN	TAG IN	TAG IN	TAG IN	TAG IN	TAG IN	Read Data 8	Error Code 8	TAG IN

CHAPTER 4 FUNCTIONAL DESCRIPTION

4.1 Outline

Figure 4.1 is a block diagram of the FMT section. In this diagram, each block corresponds to a PCA. The controller interface control PCA, write control PCA, read control PCA, 800 RPI control PCA, demodulation PCA, microprocessor PCA, and device interface PCA are installed on the FMT shelf.

This chapter describes how the above control sections operate. Figure 4.2 shows the PCA locations.

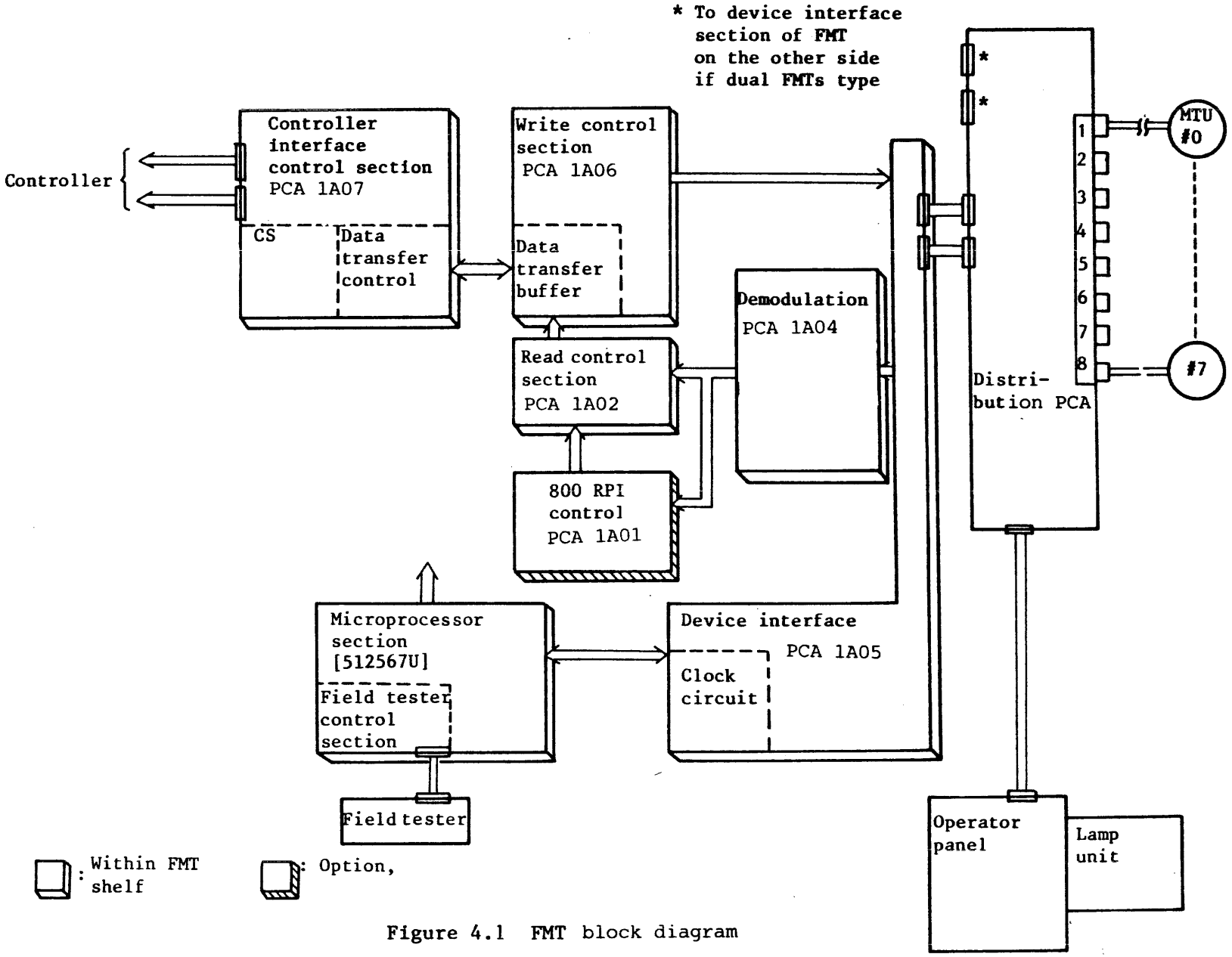


Figure 4.1 FMT block diagram

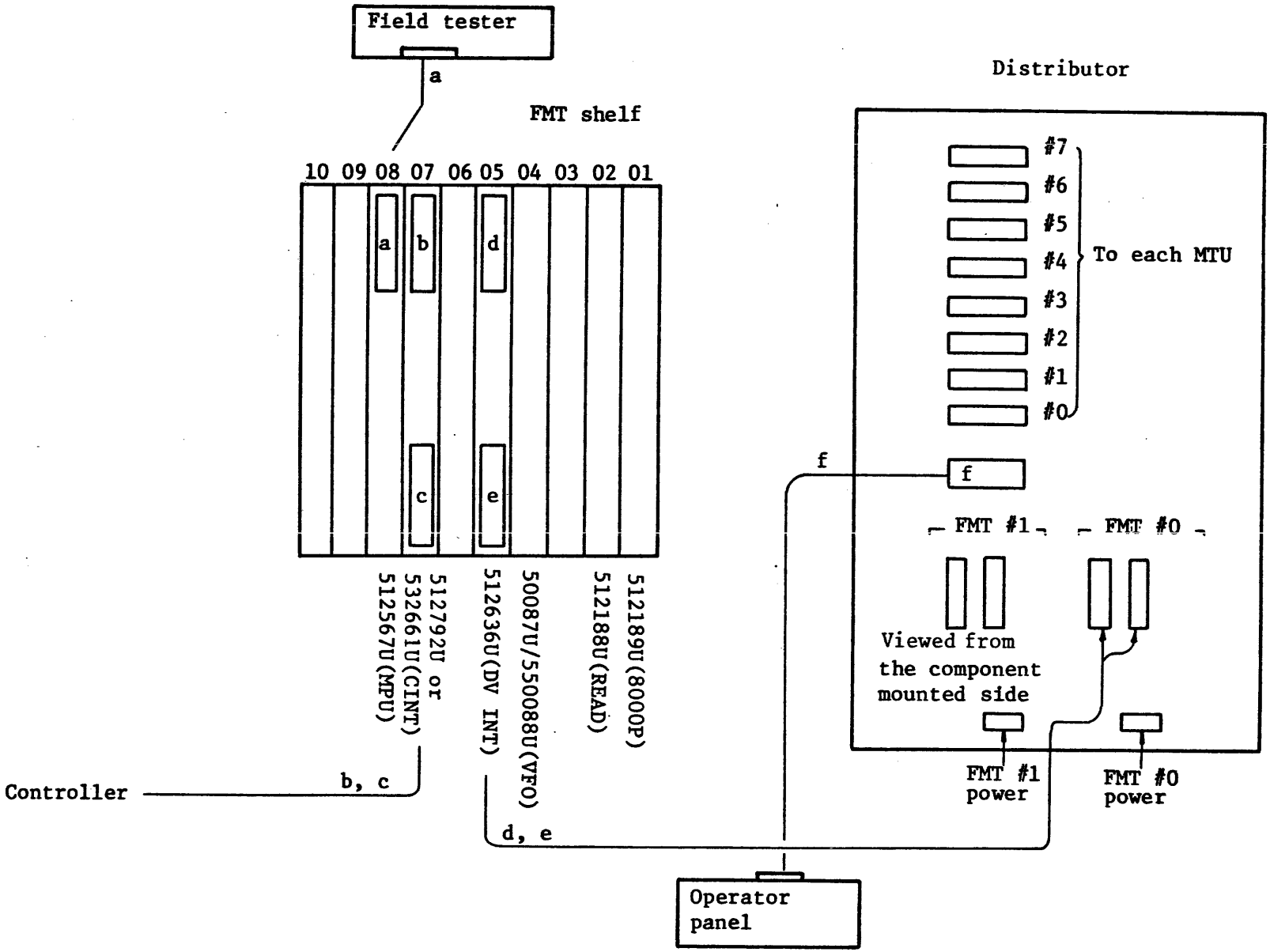


Figure 4.2 PCAs mounting positions

4.2 Reset System

The reset function is activated when:

(a) Power is applied.

(b) The ONL/OFL switch on the Field Tester is switched or a CE-reset operation is performed.

(c) A System Reset is directed from a controller.

(d) A microprocessor error (PERR) has occurred.

Figure 4.3 is a functional block diagram of the reset function. The reset function generates three levels of signals as Reset Signals; System Reset (SYRT), Selective Reset (SERT), and Hardware Clear (HCLR). Table 4.1 lists the conditions under which these three levels of Reset signals are generated.

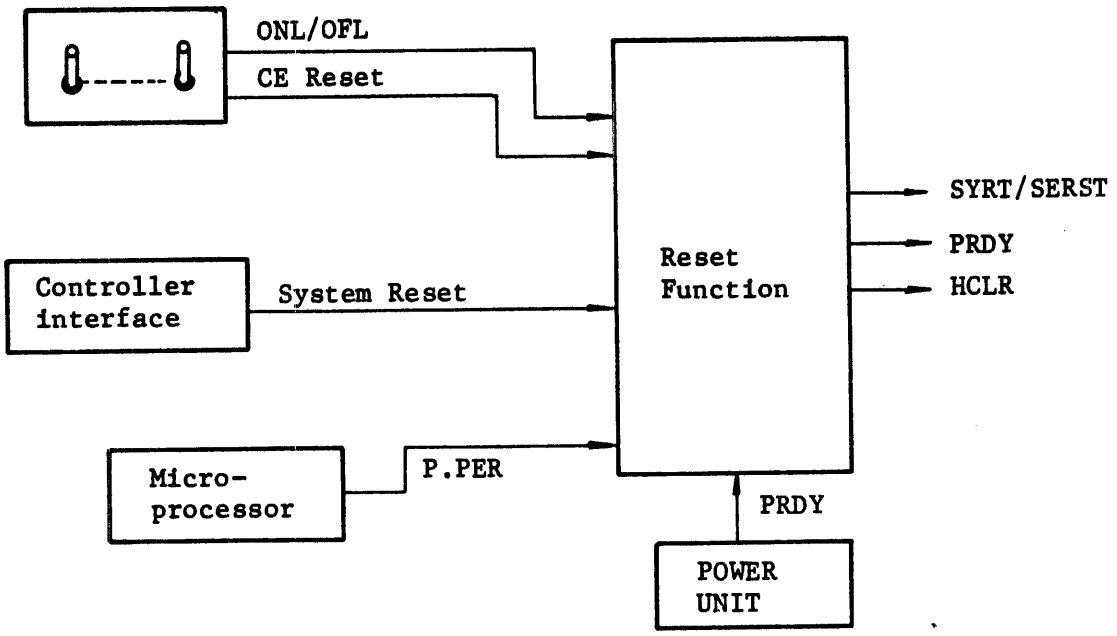


Figure 4.3 Reset function

The HCLR signal is to the demodulation PCA, write control PCA, read control PCA, 800 RPI control PCA, etc., so that these circuits can be reset to their initial status.

The PRDY signal restores the FMT to a power-on status.

The SYRT signal restores the FMT to an idle status.

Table 4.1 Conditions that generate reset signals

Condition	SYRT	PRDY	HCLR
Power On/Off (PRDY)	Yes	Yes	Yes
ONL/OFL SW on Field Tester (R.OFL)	Yes	No	Yes
System Reset from the Controller	Yes	No	Yes
PERR	No	No	Yes

4.3 Clock System

The clock circuit in the FMT section is configured so that the MTU can operate in a recording densitys of 6250 RPI, 1600 RPI, and 800 RPI at running speeds of 75 IPS, 125 IPS, and 200 IPS, respectively. As shown in Table 4.2, the clock circuit is provided with six crystal oscillators. The crystal oscillator outputs are divided and phase corrected so that five basic clock pulses are generated. Figure 4.4 shows the configuration of the clock circuit.

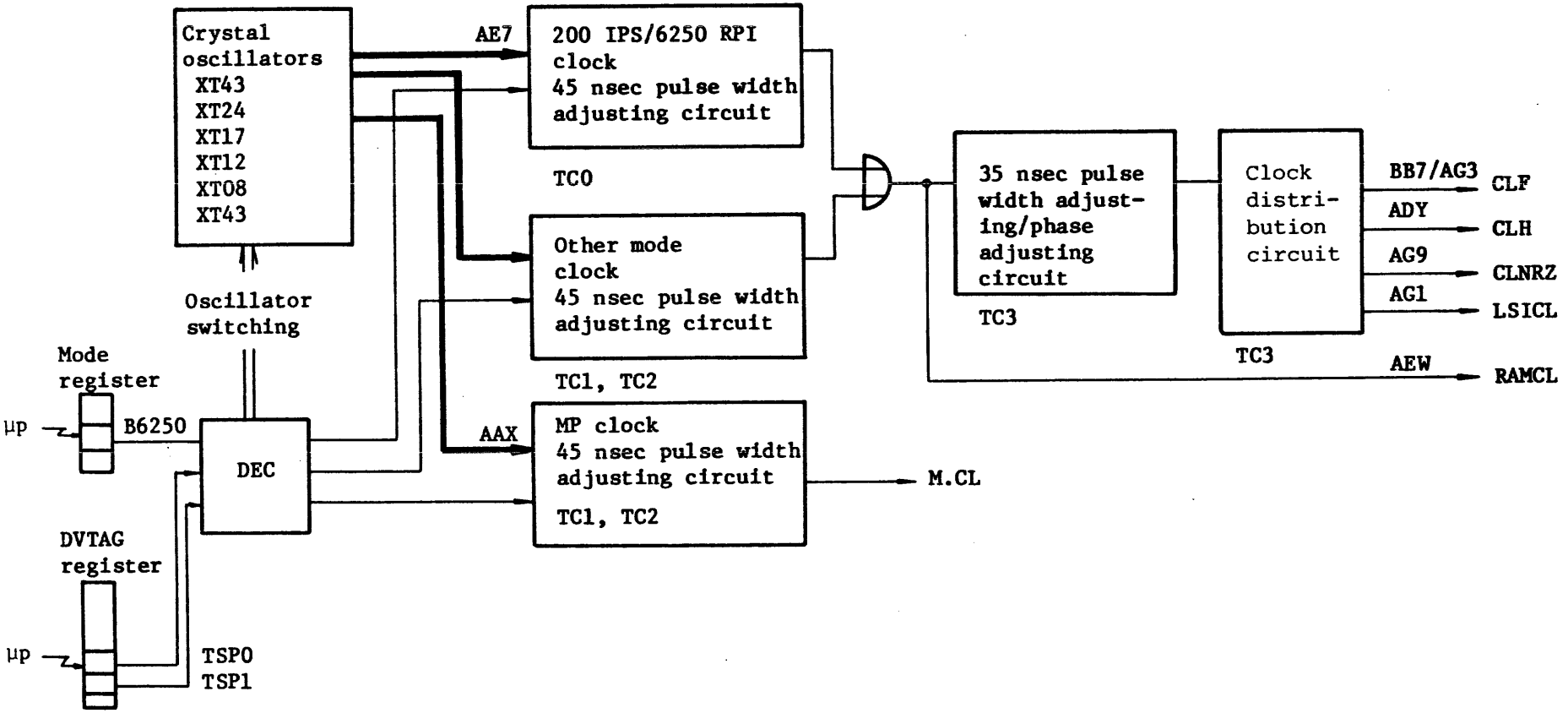


Figure 4.4 Clock circuit configuration

(1) CLF (Clock Full), CLH (Clock Half)

These clock pulses are fed to the format/deformat circuit*. Table 4.2 shows the crystal oscillators used and their clock pulse widths.

(2) CLNRZ (Clock NRZI)

This clock pulse is fed to the PCA 1A101 (800 RPI option).

(3) LSICL (LSI Clock)

This clock pulse is fed to the LSI of the format/deformat circuit*. It assists the phase adjusting cicuit adjust the phase difference between CLF/CLH and LSICL.

(4) RAMCL (RAM Clock)

This clock pulse is fed to the deskewing buffer in the deformat circuit*.

(5) M.CL (Micro Clock)

This clock pulse is fed to the microprocessor. The pulse width is 45 nsec and the period is 208 nsec.

*The format/deformat circuit includes the write control (format circuit). Read control, 800 RPI control and demodulation sections (deformat circuit).

Table 4.2 Clock pulse period for each running speed/recording density (The figures in parentheses refer to pulse widths)

Clock / Mode	CLF(ns) (35 ns)	CLH(ns) (35 ns)	CLNRZ(ns) (35 ns)	LSICL(ns) (35 ns)	RAMCL(ns) (45 ns)	Used Oscillator (ns)
200 IPS 6250 BPI	184.4	92.2	92.2	92.2	184.4	XT43 92.16
200 IPS 1600/ 800 BPI	520.8	260.4	130.2	260.4	520.8	XT12 65.11
125 IPS 6250 BPI	294.4	147.2	147.2	147.2	294.4	XT24 73.73
125 IPS 1600/ 800 BPI	833.2	416.6	208.3	416.6	833.2	XT08 104.17
75 IPS 6250 BPI	494.4	247.2	494.4	247.2	494.4	XT17 123.40
75 IPS 1600/ 800 BPI	1388.8	694.4	347.2	694.4	1388.8	XT48 86.81
50 IPS 6250 BPI	737.6	368.8	368.8	368.8	737.6	XT43 92.17
50 IPS 1600/ 800 BPI	2083.2	1041.6	520.8	1041.6	2083.2	XT12 65.11

4.4 Microprocessor

4.4.1 Microprocessor configuration

Figure 4.5 is a block diagram of the microprocessor configuration. Table 4.3 shows the major performance characteristics of the microprocessor. The microprocesser,(a 32-bit fixed/variable length instruction type processor) is so configured that it can execute a microprogram of up to 8k steps. The microprocessor fetches an instruction from the control storage (CS) section into the CS register (CSR); decodes the instruction; processes and evaluates data, on the LSR/EXR; stores the data and jumps to a specified step. The sequencer controls the program flow by advancing steps one by one, jumping or branching to a specified step, stacking control information and data on a specified step, and stacking control information and data on a Subroutine Call/Return. The sequence also contains the microprogram address register (CSAR: CS address register).

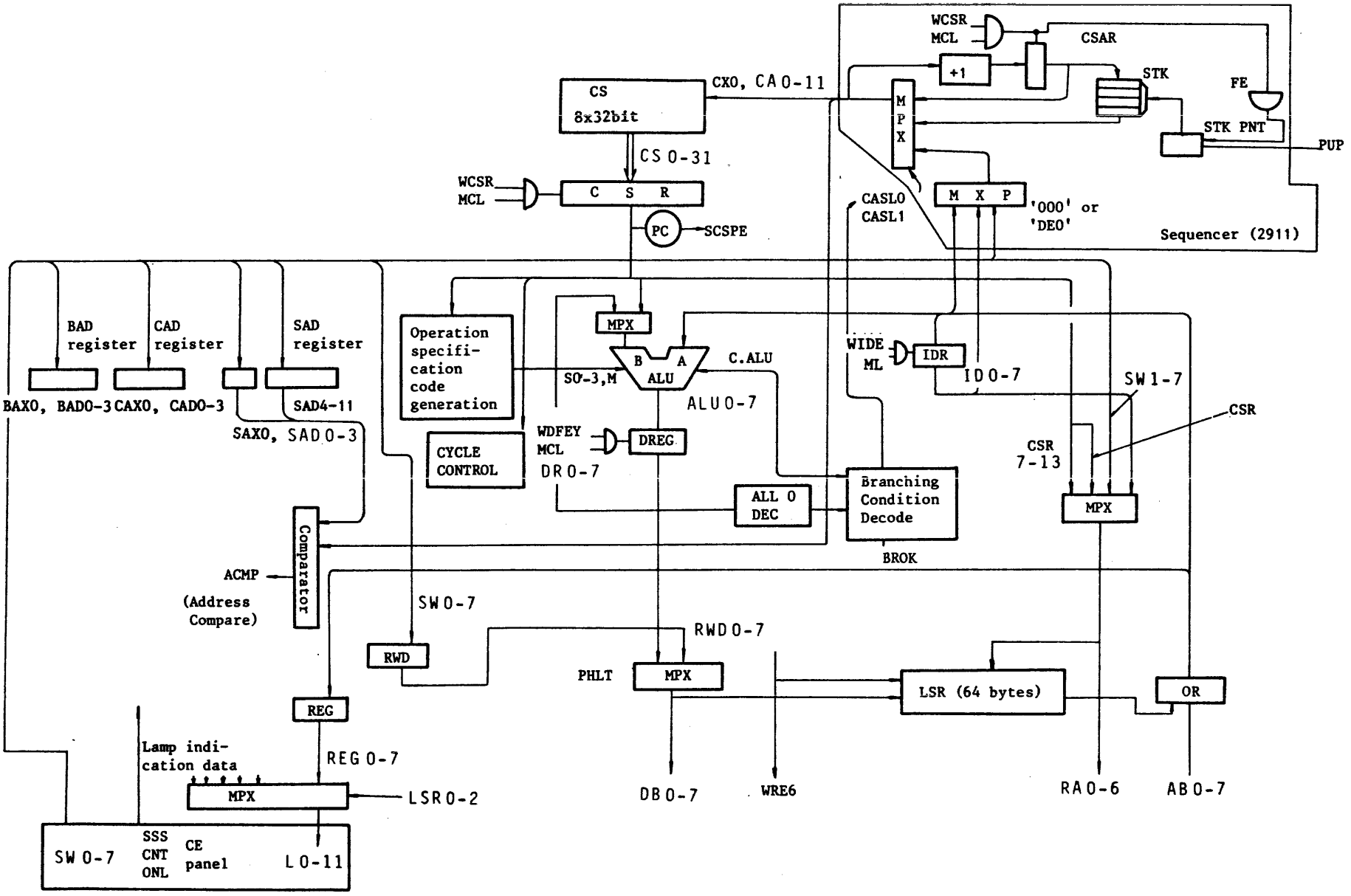


Figure 4.5 Microprocessor configuration

Table 4.3 Major performance characteristics of processor

Item	Performance
Basic clock	208 ns (ϕ)
Instruction execution time	416 ns (2ϕ), 624 ns (3ϕ) 832 ns (4ϕ), 1.04 ns (5ϕ)
Number of instruction types	38 types
Instruction bit length	32 bits (including parity bits)
Instruction counter	13 bits (maximum of 8K steps)
External register (EXR)	Up to 64 bytes
Internal register (LSR)	64 bytes
Number of interrupt sources	5
Interrupt mask	Possible for each interrupt
CS access time	200 ns or less
Subroutine nesting	Up to 4 levels
Others	CS parity check, LSR parity check, Address Compare, CS scan, step function, CE panel functions, etc.

4.4.2 Processor cycle control

Figure 4.6 shows the cycle timing control of the processor. The Read Cycle (RCY) signal conveys the timing to access the LSR/EXR, etc. The Write Cycle (WCY) signal conveys the timing to operate, evaluate, and store data. The Extend Cycle 1 (EXCY1) and Extend Cycle 2 (EXCY2) signals control the extended cycle when Extend Cycle instruction is executed. The WCY signal can be extended by one clock by a Branch Condition OK (BCOK) signal to be generated when control is branched by a Branch instruction to an address other than the next address.

The C.WCY signal conveys the timing to fetch an instruction to the CSR. The instruction is set on the CSR at the timing of the trailing edge of the C.WCY signal (the trailing edge of the WCSR signal). The P.WCY signal conveys the timing to store data into the EXR or LSR.

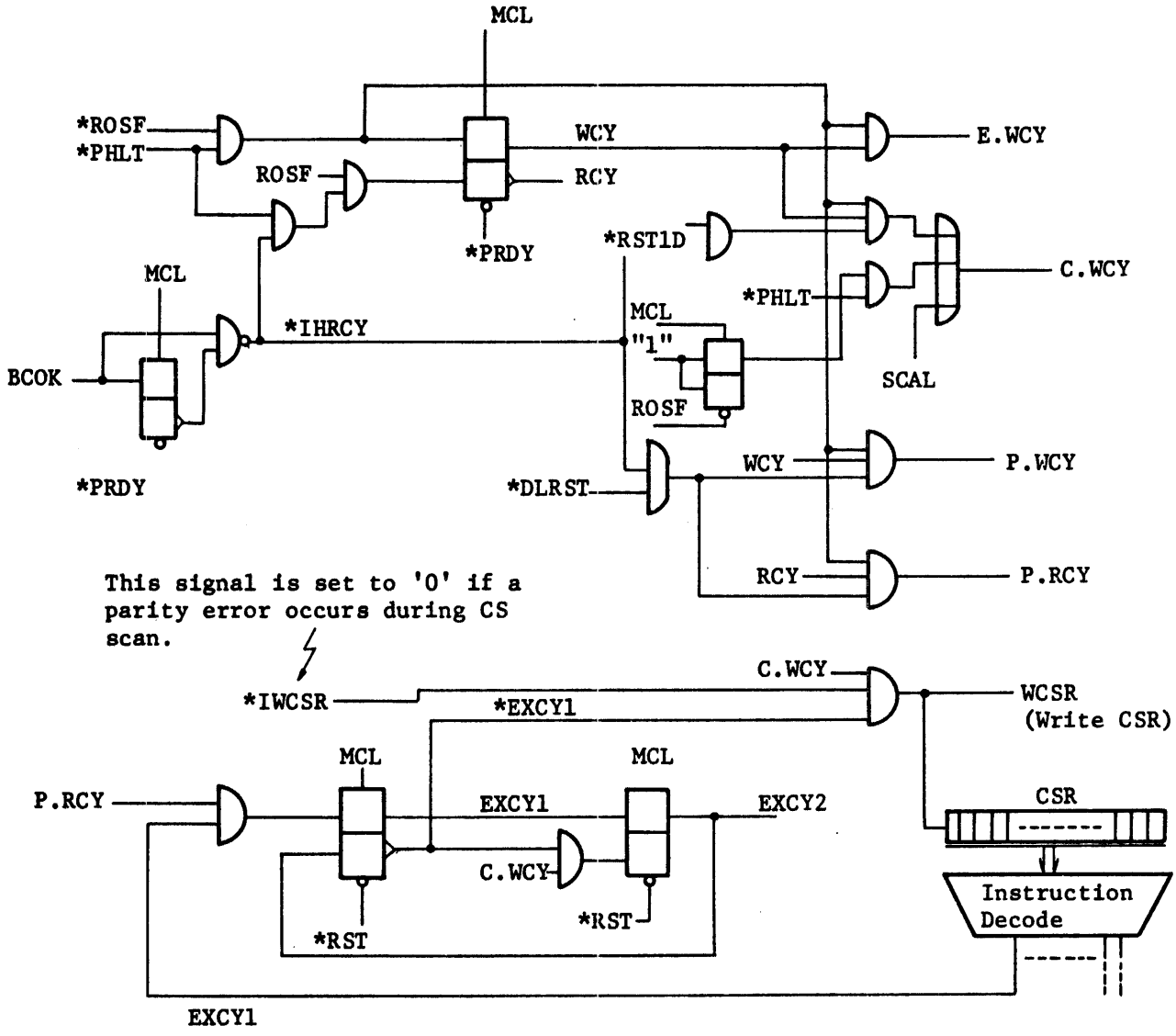


Figure 4.6 Processor timing control circuit

Figure 4.7 is a timing chart showing when the processor will start with address '0' after resetting the circuit by a Reset (S.CLR) signal.

Table 4.4 shows the bit assignment (configuration) of each instruction for the processor. The timing operation within the processor is controlled by the I, S, RTN, T, and DE bits.

PROCESSOR START

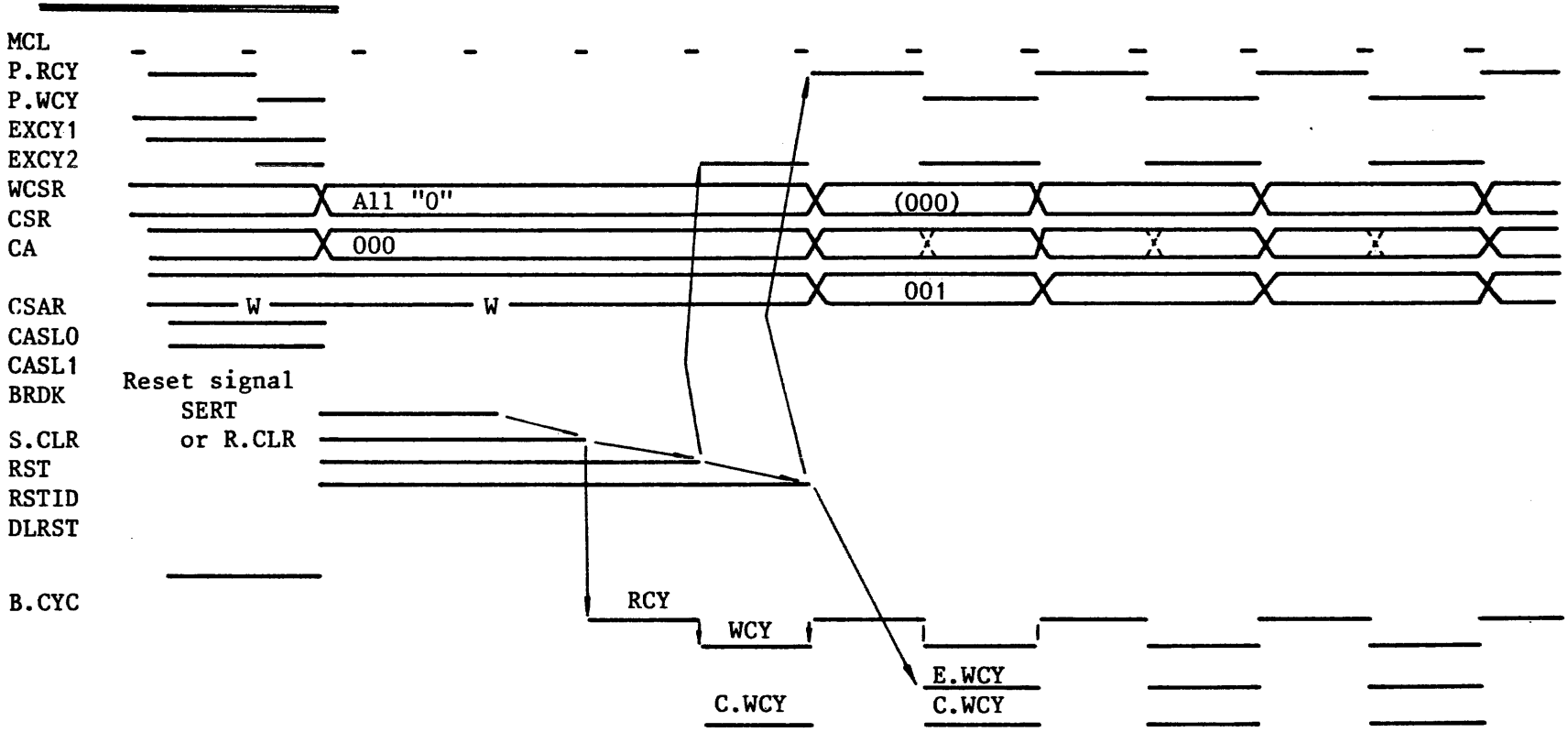


Figure 4.7 Processor start timing chart

Table 4.4 Instruction code configuration

Kind of Instruction	OP			EOP				Source Reg							Immediate data / Branch Adrs / Destination Reg															P	Mnemonic
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Branch Uncondition	1	0	0	I	S			Source Reg if I = '1'															Branch Adrs								Invalid if I='1'		P	B, CALL, BI, CALLI
Branch on condition	1	0	1	I	S	RV	C	Source Reg if I = '1'															Branch Adrs								Invalid if I='1'		P	BOC, COC BOCI, COCI
Test Bit & Branch	1	1	0/1	I	S	RV	C	Source Reg							Immediate data								Branch Adrs										P	TBB,TBC TBBI,TBCI / BEQ,BNE, CEQ,CNE BEQI, BNEI, CEDI, CNEI
ALU Immediate	0	0	RTN	I	ALU			Source Reg							Immediate data								T	DE	Destination Reg if I='0'							P	MV,MV* MVHI, MVHI* MVFI, MVFI* LD, LDI, LD*, LDI*
ALU Register	0	1	RTN		ALU			Source Reg															T		Destination Reg							P	MF, MF* MFD, MFD*

I : Indirect bit
S : Adrs Stack; '1' if Subroutine Call
RTN : Return; '1' if returned from a subroutine
T : Test; ALU output data is not stored in the destination register if T='1'
DE : Stored in the source register if '1'

4.4.3 Interrupt (Trap)

A trap to the microprocessor results from any of five types of sources to each of which a trap sector address is assigned, as shown in Table 4.5.

Table 4.5 Sources of trap

Trap signal		Trap address (Hex.)	Mask bit
Name	Description		
DVINT	Device interrupt is an interrupt signal from a MTU and is set to '1' if a BOT is detected while the MTU is running in the reverse direction or a SAGC error has occurred.	(0100)	M.INT bit (TMSK bit)
TMINT	Timer interrupt is an overflow signal from the timer circuit. The timer circuit stops operating after this signal is generated.		M.TMR bit (TMSK bit)
ISINT	Initial Selection Interrupt is an interrupt signal from the controller interface circuit afnd is generated at the beginning of the initial selection sequence. It is reset when a microprogram sets the Busy signal to on. Also, an interrupt can be issued from the field tester while the FMT is offline.	(1100)	M.INS bit (TMSK bit)
TCSTP	Tacho-Stop. This interrupt signal is generated when the period of tacho pulses from a MTU has increased abnormally.	(0100)	M.TCS bit (TMSK bit)
PERR	This interrupt signal is set on when a ROM parity error or a LSR parity error occurs.	(00E0)	None (TMSK bit)

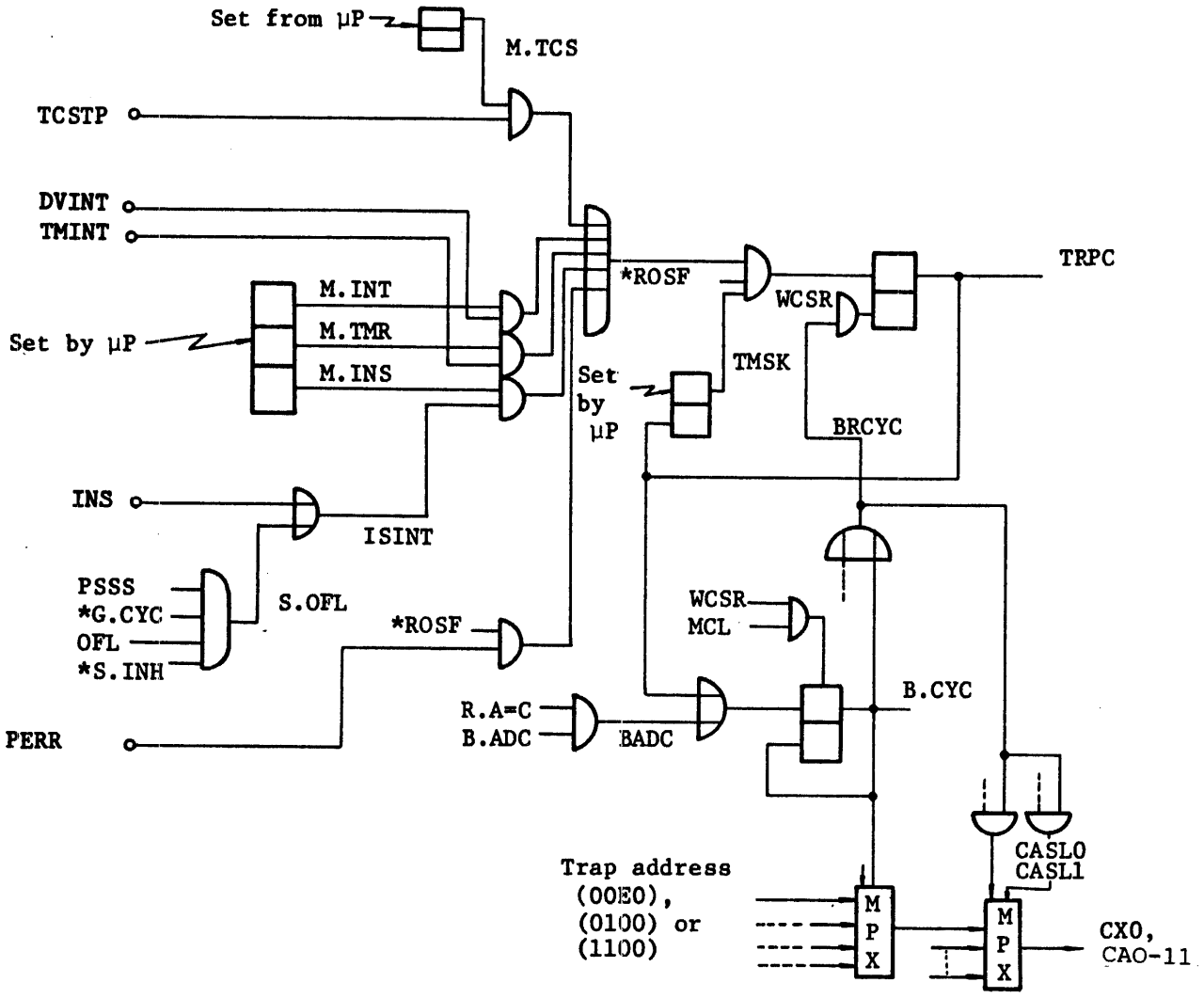


Figure 4.8 Trap control circuit

The processor can be interrupted while a Trap Mask (TMSK) signal is set to on. The TMSK signal is reset after the interrupt has been accepted. No other interrupts can be accepted until TMSK is set to on by the microprogram. After the TRPC signal is set to on, a Branch Cycle (B.CYC) signal is generated at the timing of the WCSR signal (end of executing an instruction). The B.CYC signal acts on the sequencer circuit so that the microprogram address is switched to the address.

Thus, the instruction stored at the trap address begins at the second instruction cycle after the trap was issued.

4.4.4 Field Tester

The field tester is a control panel consisting of switches and lamps used for maintenance. It can stop, advance, and start the microprocessor; rewrite the contents of the LSR (Local Storage Register), EXR (External Registers), and microprogram address register; scan the contents of the CS (Control Storage); and realize various indication functions by connecting it to FMT PCA 1A08.

Lamps L0 to L11 light when switches SW0 to SW7 are set to a specified status. To specify a particular function, set switches SW0 to SW7 as described in the Maintenace Manual, and toggle the CNT (Control) switch. To send control information (such as stop address, branch address, program address, and write data), set switches SW0 to SW7 as described in the Maintenace Manual, and toggle the SSS (Start/Stop/Set) switch. While the control information is being requested by the SW0 to SW7 switches, each of S.BAD, S.CAD, S.SAD, W.REG, and S.MOD signals is set to on. These signals show that the SW0 to SW7 switches are operating in the control information input mode until they are reset by a PSSS signal (timing pulse generated at the rise of the SSS switch). This section describe major operations of the field tester.

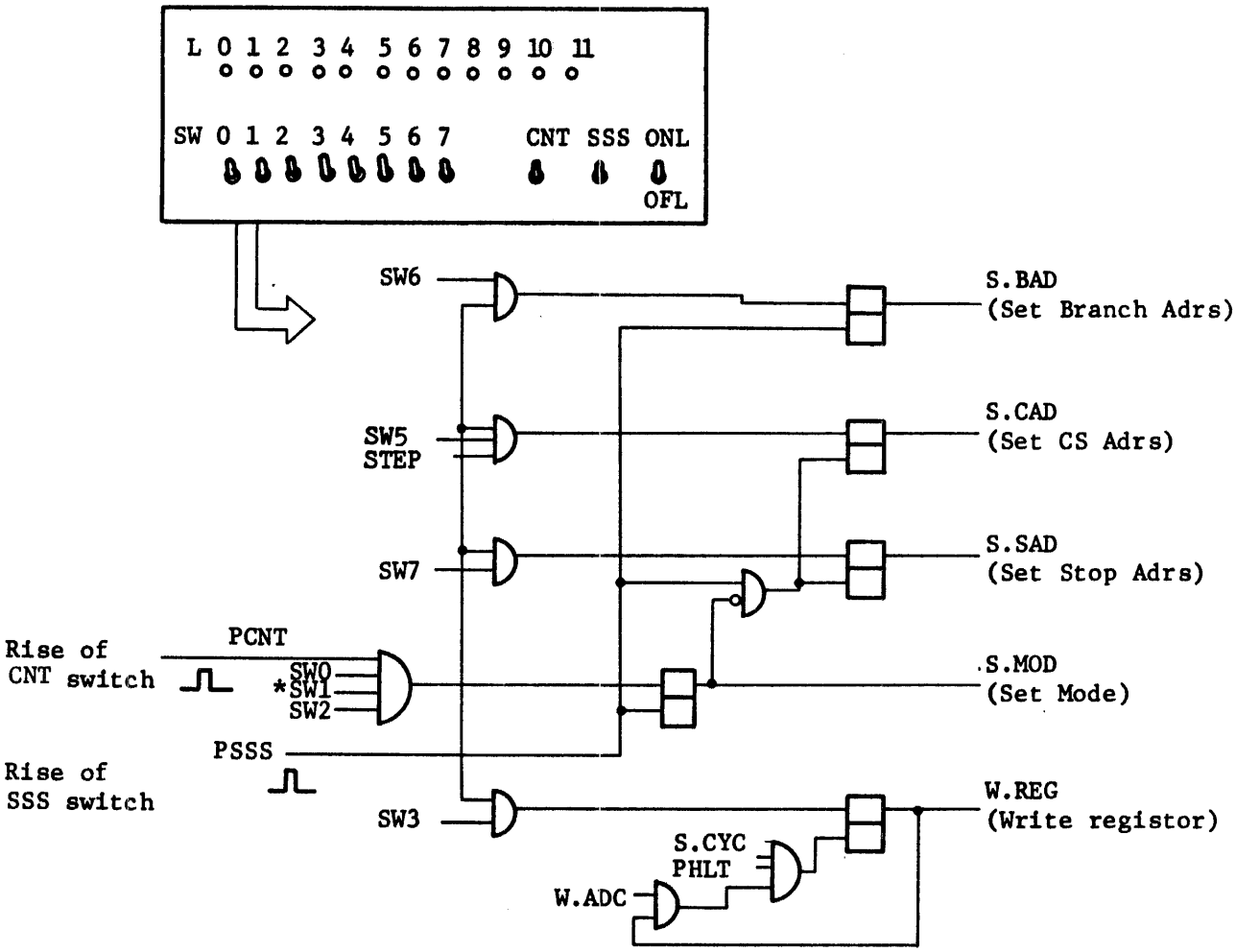


Figure 4.9 Input mode control over switches

(1) Step

As shown in Figure 4.10, if the CNT switch is set on when the SWO-2 switches are set to on; then the Set MP-Control F(S.MPC) signal is set to on. If switch SW4 has then been set to on, the STEP bit is set to on. The Step signal generates a Processor Halt (PHLT) signal at the timing of fetching an instruction so that the processor is halted under the condition of RCY (See section 4.4.2 0). Then, the PHLT signal is reset for one intruction period whenever the SSS switch is toggled. Thus, instructions are exceuted one by one. The G.CYC signal becomes '1' while SWO to SW7 switches are operating in the control information input mode. Even if the SSS switch is then set to on, PHLT signal is not reset and the processor does not step further.

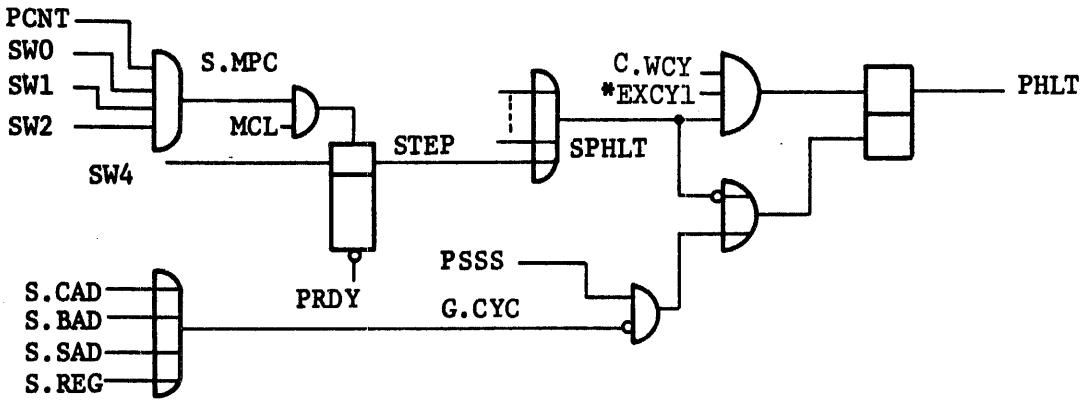


Figure 4.10 Halt control

(2) Address compare/address compare stop

If the CNT switch is set to on when the SWO-2 switches are set to '101' and the SW7 switch set to '1', then the S.SAD and S.MOD signals are set to on and the SWO-3 switches are set to the high order compare address input mode. Data is then entered to stop addresses 0 to 3 (SADO to SAD3) by the SSS switch and the S.MOD signal is reset so that the low order compare address (SAD4-11) can be entered. Thus, the address set in the SAD register is compared with CAO-11 within the comparator. If the result of the comparison (P.C = S signal) is output and the S.ADC bit has been set on, then a PHLT signal is set to on. Then, if the SSS switch is set to on, the address compare latch signal (F.C=S) and the PHLT signal are reset.

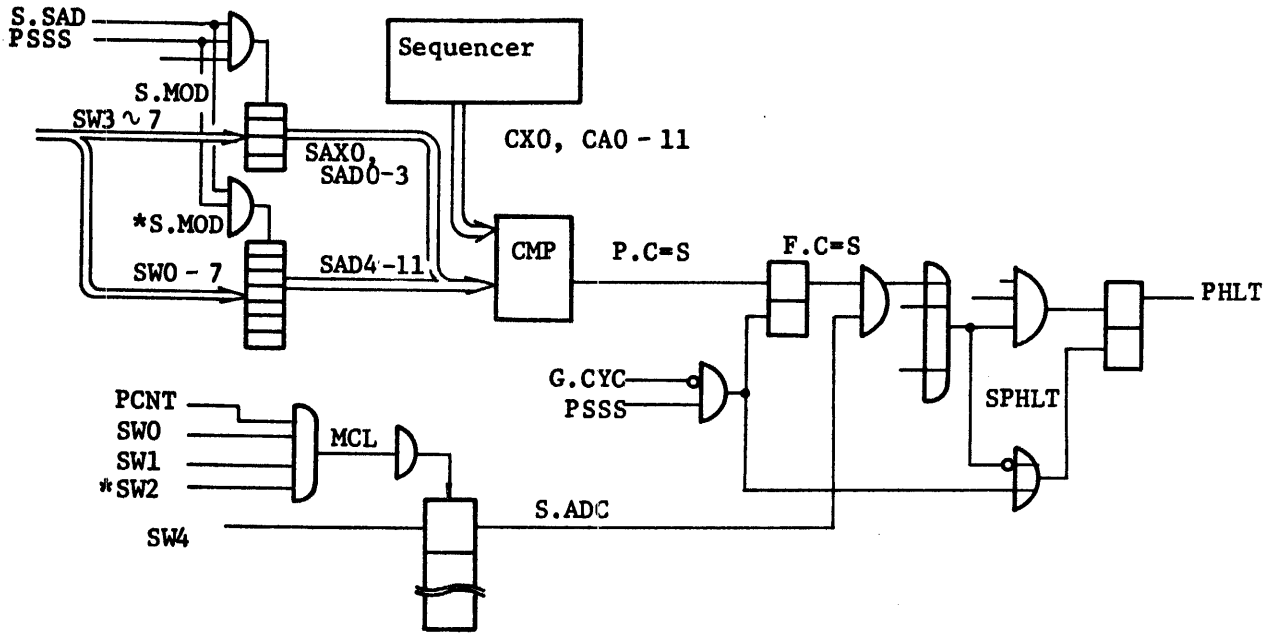


Figure 4.11 Address compare & stop

(3) Register write/display

As shown in Figure 4.12, if the PHLT signal is set to on, the contents of SWI to SW7 are output to register addresses RAO to RA6 and the contents of the RWD register are output data bus of the processor. While the PHLT signal is set to on, data is written and displayed to the register. Data is set on the read/write data (RWD) register in the following way: set the SWO to SW3 switches to '1011' and set the CNT switch to '1'. This causes the SWO to SW7 switches to be set to the RWD register input mode. Set the SWO to SW7 switches to desired data and toggle the SSS switch. The W.REG signal directs the register write mode. The Steal Cycle (S.CYC) signal serves as a write strobe (W.REG) signal for the Register Write/Display.

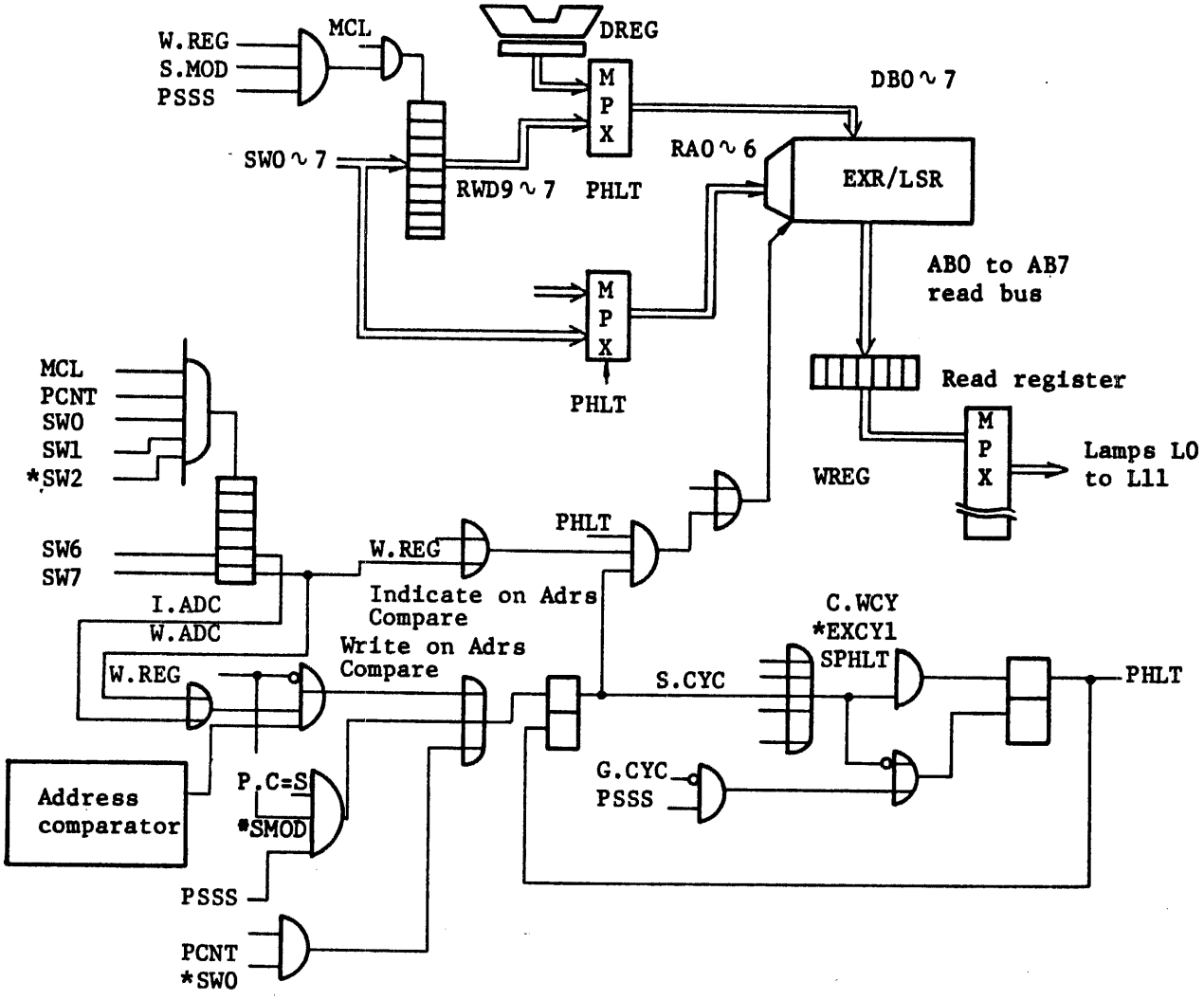


Figure 4.12 Register write/display

(4) Micro program address set

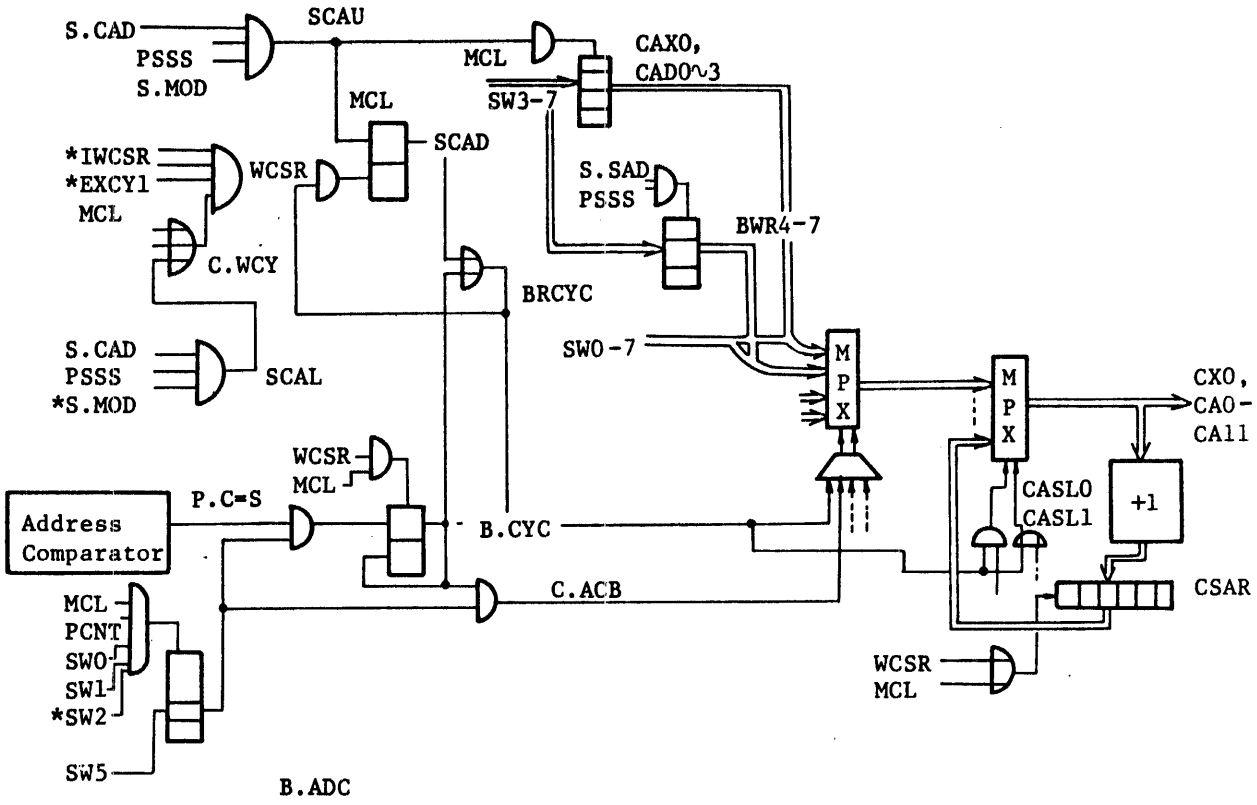


Figure 4.13 CA set

As shown on Figure 4.13, if the CNT switch is set to on when the SW0-3 switches are set to '101', the S.CAD and S.MOD signals are set on which enables the CA Set mode. Then, if the SSS switch is toggled with SW0 to SWW3 set to the high order four bits of the CS address (microprogram address), the CAD register is set to the data in SW0 to SW7. The S.MOD signal is then reset. Then, if SW0 to SW7 are set to the contents of the low order eight bits of the CS address, the CA signal is switched to the contents of the BAD register and SW0 to SW7. Finally, if the SSS switch is set on, the instruction at the specified address is loaded into the CSR and the address register updated.

(5) Address Compare Branch

If the CNT switch is set to on when SWO-2 are set to '110', the B.ADC bit is set to on so that this function is activated. If address comparison is successful when the B.ADC bit is '1', the B.CYC signal is set to on. The CA signal (microprogram address) is switched to the contents of the high order four bits of the BAD register (previously set) and to the contents of SWO to SW7 (low order eight bits). The branch function is then activated so that the instruction stored at the address specified by the BAD register and SWO to SW7 can be executed next. Figure 4.25 shows the associated circuits.

(6) CS Scan

If the ROS function (ROSF) bit is set on, the ROSF signal is set to on and the C.WCY silgnal always becomes '1'. This causes the contents of the CS to be read into the CRS at every clock (MCL) pulse and the address register to increment. If a parity error occurs during scanning, an Inhibit Write-CSR (IWCRS) signal is set to on which halts the processor.

4.4.5 Microprogram instructions

Every instruction to be executed in the microprocessor is a 32-bit fixed length format. The processor provides 38 types of mnemonic instructions; each of which can perform branching, conditional branching, operating, and storing data in a register. This section describes the functions, bit patterns, and cycle lengths of these instructions. Also, ASSEMBLER coding schemes are inserted for reference.

Unconditional Branch instructions

1 B (Branch Uncondition)

B destination

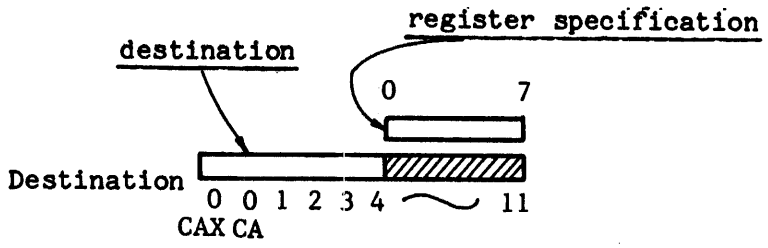
Unconditionally branches to the destination.

Example:
```
B   LABEL1
B   *
B   X'0256'
```

2 BI (Branch Indirect)

BI destination, register specification.

Branches to the address resulting from replacing the low order eight bits of the destination address (represented by the above destination operand) with the contents of the register specified by the register specification operand.



Example: BI CMDDEC, R1

3 CALL (Call Subroutine)

CALL subroutine name.

Branches to the subroutine, with the next address stacked.

Example: CALL SUB1

4 CALLI (Call Subroutine Indirect)

CALLI subroutine name, register specification.

Branches to the subroutine address (resulting from replacing the low order eight bits of the destinated subroutine address value with the contents of the register specified by the register specification operand), with the next address stacked before the branching.

Example: CALLI SUBX, R0

Conditional Branch instructions

5 BOC (Branch On Condition)

BOC condition specification, destination.

Branches to the destination if the condition register is in the status specified by the condition specification operand.

Condition register =DREG — Method of specifying conditions

ALL0	all bit = 0
CAR	CAR bit on
ANY1	any bit = 1
NCAR	CAR bit off

Example:
```
BOC   ALL0, RDEND
BOC   ANY1, STOPWT
```

6 BOCI (Branch On Condition Indirect)

BOCI condition specification, destination, register specification.

Conforms to BOC except that the destination address depends on the high order four bits of the destination and the contents (eight bits) of the specified register.

Example: BOCI CAR, LABEL1, R3

7 COC (Call Subroutine On Condition)

COC condition specification, subroutine name.

Branches to the subroutine specified by the subroutine name operand if the condition register is in the status specified by the condition specification operand.

Example: COC ANY1, GOUP

8 COCI (Call Subroutine On Condition Indirect)

COCI condition specification, subroutine name, register specification

Conforms to COC except that the called subroutine address depends on the high order four bits of the address specified by the subroutine name operand and the contents (eight bits) of the register specified.

Example: COCI NCAR, SUB1, R6

9 TBB (Test Bit & Branch)

TBB condition specification, register specification, test bit specification, destination within page.

Branches to the destination if the bit corresponding to the test bit specification = '1' if the contents of the register specified by the register specification operand is in the status specified by the condition specification operand.

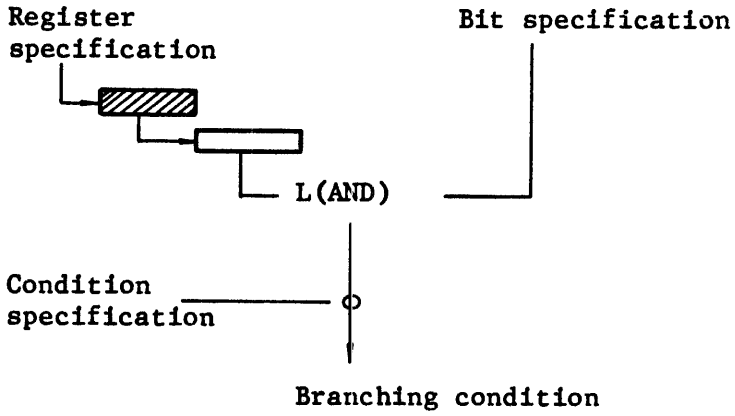
ALL0	all bit 0
ALL1	all bit 1
ANY1	any bit 1
ANY0	any bit 0

```
Example:  TBB   ANY1, WREG, X'0F', LABEL1
          TBB   ALL0, RL, 4, GOON1
```

10 TBBI (Test Bit & Branch Indirect)

TBBI condition specification, register specification, test bit specification, destination within page

Branches to the destination if the bit corresponding to the test bit specification = '1' if the contents of the register specified by the register specification operand is in the status specified by the condition specification operand. For the condition specification operand, refer to the TBB.



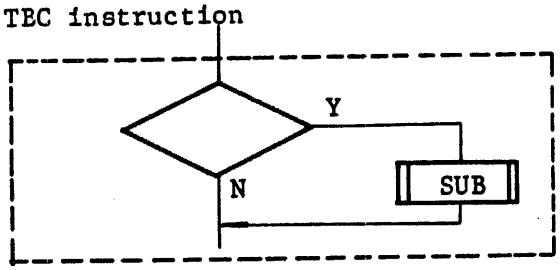

```
Example:  TBBI   ANY0, R1, X'=0', LABEL2
          TBBI   ALL1, REG1, 4+2+8+16, START1
```

NOTE; "Page" means 512 addresses boundary.

11 TBC (Test Bit & Call Subroutine)

TBC condition specification, register specification, test bit specification, subroutine name within page

Executes the subroutine specified by the subroutine name operand if the result of ANDing the contents of the register specified by the register specification operand with the test bit specification becomes the status specified by the condition specification operand. If the condition is not satisfied or a Return instruction in encountered in the subroutine, then the next instruction is executed.



For the condition specification operand, refer to TBB. instruction. Also, the ANDed result remains in the DREG (condition register).

Example: TEC ANY1, AREG, X'24', SUBABC
TEC ALL0, R1, B(456-8), GOUPSUB

12 TBCI (Test Bit & Call Indirect)

TBCI condition specification, register specification, mask data, subroutine name within page

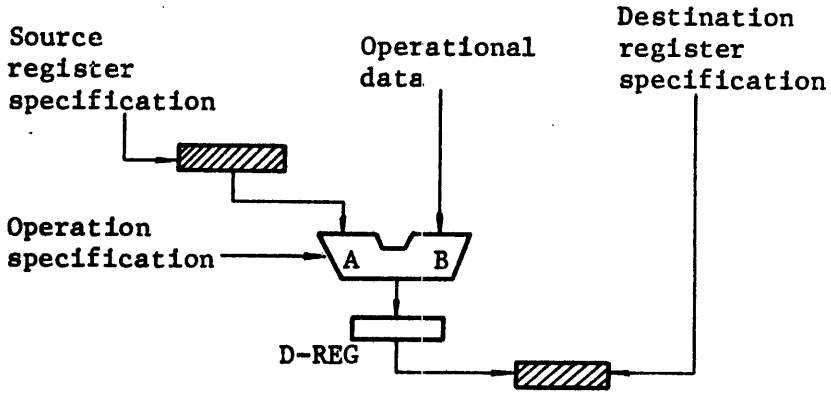
Executes the subroutine specified by the subroutine name operand if the result of ANDing the contents of the register indirectly specified by the contents of the register specified by the register specification operand with the mask data becomes the status specified by the condition specification operand.
The ANDed result remains in the DREG. For the condition specification operand, refer to the TBB instruction.

Example: TBCI ANY0, R0, 80+40, SUB0

14 MV (Move)
MV* (Move & Return)

{MV / MV*}	source register specification ,	operation specification ,	constant ,	destination register specification

Performs the operation specified by the operation specification operand between the content of the register specified by the source register specification operand and the operational data. The result of the operation is then stored in the register specified by the destination register specification operand.



- The operated result remains in the DREG.
- The MV* instruction is accompanied by a return from the subroutine.
- The operation specification operand conforms to the following table.

Table 4.6 Operation specifications

	Operation specification	Data to be stored	Abbreviation
F=B	IMD	Data written in the operational data operand	C
	DREG	DREG contents	D
F=A.B	AND	(Source register contents)* (Operational data)	A
F=AVB	OR	(Source register contents)V (Operational data)	O
F=A⊕B	EOR	(Source register contents)⊕ (Operational data)	E
F=A	SREG	Source register contents	S
F=A+B	PLS	(Source register contents)+ (Operational data)	P
F=A-B	MNS	(Source register contents)- (Operational data)	M

where A and B refer to source data.

```
Example:  MV    R1, AND, X'F2', R1
          MV*   R2, PLS, 31, R3
```

14a STR (Store Register)
STR* (Store Register & Return)

{STR / STR*} data, register

Sets the register specified by the second operand to the data specified by the first operand.

These instructions conform to the following MV and MV* instructions:

{MV / MV*} 0, IMD, data, register

Example:
```
STR    X'30', R1
STR*   D(256-38), W0
```

14b MVR (Move Register)
MVR* (Move Register & Return)

{MVR / MVR*} source register, destination register

Stores the contents of the source register into the destination register.

The contents of the source register remain in the DREG.

These instructions conform to the following MV and MV* instructions:

{MV / MV*} source register, S, 0, destination register

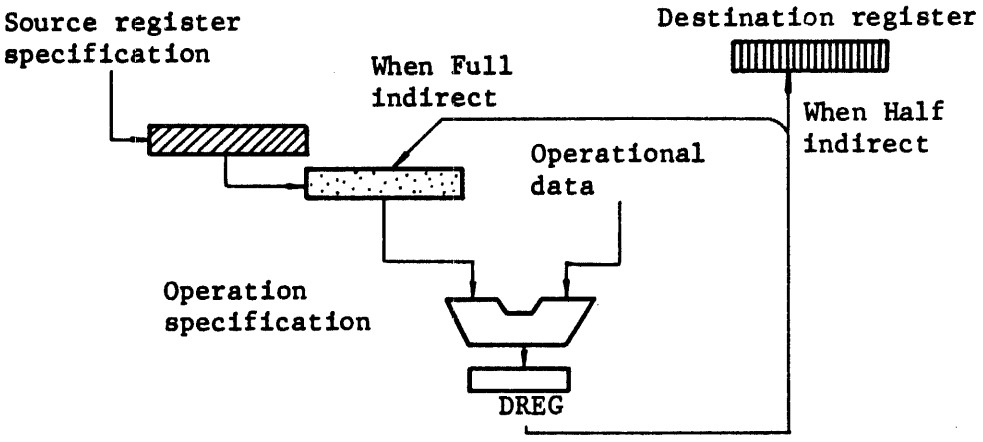
Example:
```
MVR   R1, R2
```

15 MVFI (Move Full Indirect)
MVHI (Move Half Indirect)
MVFI* (Move Full Indirect & Return)
MVHI* (Move Half Indirect & Return)

MVFI MVHI MVFI* MVHI*	source register specification ,	operation specification ,	operational data ,	[destination register specification (*1)]

1 Write this operand only for MVHI and MVHI instructions.

Performs the operation specified by the operation specification operand between the contents of the register specified indirectly by the contents of the register specified by the source register specification operand and the operational data. The operation result is then stored in the register indirectly specified by the contents of the register specified by the source register specification operand for a mVFI or MVFI* instruction; into the register specified by the destination register specification operand for a MVHI or MVHI* instruction.



The operated result remains in the DREG.
The MVFI* and MVHI* are accompanied by a return from the subroutine.
The operation specification operand conforms to that of the MV instruction.

```
Example:  MVFI    R0, OR, 512
          MVHI    R0, PLS, B(310), REGABC
          MVFI*   AREG, EOR, X'32'
          MVHI*   X, MNS, 32-5+8, R4
```

16 LD (Load D-register)
LD* (Load D-register & Return)

```
{LD }          source
{LD*}          register          operation          operational
               specifi-          specifi-           data
               cation   ,        cation    ,
```

Performs the operation specified by the operation specification operand between the contents of the register specified by the source register specification operand and the operational data. The DREG is then set to the operation result.

The contents of registers other than the DREG do not change.

The operation specification operand conforms to that of the MV instruction.

The LD* instruction is accompanied by a return from the subroutine.

```
Example:  LD     XREG, IMD, X'43'
          LD*    W0, PLS, 1
```

17 LDI (Load D-register Indirect)
LDI* (Load D-register Indirect & Return)

```
{IDI }         source
{IDI*}         register          operation          operational
               specifi-          specifi-           data
               cation   ,        cation    ,
```

Performs the operation specified by the operation specification operand between the contents of the register indirectly specified by the contents of the register specified by the source register specification operand. The DREG is then set to the operation results.

The contents of registers other than the DREG do not change.

The operation specification operand conforms to the MV instruction.

The LDI* instruction is accompanied by a return operation.

```
Example:  LDI    EXR0, SREG, X'80'
          LDI*   W0, AND, B(40+80)
```

MF system (inter-register operation system) instructions

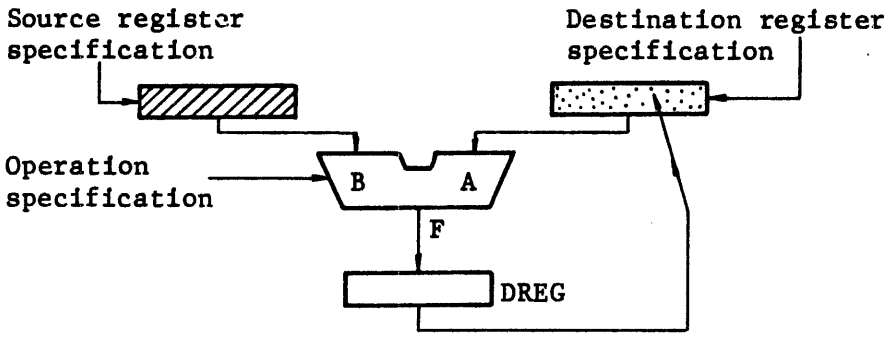
18 MF (Modify)
MF* (Modify & Return)

{MF / MF*}	source register specifi- cation	,	operation specifi- cation	,	destination register specification

Performs the operation specified by the operation specification operand between the contents of the register specified by the source register specification operand and the register specified by the destination register specification operand. The operation result is the stored in the destination register.

The operated result remains in the DREG.

The MF* instruction is accompanied by a return from the subroutine.



The operation specification operand of any MF system instruction can be specified as follows:

Table 4.7 Operation specification

	Specification	Operation
F=$\overline{A}$.B	NA	$\overline{\text{(Source register)}}$ * (Destination register)
F=$\overline{A}$VB	NO	$\overline{\text{(Source register)}}$ V (Destination register)
F=A.B	AND or A	(Source register) * (Destination register)
F=AVB	OR or O	(Source register) V (Destination register)
F=A⊕B	EOR or E	(Source register) ⊕ (Destination register)
F=$\overline{A \oplus B}$	EN	$\overline{\text{(Source register)} \oplus \text{(Destination register)}}$
F=A+B	PLS or P	(Destination register) + (Source register)
F=A-B	MNS or M	(Destination register) - (Source register)

where A: destination
B: source

Example: MF R1, A, BREG
MF R0, NO, R1

19 MFD (Modify D-register)
MFD* (Modify D-register & Return)

{MFD / MFD*} source register specification , operation specification , destination register specification

Performs the operation specified by the operation specification operand between the contents of the source register and those of the destination register. The operation result is then stored in the DREG.

Conforms to the MF and MFD* instructions except that the operation result is not stored in the destination register

The MFG* instruction is accompanied by a return operation.

The operation specification operand conforms to that of the MF and MF* instructions.

Example: MFD R1, NA, R2

Relational instructions

20 **BEQ (Branch If Equal)**

BEQ register specification, relational data, destination within page

Branches to the destination if the contents of the register specified by the register specification operand coincide with the relational data.

The result of EXCL-ORing the contents of the register with the relational data remains in the DREG.

Example: BEQ W0, X'43', LABEL2

21 **BEQI (Branch If Equal Indirect)**

BEQI register specification, relational data, destination within page

Branches to the destination if the relational data coincides with the contents of the register with the address contained in the register specified by the register specification operand.

The result of the EXCL-OR operation remains in the DREG.

Example: BEQ I0, 100, AAA01

22 **CEQ (Call Subroutine If Equal)**

CEQ register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data coincides with the contents of the register specified by the register specification operand.

The result of the EXCL-OR operation remains in the DREG, similar to the BEQ instruction.

Example: CEQ W2, 523, SUB1

23 **CEQI (Call Subroutine If Equal Indirect)**

CEQI register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data coincides with the contents of the register with the address contained in the register specified by the register specification operand.

The result of the EXCL-OR operation remains in the DREG.

Example: CEQI R1, X'3A', SUBX

[24] BNE (Branch If Not Equal)

BNE register specification, relational data, destination within page

Branches to the destination specified by the destination operand if the relational data does not coincide with the contents of the register specified by the register specification operand.

The result of the EXCL-OR operation remains in the DREG.

Example: BNE R1, X'01', LABEL3

[25] BNEI (Branch If Not Equal Indirect)

BNEI register specification, relational data, destination within page

Branches to the destination specified by the destination operand if the relational data does not coincide with the contents of the register specified by the register specification operand.

The result of the EXCL-OR operation remains in the DREY.

[26] CNE (Call Subroutine If Not Equal)

CNE register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data does not coincide with the contents of the register specified by the register specification operand.

The result of the EXCL-OR operation remains in the DREY.

[27] CNEI (CNE Indirect)

CNEI register specification, relational data, subroutine name within page

Branches to the subroutine specified by the subroutine name operand if the relational data does not coincide with the contents of the register with the address contained in the register specified by the register specification operand.

The result of the EXCL-OR operation remains in the DREY.

MLI instruction

28 MLI (Machine Language Immediate)

MLI instruction code (bits 0 to 31)

Generates the instruction specified by the instruction code operand. Specify this instruction optionally if a code other than the codes specified in ASSEMBLER is to be assembled. Try to avoid using this instruction except special cases, such as remodeling ROMs, etc.

Parities are automatically generated.

Example: MLI X'4023516'

ASSEMBLER instructions

ORG (Origin)

ORG address value specification

Sets the location counter to the value specified by the address value specification operand.

Example: ORG X'300'

EQU (Equivalence)

Symbol definition EQU equivalent representation

Declares that the representation specified by the symbol definition operand matches the equivalent representation operand.

Define the equivalent representation before this instruction.

```
Example:  LABEL1     EQU    LABEL3
          R0         EQU    0
          ZERO       EQU    X'00'
          ALLONE     EQU    X'FF'
```

Do not use the representations used in ASSEMBLER: ALL1, ANY1, OR, AND, etc.

SPACE (Space): List control

SPACE line count specification

Leaves out space for the line count specified by the line count specification operand on the assemble list.

Example: SPACE 10

EJECT (Eject)

```
EJECT
```

Slews the top-of-page on the assemble list.

DS (Define Storage)

```
DS   address reservation specification
```

Leaves out free space for the number of addresses specified by the address reservation specification operand.

The address reservation specification operand conforms to the following:

```
nH : Reserves 2xn addresses
nC : Reserves n addresses
nX : Reserves n addresses
0B : 256 boundaries
nB : 2^n boundaries (1≤n≤16)
```

```
Example:  DS   4H
          DS   0B
```

Table 4.8 Bit patterns

Mnemonic	0 1 2	3 4	5	6	7 8 9 10 11 12 13	14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30	31
B	1 0 0	0 0	RV	C	Source register address	Branch address	P
BI		1 0				Branch address	
CALL		0 1				Subroutine address	
CALLI		1 1				Subroutine address	
BOC	1 0 1	0 0			Source register address	Branch address	P
BOCI		1 0				Branch address	
COC		0 1				Subroutine address	
COCI		1 1				Subroutine address	
TBB	1 1 0	0 0	RV	C	Source register address*	Mask data (Test bit data)	P
TBBI		1 0				Branch address	
TBC		0 1				Subroutine address	
TBCI		1 1					
BEQ	1 1 1	0 0	0	0	Source register address*	Mask data	P
BEQI		1 0				Branch address	
CEQ		0 1				Subroutine address	
CEQI		1 1					
BNE		0 0	1	0		Branch address	
BNEI		1 0					
CNE		0 1				Subroutine address	
CNEI		1 1					

Table 4.8 Bit patterns (continued)

Mnemonic	0 1	2 3	4 5	6 7 8 9 10 11 12 13	14 15 16 17 18 19 20 21	22	23	24 25 26 27 28 29 30	31
MV		0 0							
MV*		1 0					0		
MVHI	0 0	0 1	ALU	Source register address	Operational data	0		Destination address	P
MVHI*		1 1							
MVFI		0 1					1		
MVFI*									
LD		0 0							
LDI		0 1				1	0		P
LD*	0 0	1 0							
LDI*		1 1							
MF		0		Source register address		0		Destination address	
MF*		1				0			
MFD	0 1	0	ALU			1			P
MFD*		1				1			

* Each source register address marked an asterisk takes an indirectly specified register address for an indirectly specified instruction.

The shaded sections contain all '0'.

The dotted sections are replaced with indirect addresses.

Table 4.8 Bit patterns (continued)

Specification code

MV system	MF system	ALU
IMD, C	NA	0 0 0
DREG, D	NO	0 0 1
AND, A	AND, A	0 1 0
OR, O	OR, O	0 1 1
EOR, E	EOR, E	1 0 0
SREG, S	EN	1 0 1
PLS, P	PLS, P	1 1 0
MNS, M	MNS, M	1 1 1

Specification condition	RV C
ALL0	0 0
NCAR	0 1
ANY1	1 0
CAR	1 1

Specification condition	RV C
ALL0	0 0
ALL1	0 1
ANY1	1 0
ANY0	1 1

Format and cycle count

Table 4.9 Format and cycle count

Mnemonic operation code	Operands	Cycle count (1*)
B	Destination	2ϕ
CALL	Subroutine name	2ϕ
BI	Destination, register	3ϕ
CALLI	Subroutine name, register	3ϕ
BOC	Condition, destination	3ϕ
COC	Condition, subroutine name	3ϕ
BOCI	Condition, destination	3ϕ
COCI	Condition, subroutine name	3ϕ
TBB	Condition, register, test bit, destination within page	3ϕ
TBBI	"	5ϕ
TBC	Condition, register, test bit, subroutine name within page	3ϕ
TBCI	"	5ϕ
BEQ	Register, data, destination, within page	2ϕ
BEQI	"	4ϕ
BNE	"	2ϕ
BNEI	"	4ϕ
CEQ	Register, data, subroutine name within page	2ϕ
CEQI	"	4ϕ
CNE	"	2ϕ
CNEI	"	4ϕ
MV	Source register, operation, data, destination register	2ϕ
MV*	"	2ϕ
MVHI	"	4ϕ
MVHI*	"	4ϕ
MVFI	Source register, operation, data	4ϕ
MVFI*	"	4ϕ
STR STR*	Data, register	2ϕ

Table 4.9 Format and cycle count (continued)

Mnemonic operation code	Operands	Cycle count (1*)
MVR	Source register, destination register	2ϕ
MVR*		
LD	Source register, destination register	2ϕ
LD*	"	2ϕ
LDI	"	4ϕ
LDI*	"	4ϕ
MF	Source register, operation, destination register	4ϕ
MF*	"	4ϕ
MFD	"	4ϕ
MFD*	"	4ϕ

* The cycle counts take values for the EPROM mode, where ϕ is 208 ns.

4.5 Registers

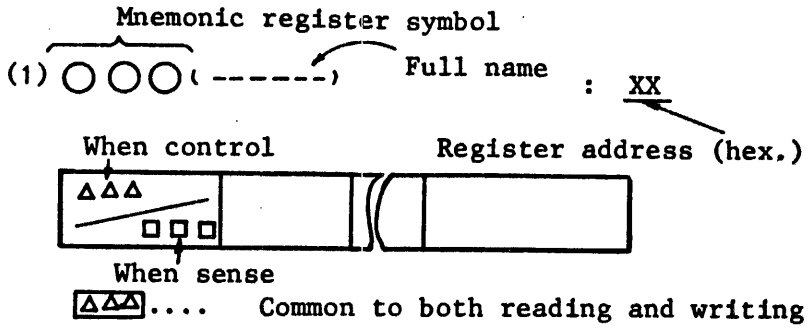
This section describes the registers to control the microprocessor. The microprocessor has seven bits of address lines RA0 to RA6 with which up to 128 bytes of registers are addressed.

The leading 64 bytes of the registers areas are known as the local storage register (LSR) area; the trailing 64 bytes are known as the external register (EXR) area.

The LSR area with register addresses X'00' to X'3F' consists of a RAM (9 bits x 64 bytes) whose each byte has its own parity bit. The EXR area with register addresses X'40' to X'7F', i.e. the control registers area for the interface control section, write/read control section, etc. have no parity bits.

Register addresses X'40' to X'4F' are unused by the FMTs.

The following shows the notation of these registers:



Abbreviations:

μP : Microprogram
FTP : Full Tacho-pulse signal
QTP : Quarter Tacho-pulse signal
MCY : Machine Cycle signal
VFO : Variable frequency oscillator; this chapter refers to the demodulation section.

4.5.1 LSR

(1) DVENQ0-DVENQ7 (Device Enquiry #0 to #7) : 00-07

These registers are employed as a enquiry memo or a condition memo about each MTU.

(2) SCMD (Initiated Command) : 08

The FMT stacks the initiated command and density select signals in this register before executing the command.

(3) SCANP (Scan Pointer) : 09

This register is used in the 'device scan routine" as a device address scanning pointer.

(4) DSB (Device Sense Byte) : 0A

The microprogram refers to this register when a new command is initiated or when a command operation is finished to generate status information for the Controller.

(5) LCMD (Last Command Code) : 0B

After a command operation, the microprogram stacks the last command code that is the internal command code.

(6) DVS0-DVS3, DVS8 (Device Sense byte 0-3, 8) : 0C-0F

When the FMT initiates a new command, the microprogram senses the current condition of the selected MTU. The sensed information is stacked in these registers.

(7) W0-W7 (Work Register0-7) : 10-17

These are work registers.

(8) MCYENT (MCY Entry parameter) : 18

The respective bits of this register serve as control flags when entering into a machine-cycle. These flags include the crease length increment flag, streaming mode flag, command classification flag, etc.

(10) CMDSEQ (Command Sequence) : 19

This register conforms to the MCYENT register.

- LIBGF : Long IBG Flag
- NOCK : No Check Flag
- LWR RW : LWR Read/Write Flag (LWR2 flag)
- XFROP : Diagnostic Transfer Operation Flag
- CMODE0-3: Internal Command Code

(11) SUB0, SUB1 (Subparameter 0, 1) : 1A, 1B

These serve as control parameters between subroutines in a MCY.

(12) Q0, Q1 : 1C, 1D

(13) Y0, Y1 : 1E, 1F

These four registers serve as work registers during a MCY.

(14) SB0-SB23 (Sense Byte Stacks 0-23) : 20-2B

These registers are set to the results of the command operation corresponding to the sense data bytes. An SNS command sends a sense byte on the basis of the contents of these registers.

(15) R0, R1 : 2C, 2D

These two registers serve as position counter.

(16) CMD (Command) : 2E

(17) DVA (Device Address) : 2F

These two registers contain the internal command code and device address that is currently being executed

(18) RJC (Reject Code Stacks) : 30

This register helps to generate a reject code to the Controller.

(19) RWE (Read Write Error) : 31

This register generates status informations about read/write command operation.

(20) EMPXP (Error Multi Plexer Parity) : 32

This register helps to set the EMX's Parity bits.

(21) RTRY (Retry Counter) : 33

This register is employed as the retry counter during retry operation.

(22) SNSCNT (Sense Counter) : 34

This register indicates how many SNS commands have been initiated. This counter is used as a HEX counter.

(23) Y2, Y3 : 35, 36

Spare register.

(24) LDVA (Last Device Address) : 37

The device address corresponding to the last command operation is stacked in this register.

(25) SDIA0-SDIA3 (Set Diagnostic Flag Byte 0-3) : 37-3B

These registers are set to four bytes of diagnostic flag bytes received by a SDIA command. Diagnostic operations are determined according to the contents of these flag bytes during a MCY.

(26) OFLCNT (Offline Control Register) : 3C
OFLCMD (Offline Command Register) : 3D
OFLDVA (Offline Device Address) : 3E
BCT (Offline Byte Counter) : 3F

This bit is set to '1' as follows:
During GCR or PE read/write operation when a parity error is detected in the read Out data but the error correction cannot be performed.
During NRZI write operation when exessive skew is detected.

4.5.2 EXR

(1) EMX0 (Error Multiplex 0) : 50

EMX0 - EXM3 provide additional error status information to the Controller. One of the four registers is multiplexed through the ERRMX bus as specified by the SLX0 - SLX2 lines. When the EMXPSL bit is '1', the microprocessor can access the parity bit.

0	1	2	3	4	5	6	7
DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0 / DTP

EMX0 indicates Pointer Track bits that are detected during a RD, RDB, WRT or LWR command operation. During PE or GCR operation, Pointer track is caused by the drop out, phase error, excessive skew or invalid code detection on a specific track. During NRZ operation, Pointer track is caused by the inability to detect correct data on a specific track. The assertion of bits DTP, **DT7, and DT6 indicate that the track in error (TIE) cannot be found.**

These bit are reset at the initiation of new command (except for a NOP, SNS and DMS command).

(2) EMX1 (Error Multiplex 1) : 51

0	1	2	3	4	5	6	7
WTMCK	UCE	PREC	MLTE	MISC	EDC	VEVCNG	DIAGL / CRC

(a) WTMCK (Write Tape Mark Check)

During a WTM command operation, this error detects that a tape mark cannot be written correctly in spite of seven retries.

(b) UCE (Uncorrectable Error)

This bit is set to '1' as follows:
During GCR or PE read/write operation when a parity error is detected in the read Out data but the error correction cannot be performed.
During NRZI write operation when exessive skew is detected.

(c) PREC (Partial Record)

When an IBG is detected before detecting a postamble during RD, RDB, WRT or LWR command operation, PREC bit is set to '1'.

(d) MLTE (Multiple Track Error)

This bit is set to '1' under the following conditions.
During GCR read operation, more than three DT7 to 0, P bits are set.
During PE read/write operation, more than two (DT7-O/P) bits are set.
During NRZI read/write operation, LRC error is detected.

(e) MISC (Miscellaneous Data Error)

This bit is set to '1' when any bit of DSB11 or Bit 3-O of DSB12 is set during read or write operation.

(f) EDC (End of Data Check)

This bit is set to '1' under the following conditions.
During GCR or PE read/write operation, the postamble is not detected correctly.
During NRZI read/write operation, the VRC error is detected.

(g) VELCG (Velocity Error)

This bit is set to '1' when MTU tape speed is outside acceptable limits during a write operation.
(±7% change)

(4) EMX3 (Error Multiplex 3)

0	1	2	3	4	5	6	7
EOT	BOT	NSP	FPE	BWD	HD	RDY	ONL/WRS

This register is set to indicate the selected MTU status.
Some and duplicated as separate interface lines.
Refer to (12) and (16).

(5) EMX4 : 54

(6) EMX5 : 55

(7) EMX6 : 56

(8) EMX7 : 57

(6)-(8) are reserved for future use.

(9) CMR (Command Register) : 58

0	1	2	3	4	5	6	7
$\overline{DS0}$	$\overline{DS1}$	$\overline{START}$	$\overline{CMDE}$	$\overline{CMD0}$	$\overline{CMD1}$	$\overline{CMD2}$	$\overline{CMD3}$

(a) DS0 (Density Select 0)

(b) DS1 (Density Select 1)

DS0 and DS1 are density select lines from the Controller and are used to direct the recording density of the selected MTU with the TUAD lines. The density select lines are only valid when the selected MTU is positioned at BOT and the intitiated command is WRT, WTM or ERS command. During all other positions of all other commands, the FMT ignores these lines and so the MTU's recording density will be unchanged.

(c) START (Initiate Command)

START is command a initiation line. If the FMT is in a BUSY state, assertion of start has no effect. If the FMT is not in a BUSY state, an INS trap will occur. The Controller must continue to assert the START signal until the FMT responds with a BUSY signal. In order to inform the FMT of receiving the BUSY response, the START signal may be reset before BUSY is reset.

(d) CMDE (Command Extend)

(e) CMD0-CMD3 (Command Select 0-3)

(d) and (e) are command select lines from the Controller that are **decoded in the FMT and cause one of *20 command operations.**

* This is a CMDE bit valid model. It is decided by the PCA jumpers. If the jumpers are not installed in the extend command mode, the CMDE line has no effect as a command select line. In this case, the command operation number is 16.

(10) ADR (MTU Address) : 59

0	1	2	3	4	5	6	7
TRAK	$\frac{R.BPE}{BUSPE}$	SLX2	SLX1	SLX0	TUAD2	TUAD1	TUAD0

(a) TRAK (Transfer Acknowledge)

TRAK signal is asserted by the Controller in response to TREQ signal during a data transfer operation.

(b) R.BPE/BUSPE (Reset Bus Out Parity Error/Data Bus Parity Error)

BUSPE is set when parity error is detected during a read/write command operation. While MCY is OFF, this bit is '0' if there is a parity error in the data bus.
This bit is reset by the R.BPE bit.
After a read/write operation, BUSPE bit '1' indicates that a Data Bus Out Parity Error has not been detected during a read/write operation.

(c) SLX2-SLXO (Select Multiplex 2-Select Mulitiplex O)

SLX2-SLXO are Select Multiplex lines that are decoded in the FMT to determine which of eight 9 bit registers is multiplexed to the Error Multiplex Bus.

These line are valid only when the FMT is not BUSY except select EMX2-Parity bit (TACH). Therefore, the microprogram is able to access the EMX registers during the FMT BUSY state.

(d) TUAD2-TUADO (MTU Address 2 - MTU Address O)

These three signal lines are MTU select lines from the Controller. The FMT decodes these bits to select one of the eight tape units which should execute the command operation. While in the FMT BUSY state, these lines are also ignored and have no effect on the status lines.

(11) FMTST (Formatter Status) : 5A

0	1	2	3	4	5	6	7
IDBST	TMS	OVRN	CRERR	DCK	REJECT	SSC	BUSY

FMT status lines are private signals for the Controller.

(a) IDBST (Identification Burst)

When the FMT is performing an ID burst or an ARA burst procedure in a read/write operation at BOT; IDBST bit is set '1'.
After the procedure is normally performed, IDBST bit is reset, and then the FMT starts the command operation. If an error condition is detected during the process, a retry operation is automatically performed.
In this case, the PCA jumpers are installed in a retry mode (FIDO bit is 'O'). Otherwise the command operation terminates abnormally with REJECT, OPINC, IDBST. If a RDB, BSP or BSF command is initiated with the tape positioned away from EOT, and the FMT detects BOT before a data block or a tape mark block appears; IDBST is also set.

(b) TMS (Tape Mark Status)

On a RD, RDB, BSP, FSP, BSF, FSF or WTM command, this signal is set to '1' to indicate that a tape mark block is detected or WTM command is performed correctly. In the case that the MTU has performed a disconnect Skip File Function, this bit is set by BLOCK in a CLR command after a BSF or FSF command operation executed by the MTU terminates. This bit is reset when any command (except SNS, NOP, and DMS) is initiated.

(c) OVRN (Over Run)

On a WRT, LWR, RD or RDB command, the OVRN bit is set to '1' to indicate that the command operation has not been normally completed because TRACK response to TREQ was too late. When OVRN is detected, the data transfer operation is terminated, but the position control for a block on the tape is not affected. When OVRN is detected during a RD or RDB command, data transfer is terminated and the FMT sets the ENDAT signal.

(d) CRERR (Corrected Error)

This bit is set in following conditions.
- One track error correction was performed during a GCR write operation or during a PE read operation.
- One or two track error corrections were performed during a GCR read operation.
- In NRZ operation, a reread to attempt a correction of the error block has been performed.

(e) DCK (Data Check)

The FMT sets the DCK bit in following cases to indicate that data just written or read out, is not, or may not be correct.

- When any of following errors occurs during WRT, LWR, RD or RDB command operation.

EMX0	DT7-0,	DTP can not be detected during NRZI operation
EMX1	bit P	CRC ERR
	bit 6	UCE
	bit 5	PREC
	bit 4	MLTE*
	bit 3	MISC
	bit 2	EDC
	bit 1	VELCNG

* Note ; MLTE error does not cause DCK during GCR read operation

(f) REJECT (Reject)

The FMT sets this bit to indicate that the command operation can not be executed and is incomplete when any of the following conditions is detected.

-Any command (except SNS, NOP, DMS and CLR) is issued to the MTU which is not in READY status.
- The condition of the selected MTU does no meet with the command.
- An undefined command is issued.
- During command operation, FMT detects the error condition to interrupt the operation. OPINC signal is also set.

(g) SSC (Slave Status Change)

The FMT sets SSC to indicate that one or more MTUs have gone ONLINE, gone OFFLINE, or have gone from a Not Ready to a Ready status.

During a command operation, the FMT does not set this bit even if the status of the selected MTU changes. The FMT sets this bit to inform the Controller of completion of a REW, DSE, FSF, or BSF command. This bit reset when any command (except a NOP, SNS and DMS command) is initiated to the MTU which has these status changes.

(h) BUSY (FMT Busy)

Busy signal is the response signal from the FMT for the command initiation.
The FMT holds this bit at least 20 microseconds until the command execution is completed.
This bit is also set during Power on diagnostic operation.
While the BUSY signal is asserted, START signal assertion has no effect. The FMT ignores command initiation in this case.

(12) TUST (MTU Status) : 58

0	1	2	3	4	5	6	7
HDENS	EPOS	EOTS	BOTS	WRTS	ONLS	NRZI	RDYS

MTU status lines are current MTU's status signals and are set/reset by FMT. When the microprocessor accesses the TUST register, it should be set DVAMPX2 - O by TULHT and TUSMP. (Refer to see Figure 4.14) Register write operation is performed only by the processer.

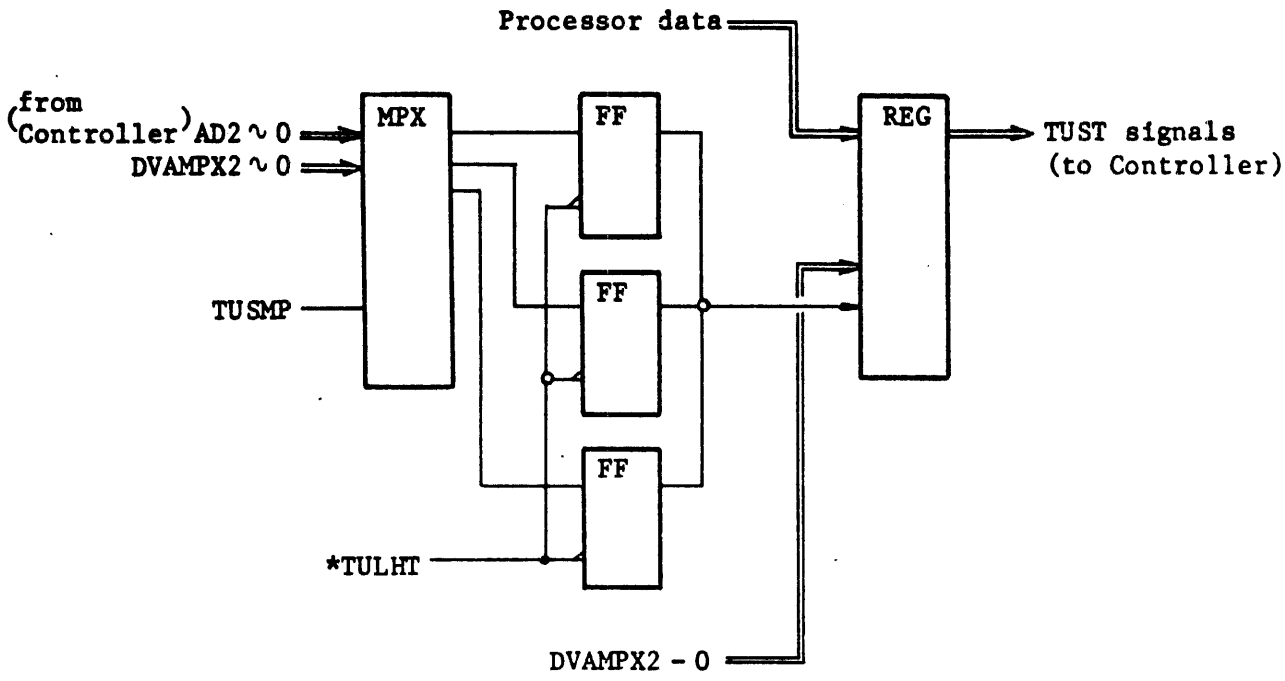


Figure 4.14 TUST register file

(a) HDENS (High Density Status)

The FMT informs the selected MTU's density mode with HDENS and NRZI signal lines.

Signal combinations are as Table 4.10.

Table 4.10 Density status

HDENS	NRZI	Density Mode
0	0	PE
0	1	NRZI
1	0	GCR
1	1	GCR

(b) FPOS (File Protect Status)

FPOS signal is set to indicate the selected MTU is in File Protect status. This conditions are as follows.

- A write enable ring is not set on the file reel.
- File Protect switch of the MTU operator panel is pushed.

(c) EOTS (End of Tape Status)

The FMT sets the EOTS bit when tape loaded on the selected MTU is positioned on or past the ECT marker which indicates that the tape is within the tape warning area (TWA).

(d) BOTS (Beginning of Tape Status)

The FMT sets the BOTS bit to indicate that the tape is loaded on the selected MTU and positioned at the BOT marker.

(e) WRTS (Write Status)

The WRTS bit is set when the selected MTU is in the write status and not in a file Protect status.

(f) ONLS (ONLINE Status)

The ONLS bit is set when the selected MTU has been set to ONLINE by the ONLINE switch on the MTU operator panel, when the tape is loaded in the columns, and the Tape Unit Check (TUC) does not occur. The MTC resets this bit when a UNL command is receveied from FMT, TUC occurs, or the RESET switch on the MTU operator panel is pressed.

(g) NRZI (NRZI Status)

Refer to HDENS.

(h) RDYS (Ready Status)

This bit is set when the selected MTU has a tape loaded, is in the online status, is not rewinding, is not Skip File or a DSE command operation.

(13) SIF (Status In Function) : 5C

0	1	2	3	4	5	6	7
TULHT	IRECV	ENDAT	TUSMP	EMXPSL	DVAMPX2	DVAMPX1	DVAMPX0

(a) TULHT

Refer to (12) TUST.

(b) IRECV (Expecting Data)

The FMT sets the RECV bit to decide data transfer direction of the bi-directional data bus (DATS7-DATA0,DATAP) when the transfer direction is from the Controller to the FMT.
This signal is set only on WRT, LWR, and SDIA command operation.
This signal is held until the next command is initiated.

(c) ENDAT (End of Data Pulse)

The FMT sets the ENDAT bit to indicate terminataion of the data transfer operation (RD or RDB) to the Controller.

- If the data buffer in the FMT is empty or STOP has been issued when the IBG behind the data block is detected, this signal is immediately pulsed about 1 microsecond.
- If the data buffer is not empty and STOP has not been issued at this time, the FMT waits for the termination of data transfer for 75 milliseconds. If the data transfer operation is completed wilthin this limit, this signal is immediately pulsed and the command operation is terminated.
- If the data transfer operation did not complete in this limit, the FMT immediately terminates the data handshake sequence with TREQ and TRaK and pulses this signal.

(d) TUSMP (MTU Status Register Control)

Refer to (12) TUST.

(e) EMXPSL (Error Multiplex Parity Bit Select)

Before the processor accesses a EMX parity bit, this bit is set to '1'. This bit gates the EMX parity control logic.

(f) DVAMPX 2 - DVAMPX 0 (Device Address Multiplex 2 - 0)

These three bits are employed to select TUST register address by the processor.
Refer to (12) TUST.

(14) BUS (Bus data) : 5D

0	1	2	3	4	5	6	7
BI0/A / VB00	BI1/*B / B01	BI2/SDI / B02	BI3 / B03	BI4 / B04	BI5 / B05	BI6 / B06	BI7 / B07

(a) BIO - B17 (Microprocessor Bus In Register)

This register is the data buffer register of microproccor BUS Out data (write data) and is employed to set the transfer buffer data or offline byte counts.

(b) A (Scan Clock A)

(c) *B (Scan Clock B)

(d) SDI (Scan Data In)

(b) - (d) are assigned to the LSI scan test when the SCAN bit is set to '1'.

(e) BOO - BO7 (Interface Bus Data O - 7)

These are interface Bus Out and Bus In Signals from/to the Controller.

(15) XCTL (Transfer Control) :5E

0	1	2	3	4	5	6	7
DXFI	DXFO	RECV	MTREQ / $\overline{\text{TREQ}}$	BLOCK	OPINC	MPRD	SCAN

(a) DXFI (Data Transfer In)

Set this bit to '1' for data transfer from the FMT to a Controller channel. This sets the data transfer circuit to enable in the required direction. This bit is reset by SERT signal.

(b) DXFO (Data Transfer Out)

Set this bit '1' to enable data transfer from the Controller to the FMT. This sets the data transfer circuit to enable in the required direction.

(c) RECV (BUS Direction Receive Mode)

Setting this to '1' inhibits the bi-directional data bus driver. This operation must be finished before RD, RDB or SDIA command operation is executed. This bit is reset by SERST or receipt of a new command.

(d) MTREQ (Microprogram TREQ)

This signal is a TREQ signal to the Controller from the microprogram. The TREQ signal for data transfer is generated on a DMS or SDIA command. This bit is also reset by SERT.

(e) TREQ (Transfer Request)

This is an ORed MTREQ and an internal TREQ signal that is generated in the data transfer control section.

(f) BLOCK (Block Status)

This bit is set to '1' when a data block or a TM (Tape Mark) is detected during an FSP and BSP command or a TM is detected during RD, RDB, FSF, or BSF command operation. When a data block is detected, the FMT sets BLOCK at the trailing edge timing (of the data block) as a pulse signal. The width is between 350ns and 1 microsecond. In the case of a TM, the FMT sets BLOCK and holds the TMS signal until after not BUSY state.

(g) OPINC (Operation Incomplete)

When the command is initiated but incomplete because of an error condition that interrupts the commnand operation, the FMT sets OPINC signal.

(h) MPRD (Microprogram Read)

This bit is set to '1' to store MP data to XFR buffer.

(i) SCAN (Scan Mode)

When this is set to '1', all the LSI FFs in the formatter circuit are set in serial scan mode. Scan operation is controlled by the CBI 0 - 2 bits. The SCAN function is used with diagnostic operations. This bit is reset by SERT signal.

(16) XSNS (Transfer Sense) 5F

0	1	2	3	4	5	6	7
16TH *ABPE	SETBC BLKE	DXFE	STOP	REWS	AROBR	BIBSY	SCMP

(a) 16TH (Byte Count 16 Times)

This bit causes the offline byte counter to act as an 8 bit counter.

(b) *ABPE (A or B Register Parity Error)

*ABPE is set to '0' if a parity error has been detected in A or B register during a data transfer operation from the FMT to the Controller. When this bit is a one, it indicates that a parity error was not detected in A or B register. This bit is reset by MCY.

(c) SETBC (Set Byte Counter)

Setting this bit '1' presets the contents of the BUS register in the upper 8 bits of the 12 bit byte counter. '1' are entered in the lower 4 bits. If the 16th bit is 'O', the B17 bit corresponds to 2^4 LSB. If the 16th bit is '1', the B17 bit corresponds to 2^0 LSB.
In the case the byte counter becomes an 8 bit counter and is capable of counting up to 255 bytes.
This function may be employed only if FMT is in offline status.

(d) BLKE (Block End)

BLKE is set when the data block end is detected correctly during a RD or RDB command operation.

(e) DXFE (Data Transfer End)

The DXFE signal indicates that any data transaction with the formatter circuit has finished. This bit is set by the STOP signal or by the offline byte counter's overflow-bit. DXFE is reset by MCY.

(f) STOP (Command terminate)

This signal is set by Controller to terminate the command operation in the response to TREQ or BLOCK as listed below:

- During a WRT or LWR command, in response to TREQ, the last data byte to be written in the data block has been placed on the bi-directional data bus.
- During a RD or RDB command, in response to TREQ, the formatter is to terminate the data transfer operation through the bi-directional data bus.
- During a BSP or FSP command, in response to BLOCK, the formatter is to terminate spacing over blocks.
  In this case, STOP assertion shall occur within 50 microseconds after the leading edge of BLOCK assertion and must have a 1 microsecond minimum duration.
  If spacing of only one block is desired, STOP may be asserted throughout the command operation.

In the first two situations, STOP replaces TRAK as the controller response to TREQ.
In response to STOP, the formatter terminates the command after completing the operation and resets BUSY.

(g) REWS (Rewinding Status)

REWS bit is set when the selected MTU is in the rewinding process. At this time the MTU status is in ONLINE and Not Ready.

(h) **AROBR (A Reg or B Reg)**

AROBR bit is the data transfer control signal and when this bit is '1', it indicates that the data transfer command is excuting. **This bit is reset by DXFE, DXFI or DXFO.**

(i) **BIBSY (Bus In Busy)**

BIBSY is '1' if data stored in the CHBI register does not move to the XFR buffer data. The MP should confirm that BIBSY=0 before setting the next data in CHBI register.

(j) **SCMP (Special Compose)**

Reserved for future.

(17) **MASK (Mask) : 60**

0	1	2	3	4	5	6	7
MASK0	MASK1	MASK2	MASK3	MASK4	MASK5	MASK6	MASK7

Bits containing '1' in this **register are masked without sending** write data if the mask bit is '1'. Also, if the ISPHE bit is set to '1', a PHE (Phase Error) signal is generated at each bit containing '1'. This register is reset by a HCLR signal.

(18) DACTL (Diagnostic control) : 61

0	1	2	3	4	5	6	7
DMW	DMR	IHPRE	IHPOS	INVLD	ALMSK	MASK	MASK8

(a) DMW (Diagnostic mode write)

This bit is set to '1' when data is written in the diagnostic mode.
This bit is reset by a HCLR signal.

Table 4.11 Function of DMW

Mode	When INVLD = '0'	When INVLD = '1'
6250	When a sub data group contains data '11xx', the entire sub data group is masked. (*1)	When a sub data group contains data '11xx', the sub data group data is replaced with invalid data. (*1)
1600/800	As long as tracks (bits) contain write data '1's in succession, the tracks (bits) are masked.	

*1 Invalid for a residual data group and a CRC data group in the 6250 mode.

(b) DMR (Diagnostic mode read)

This bit is set to '1' when data is read in the diagnostic mode.
This bit is reset by a HCLR signal.

Table 4.12 Functions of DMR

Mode	Function
6250	Check bytes and data are transferred to memory.
1600	Invalid.
800	CRC byte, LRC byte, and data are sent to memory.

(c) IHPRE (Inhibit preamble)

This bit is set to '1' if the preambles of all tracks are masked when data is written in the 6250 or 1600 RPI mode. For the 800 RPI mode, this bit is invalid.
This bit is reset by a HCLR signal.

(d) IHPOS (Inhibit postamble)

This bit is set to '1' when the postambles of all tracks are masked during a write operation in the 6250 or 1600 RPI mode.
This bit is invalid for the 800 RPI mode.
This bit is reset by a HCLR signal.

(e) INVLD (Invalid code)

This bit qualifies the details of DMW operation when data is written in the 6250 RPI diagnostic mode. It is valid only when DMW '1'. (See DMW.)
This bit is reset by a HCLR signal.

(f) ALMSK (All mask)

If this bit is set to '1', write data sent form the FMT to an MTU is masked.
Masking is effected at the same time as this bit is set to '1', without synchronizing with the write clock.
This bit is reset by a HCLR signal.

(g) MASK (Mask enable)

If this bit is set to '1', write data sent containing '1' bits in MASKO to MASK8 are masked.
Masking is effected as soon as this bit is set to '1', without synchronizing with the write clock.
This bit is reset by a HCLR signal.

(h) MASK8 (Mask 8)

This bit controls the masking of parity bits. See Item F(17).

(19) WTCTL (Write Control) : 62

0	1	2	3	4	5	6	7
WTN	IBW	WEC	ALlWT	WOK	-	$\overline{BFUL}$	R.BCY / BCY

(a) WTM (Write Tape Mark)

This bit is set to '1' to execute a Write Tape Mark operation in the 6250, 1600, and 800 RPI modes. The format counter sequence is set to the tape mark write sequence when this bit is set to '1'.

In the 6250 and 1600 RPI modes, the ALIWT, WOK and WEC bits must also be set along with this bit (bits 1, 3, & 4 must be masked).

The WEC bit is reset to '0' after the required length of data has been entered.
(Bit count is done by microprogram using R.BCY/BCY bits).

Processing in the 800 RPI mode is the same as in the 6250 and 1600 RPI modes except that the WEC bit is not set for Tape Mark Write Operation. (There is no need to count the data length with the microprogram).

WTM bit is reset by HCLR signal.

(b) IBW (IB Write)

This bit is set to '1' for a 6250/1600 ID Burst Write operation. The data trasmitted to the MTU is in 1600 RPI IB. Bits **WEC, WOK, and ALlWT must be set along with this bit to execute** an IB write processing. The WEC bit will be reset after entering the required length of data.

This bit is reset by HCLR signal.

(c) WEC (Write End Control)

In a Write operation, if this bit is set to '1', the format **counter stops at '13' and the processing stops till this bit is reset to '0'. This bit is set in operations like 6250/1600 RPI mode IB Write, tape mark write etc. and is used to control the data length.**
In such cases IB, ARA, ARAID and tape mark data is sent till the format counter reaches 13.

This bit is reset by HCLR signal.

(d) ALlWT (All 1 Write)

This bit is set to '1' to specify an all '1's Write operation format of 9042 fci/3200 fci/800 fci.
In the 625FO/1600 RPI mode, during IB Write and tape mark write operations, this bit must be set along with IBW and WTM bits, respectively. This bit is reset by HCLR.

The 3014 fci '1000' pattern is employed in the 6250 IB Write operation.

(e) WOK (Write OK)

This bit is set to '1' to enable the Write circuit and to start a Write operation. Modulation circuit, slip check circuit, noise check circuit and the format counter are started when this bit is set to '1'. WOK is reset when the format count reaches '15' (upon entering postamble or LRCC). This bit is reset if MCY is turned OFF.

(f) Bit 5 is a spare bit and is permanently set to 0.

(g) BFUL (Buffer Full)

This bit is set to '1' to indicate that the channel Buffer (64 bytes) on the data transfer control side is full. (This does not apply if the CBR (channel buffer read) bit is also set to '1'.) This bit is always '0' if CBR bit is set to '1'.

(h) R.BCY/BCY (Reset Byte Cycle/Byte Cycle)

Set this bit to '1' to reset the BCY signal. Now BCY signal will be set again to '1' after 8 bit cells in 6250 RPI mode, 4 bit cells in 1600 RPI mode, and 2 bit cells in the 800 RPI mode. The status of this signal will remain unchanged until this bit is set to '1'. The microprogram uses this bit to count and control write data length.

(20) RDCTL (Read Control) : 63

0	1	2	3	4	5	6	7
ROK	STPHK	VFOS	IHDXF	IHCOR	*HIG	ISPHE	SKWMG

(a) ROK (Read OK)

The Read circuit is set to Enable when this is set to '1'. This bit is reset by HCLR signal.

(b) STPHK (Stand-By Phase OK)

This bit is set to '1' to permit setting of PHOK signal. PHOK signal is reset immediately if this bit is set to '0'. Therefore, the PHOK signal may be set only if this bit has been set (by HBLK). The SLIPC and NOISE signals are set only while STPHK bits are ON.

* PHOK signal is reset after detection of postamble (EPOSA signal=1) in 6250/1600 RPI modes.
  However in 800 RPI mode, it is not reset till STPHK is reset.

STPHK bit is reset by HCLR signal.

(c) VFOS (VFO Start)

The loop filter capacitor of the VFO circuit discharges while this bit is OFF. This bit should be set to '0' for a certain period of time to completely discharge the capacitor. The VFO circuit is set to Enable status when this bit is set to '1'. The VFO circuit is controlled by WTCLK signal till the receipt of time sense signal.
Upon receipt of the time sense signal, VFO is reset for 1 peak pulse period to resynchronize with the data peak pulse. Then, it is controlled by the data. (ROK must be set to '1' to generate a time sense signal.)

(d) INDXF (Inhibit Data Transfer)

This bit is set to '1' to mask the data transfer request signal (DXRQ signal) from the Read/Write control section to data transfer control section; even if conditions for generating the DXRQ signal have been established in the Read/Write control section.

The DXRO signal may be generated only if this bit is set to '0'. '0'.

This bit is employed in 800 RPI read operation to mask TM, CRC, LRC byte transfer, and to start the control related to data transfer between the transfer buffer and read/write control section.
This bit is reset by HCLR signal.

(e) IHCOR (Inhibit Correction)

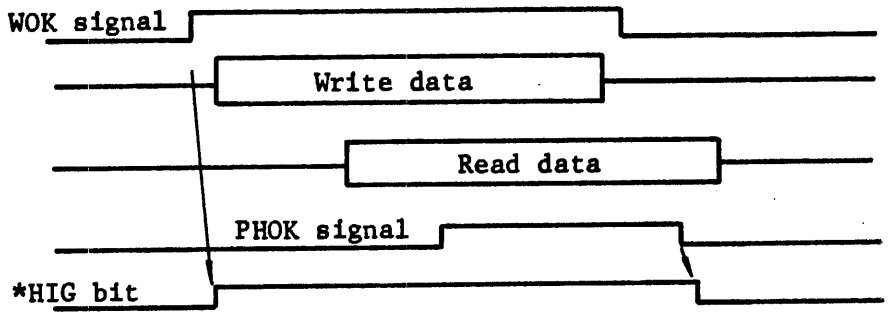
This bit is turned ON to inhibit error correction operation in the 6250/1600 RPI mode. This bit reset or set along with the ROK bit (it should be set during data byte detection operation). This bit is reset by HCLR signal.

(f) *HIG (Not High Gain)

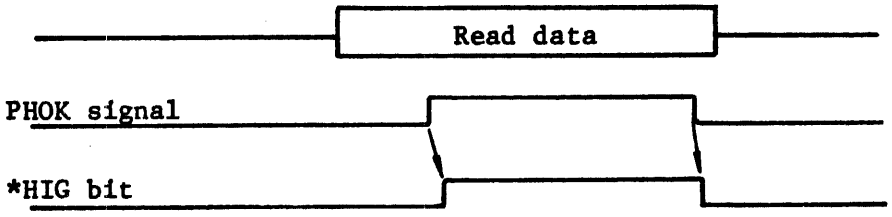
This bit is employed to alter the synchronization of the clock with data in a VFO circuit (increases the VFO loop gain). The VFO loop gain is high while this bit is set to '0'. This indicates that the synchronization capacity has increased. By setting this bit to '1' (low gain), VFO loop gain is set to normal level thus generating a very stable (low jitter) cell clock. This bit is reset by HCLR signal which sets it to a low gain status.

This bit must be set to '1' in 1600 RPI mode Read/Write operation.

In 6250 RPI mode, this bit should be controlled as shown in the following figure.



(1) Write operation



(2) Read operation

Figure 4.15 *HIG bit control in 6250 RPI mode

(g) ISPHE (Issue Phase Error)

This bit is used to generate a phase error. A phase error is (PHE) generated in the track corresponding to the MASK bit 0-9 which has been turned ON. (for further details, refer to Chapter 9).

This bit is reset by HCLR signal.

(h) SKWMG (Skew Marginal)

The skew check condition is set to marginal as soon as this bit is turned ON. This bit may be used only in 1600 mode.

This bit is reset by HCLR signal.

(21) MODE (Mode Select) : 64

0	1	2	3	4	5	6	7
MCY	BWD	WRS	ZRD	6250	1600	CMCY	CBR

(a) MCY (Machine cycle)

The MCY signal is turned ON to enable Read, Write, Device Control Circuits. In this stage these circuits may be controlled from microprogram while MCY signal is ON.

This bit is reset by HCLR signal.

(b) BWD (Backward)

This bit is turned 'ON' (set to 1) to set the FMT Read circuit to the Backward Mode. This bit is reset by the HCLR signal.

(c) WRS (Write Status)

This bit is turned ON (set to '1') to set the FMT R/W circuit to the Write Mode.

The following check conditions may be affected by this bit:
HNIS (Noise Block) check condition.

Postamble Read End (EPOSA) condition.
STRCK (Start Read Check) condition.
HTM (tape mark detection), skew error, error correction and other control conditions.
Read status is set when this bit is '0'.

This bit is reset by HCLR signal.

(d) ZRD (NRZ Read)

This bit is set to execute 800 RPI write, Read operation. When this bit is ON, the modulation circuit will generate a peak pulse as the data raises (if the BWD bit is '1') and a peak pulse as the input data falls (if the BWD bit is '0').
Both the pulses are generated as peak pulses.

This bit is reset by HCLR signal.

(e) 6250 (6250 mode)

This bit is set to '1' to execute a 6250 RPI Read/Write operation.
This bit is reset by HCLR signal.

(f) 1600 (1600 mode)

This bit is set to '1' to execute a Read/Write operation in the 1600 RPI mode.

This bit is reset by the HCLR signal.

(g) CMCY (Complete MCY)

This bit is not used. This bit is reset by HCLR signal.

(h) CBR (Transfer Buffer Read)

This bit is set to '1' to execute a transfer buffer Read operation. As soon as this bit is set to '1', the data transmit control section repeatedly transfers the transfer buffer data.
This bit is reset by HCLR signal.

(22) RDSNS (Read Format Sense) : 65

0	1	2	3	4	5	6	7
$\overline{\text{HNIS}}$	$\overline{\text{HBLK}}$	$\overline{\text{HTM}}$	$\overline{\text{WIND}}$	$\overline{\text{PHOK}}$	$\overline{\text{PREA}}$	$\overline{\text{POSA}}$	$\overline{\text{EPOSA}}$

(a) HNIS (Noise Block Detected)

If a noise pattern is detected (DNOIS=1) for a duration described in Table 4.17, this bit is set to '1'. This bit remains unchanged till ROK is turned OFF. This bit is '0' when ROK is OFF.

NIS set condition

Table 4.13 HNIS

Mode		Condition
6250	WRS	46±2 Bit cell period, continuous DNOIS
	RDS	22±2 "
1600	WRS	23±1 "
	RDS	11±1 "

This bit is not set in 800 RPI mode.

(b) HBLK (Block Detected)

If a block pattern (DBOB='1') is detected for a duration in excess of the specified bit cell period, this bit is set to '1'. This bit remains unchanged till it is reset (when ROK is turned OFF).
This bit is in Reset while ROK is OFF.

HBLK set condition

Table 4.14 HBLK

Mode		Condition
6250	WRS	25±1 Bit cell period, continuous DBOB
	RDS	"
1600	WRS	12.5 Bit cell period, continuous DBOB
	RDS	"

This bit is not set in 800 RPI mode.

(c) HTM (Tape Mark Block Detected)

If a tape mark block pattern (DTM='1') is detected continuously in excess of the specified bit cell period, this bit is set to '1'. This bit remains unchanged till reset when ROK is OFF.
This bit is reset while ROK is OFF.

HTM Setting condition

Table 4.15 HTM

Mode		Condition
6250	WRS	304±8 Bit cell period, continuous DTM
	RDS	42±2 "
1600	WRS	84±4 "
	RDS	21±1 "

This bit is not set in 800 RPI mode.

(d) WIND (Window)

In Write operation, this signal becomes '1' during a specified period (after a specified delay time has elapsed) from starting the Write operation. The leading edge of the block recorded in the corresponding write operation should be detected while this signal is '1'. The data bytes (800) or DBOB detected between the period from starting the Write Operataion will rise on this signal and will set NOISC signal to '1'.

The SLIPC will be set to '1' if the Wind Signal is set to '0' without detecting a data byte (800) or the DNOIS signal.

Figure 4.16 show the set and reset timing of the WIND signal.

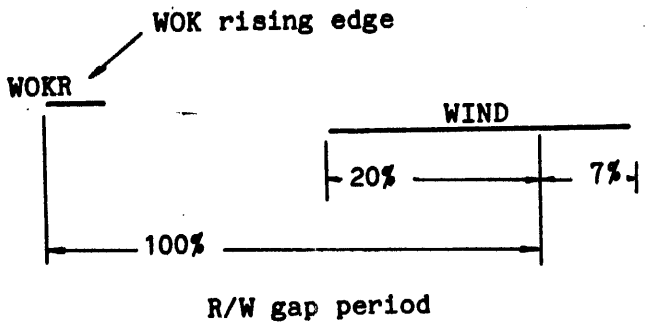


Figure 4.16 WIND signal

(e) PHOK (Phase OK)

This signal is sset while the HBLK signal rises when STPHK has been set. This signal is reset when the EPOSA signal rises (described later) or STPHK is reset. While this signal is ON, Write data error check and correction are available.

(f) PREA (Preamble Detected)

This signal is set to '1' upon detection of the first data byte in the 6250, 1600 RPI Read Circuit. The status of this signal remains unchanged till PHOK is reset. This bit is in reset status while PHOK is '0'.

(g) POSA (Postamble Detected)

This signal is set to '1' upon detection of the last data byte (Head of Postamble) in the 6250 and 1600 RPI Read Circuit. This bit remains unchanged till PHOK is reset. This bit remains in reset status while PHOK is '0'.

(h) EPOSA (End of Postamble)

This bit is set to '1' after the specified length of postamble is confirmed in the 6250 and 1600 RPI Read/Write operation. bit This bit is reset ('0') when DBIG rises.
This bit is in reset status while MCY is OFF.

EPOSA set condition

Table 4.16 EPOSA

Mode		Condition
6250	WRS	After POSA=1 and after a delay of 34±2 bit cells.
	RDS	" 6±2 "
1600	WRS	" 31±1 "
	RDS	" 21±1 "

(23) CRCST (CRC Status) : 66

0	1	2	3	4	5	6	7
$\overline{*MCRC}$	$\overline{*MCRCZ}$	$\overline{*EP=CR}$	$\overline{*B=C}$	$\overline{*B=C}$	$\overline{*MCRCC}$	$\overline{*A=B}$	$\overline{*XBIC}$

(a) *MCRC (Unmatch CRC)

This bit is set when the CRC pattern generated as a result of the Read Data (including CRC byte) operation is not normal (bits other than 2 and 4 of the CRC register are ON). This bit is employed in Read, Write, and Back Read operations in the 6250 and 800 RPI modes. This bit is ON ('1') when MCY is OFF.

(b) *MCRCZ (Unmatch CRC zero)

This bit is '1' when the CRC pattern generated as a result of the Read Data (including CRC byte) operation is not all '0's. This bit is employed in Read, Write, and Back Read operations in the 800 RPI mode. This bit is ON ('1') when MCY is OFF.

(c) *EP=CR (EP≠CR)

This bit is '1' if the pattern obtained, by reversing the pattern (except bits 2 and 4) generated by the Read data operation (including CRC byte), does not match with the error pattern register.
It is used for detecting errors along with the *MCRCZ signal in the 800 RPI mode.
This bit is set to '1' while MCY is OFF.

(d) ***B=D (CRCB≠CRCD)**

This bit is employed in Read, Write operations (excluding Back Read) in the 6250 mode. This bit is turned ON ('1') when the **Aux-CRC byte (CRCD) does not match with the CRCB pattern (CRC** generated from the transfer Buffer output). This bit is '1' while MCY is OFF.

(e) ***B=C (CRCB≠CRCC)**

This bit is employed in the 1600, 800 mode write operation. This bit is turned ON when the Write Data CRC pattern (obtained **from CRCB - XFR buffer output) does not match with the After Read data (excluding CRC byte) CRC pattern.**
This bit is set to '0' while MCY is OFF.

(f) ***MCRCC (Unmatch CRCC)**

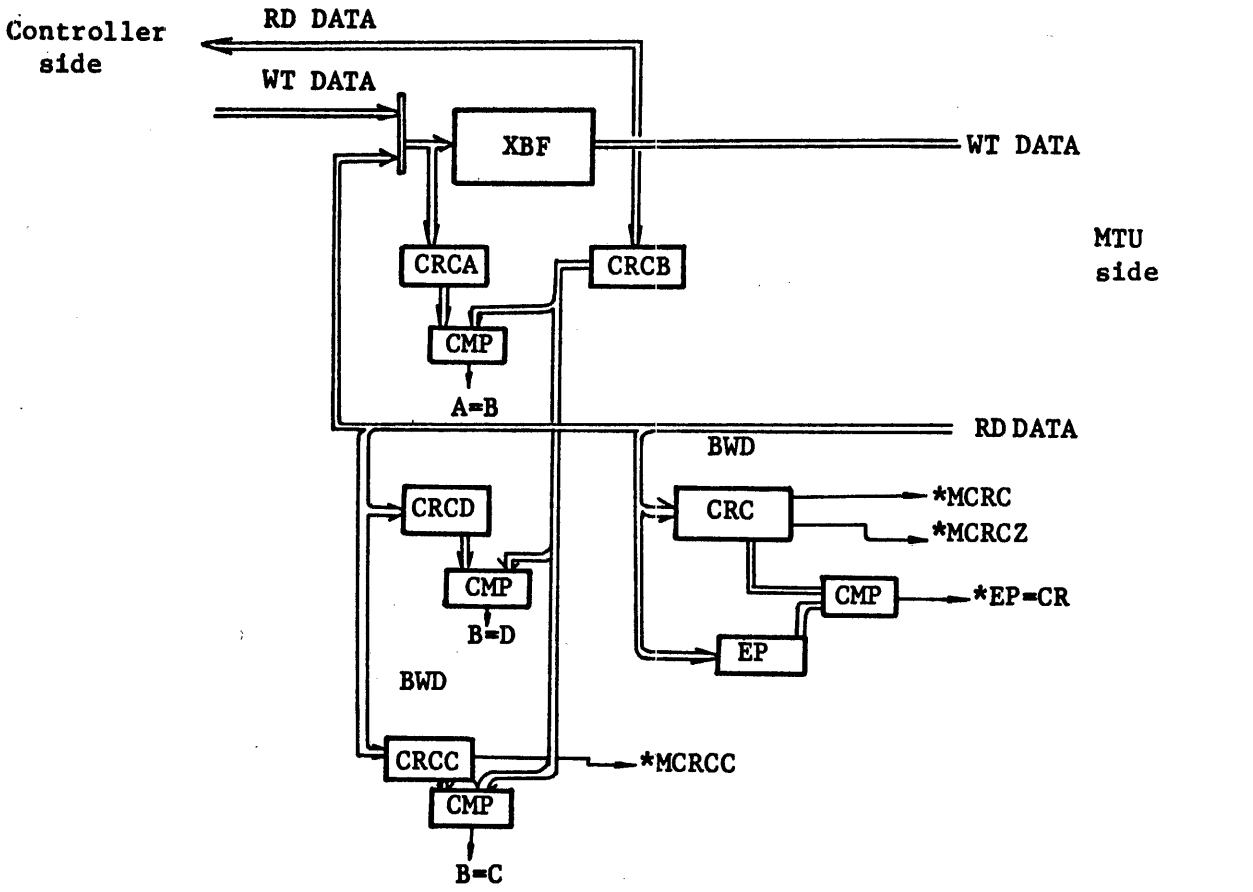
This bit is '1' when the CRC pattern obtained from Read Data (excluding CRC byte) is not normal.
This bit is employed in the Back Read processing in the 6250 mode. This bit is '1' while MCY is OFF.

(g) ***A=B (CRCA≠CRCB)**

This bit is '1' when the pattern generated from the input data to XFR buffer does not match with the CRC pattern generated from XFR register output data.
This bit is '0' while MCY is OFF.

(h) ***XBIC (*XBF Bus In Check)**

This bit is set when and illegal XFR Buffer Input data pattern is **detected. This bit is not reset until MCY is turned OFF.**
This bit is '0' while MCY is OFF.



B=C ... Invalid for BWD,
B=D ... Invalid except in 6250 FWD mode

Figure 4.17 CRC check

Table 4.17 CRC check

Mode	Input Byte Operation				
	CRCA	CRCB	CRC	CRCC	CRCD
6250	XBF Input data (Write→write data, Read→Read Data)	XBF Output data (Write→write data, Read→Read Data)	Data, Pad, Aux. CRC CRC Byte, 1 Byte	Data, Aux. CRC (BRD Only)	Aux. CRC (BRD not feasible)
1600				Data	
800			Data, CRC	Data	

(24) FMERR (Format Error) : 67

0	1	2	3	4	5	6	7
$\overline{*SRDC}$	$\overline{*EDCK}$	$\overline{*SLIPC}$	$\overline{*NOISC}$	$\overline{*WTBOC}$	$\overline{*WTVRC}$	$\overline{*OVRN}$	$\overline{*CMP}$

(a) *SRDC (Not Start Read Check)

This bit is turned ON, if the PREA signal (Start of Data Field Detection Signal) is not set within the specified delay time after PHOK.
This signal remains at '0' till MCY is OFF.
This bit is '1' while MCY is OFF. This bit ('1') means that Start Read Check error has not been detected in the Read Operation.

- SRDC Set condition -

Table 4.18 SRDC

Mode		Condition
6250	WRS	When PREA=0 upon specified delay of 128±8 bit cells after PHOK set.
	RDS	" 168±8 "
1600	WRS	" 52±4 "
	RDS	" 63±4 "

This bit is not available in 800 RPI mode.

(b) *EDCK (Not End Data Check)

This bit is turned ON if the DIBG signal cannot be detected within the specified time after EPOSA (see Table 4.19 for a specified time delay after premable). Once set to '0', it is not reset ('1') till MCY is OFF. It is '1' while MCY is OFF. This bit ('1') may be assumed that End Data Check Error has not occured in the Read Operation.

- EDC Condition -

Table 4.19 EDC

Mode		Condition
6250	WRS	When DIBC=0 upon delay of 88±8 bit cells after EPOSA=1
	RDS	" 248±8 "
1600	WRS	" 20±4 "
	RDS	" 36±4 "

Not available in 800 mode.

(c) *SLIPC (Not Slip Check)

This bit is set to '0' on detection of the data write (800 RPI) or DNOIS signal (6250/1600 RPI) while the WIND signal (section 14, d) is '1'. Once set to '0', the status of the this signal remains unchanged till MCY is turned OFF. This bit is '1' while MCY is '1'.

This bit, '1', may be assumed that no slip check error has in Write Operation.
This bit is '1' when MCY or STPHK is '0'.

(d) *NOISC (Not Noise Check)

This bit is set to '0' when data byte (800 RPI) or DBOB signal (6250/1600 RPI) is detected within the specified delay time after starting the Write Operation (WOK Rise). Once set to '0', the status of this signal remains unchanged till MCY is turned OFF. This bit is '1' when MCY is OFF.
This bit is '1' when MCY or STPHK signal is '0'.

(e) *WTBOC (Not Write Data Bus-Out Check)

This bit is set to '0' when a parity error is detected on the Write Bus Data to be entered to into the Write Circuit. This bit is not set to '0' when the WTCTL register ALIWT bit is set to '0'.

This bit remains in a '0' status while MCY is OFF. This bit is set to '1' by the HCLR signal. When this bit is '1', it is assumed that no parity error has occurred in the Write Curcuit during a Write Operation.

(f) *WTVRC (Not Write VRC)

This bit is set to '0' when a parity error is detected in the modulated Write Data. Once set to '0', the status of this byte remains unchanged till MCY is turned OFF. When this bit is '1' it is assumed that no parity error has occurred in the modulated data during a Write Operation.

(g) *OVRN (Not Over Run)

This bit is set to '0' when a overrun is detected in Read/Write Operation. Once set to '0', the status of this bit remains unchanged till MCY is turned OFF.
This bit is '0' when MCY is OFF.
When this bit is '1', it is assumed that a overrun error has not been detected in Read/Write Operation.

- OVRN Set Condition -

1. When DXFI=1 (Read Operation)

   - If XFR Buffer is Full (BFUL=1)

2. DXFO=1 (Write Operation)

   - If XFR Buffer became empty (CMP=1) before receipt of "transfer STOP" from the Controller interface during a Write Operation.

   - If the data left in the XFR buffer was less than 6 bytes before the "transfer STOP" was issued by the Controller interface in the 6250 mode Write operation.

(h) *CMP (Not Compare)

This bit is set to '0' if the XFR buffer Read-In count and the Read Out count do not match. This bit indicates the presence or absence of data in the XFR buffer. There is no data in the XFR buffer if this bit is '0' and there is data in the buffer if this bit is '1'. This bit is '0' when MCY is OFF.

(25) TSNS (Time Sense) : 68

0	1	2	3	4	5	6	7
$\overline{*TSNS0}$	$\overline{*TSNS1}$	$\overline{*TSNS2}$	$\overline{*TSNS3}$	$\overline{*TSNS4}$	$\overline{*TSNS5}$	$\overline{*TSNS6}$	$\overline{*TSNS7}$

Each of these bits is '0' when the peak pulse of the track is rising and falling, and the falling edgepulse of Read Data (corresponding to the bit) has been occuring with required period and specified cycles.
*TSNS0~7 are all '1' while MCY is OFF.
Peak pulse may only be generated if ROK=1.

(26) POINT (Pointer) : 69

0	1	2	3	4	5	6	7
*DET0	*DET1	*DET2	*DET3	*DET4	*DET5	*DET6	*DET7

DET ... Detect Error Track

This is an error track pointer used during a Read write operation in the 6250/1600 RPI mode. All the bits are '1' while MCY is OFF. DET 0-8 are set by a dead track (skew, persistent track, drop out) valid pointer or by the ECC group buffer pointer.

(27) BLFMT (Block Format) : 6A

0	1	2	3	4	5	6	7
*102CR	*DET8	*TSNS8	*DIBG	*DNOIS	*DBOB	*DRRA	*DTM

(a) *102CR (No 1 or 2 track correction)

This bit is set to '0' if 1 or 2 track error corrections have been executed in the 6250/1600 RPI read operation. Once set to '0', this bit remains in this status until MCY is OFF. This bit is '1' while MCY is OFF.

When the SCAN bit is '1', this bit represents a scan out signal of LSI chips related to a read operation.

(b) *DET8 (No Detect Error Track 8)

Refer to section (18), *DET 0-7

(c) *TSNS8 (NO TIME SENSE 8)

Refer to section (17), TNSS 0-7

(d) DBIG (NoT Detect IBG)

This bit is '1' when TSNS 0-8 represents an IBG pattern.

(e) *DNOIS (Not Detect Noise)

This bit is '0' when TSNS 0-8 represents the NOIS pattern.

(f) DBOB (Not Detect BOB)

This bit is '1' when TSNS 0-8 represents the BOB pattern.

(g) *DARA (Not Detect ARA)

This bit is '1' when TSNS 0-8 represents an ARA pattern.

(h) *DTM (Not Detect TM)

This bit is '0' when TSNS 0-8 represents a TM pattern. It is also '0' when the TM byte is detected in the 800 RPI mode.

$$DIBG = \overline{0 + 1 + 2 + 3 + 4 + 5 + 6 + 7 + 8}$$

$$DNOIS = A + B$$

$$A = (0.5.8)+(2.6.7)+(1.3.4)$$

$$B = (0+5+8).(2+6+7).(1+3+4)$$

$$DBOB = A.B$$

$$DTM = \overline{(1+3+4)}\{(0.5.8)(2.6.7)+PE.RDS[(0.5.8)+(2.6.7)] +GCR.RDS[(2.6.7)(0+5+8)+(0.5.8)(2+6+7)]\}$$

$$DARA = \overline{(0+8+5)}\{(1.3.4)(2.6.7)+RDS[(1.3.4)(2+6+7)+(1+3+4)(2.6.7)]\}$$

0-8, TSNS 0-8

(28) RDERR (Read Error) : 6B

0	1	2	3	4	5	6	7
*VRCE	*MLTE (*LRCE)	*SKWE	*DBCK	*DROE	PNMLT	*POSAE	"0"

(a) *VRCE (No VRC Error)

This bit is set to '0' when a Read Data Parity Error is detected and cannot be recovered by the pointer or ECC. Once this bit is set to '0' it remains in this status till MCY is turned OFF. This bit is '1' while MCY is OFF. This bit ('0') indicates an incorrectable VRC error. The error is not corrected if the above IHCOR bit has been set.

(b) *MLTE (*LRCE) (No Multiple Track Error of no LRC Error)

This bit is set ot '0' wnder the following conditions:

a) When more than 2 (DET 0-8) bits are set during the 6250/1600 RPI Write operation or the 1600 RPI read operation.
b) When more than three (DET 0-8) bits are set during the 6250 RPI read operation.
c) When an LRC error is detected during the 800 RPI mode write/read operation. Once set to '0', the status of this bit remains unchanged until MCY is turned OFF. This bit is set to '1' when more than one error track is detected or when an incorrectable LRC error is detected in the 800 RPI mode.

(c) *SKWE (No Skew Error)

This bit is set to '0' when multiple skew errors are detected in the read data. Once set to '0', this bit remains in this status until MCY is turned OFF.

When this bit is ON, it is assumed that a skew error has not occurred.

(d) *BDCK (No Deskewing Buffer Check)

This bit is set to '0' during 6250 RPI Write and forward Read operations if the Deskewing Buffer read out count is not all '0's when a resynchronous burst is detected. Once this bit is set to '0', it will remain in this status until MCY is turned OFF. This bit is therefore '1' when MCY is OFF. When this bit is ON, it is assumed that a skew buffer error has not occurred. This bit may not be used in the 1600/6250 RPI modes.

(e) *DROE (No Dropout Error)

This bit is set to '0' when one of the TSNS 0-8 signals is '0' while PHOK is '1' during a Write operation (WRS=1). Once this bit has been set to '0', it will remain in this status until MCY is turned OFF. This bit is therefore '1' while MCY is OFF. When this bit is '1', it is assumed that a drop out error has not been detected during a 6250/1600 RPI Write operation.

(f) PNMLT (Pointer Multiple)

This bit is set to '1' to indicate that more than two track pointers have been detected in a 1600/6250 RPI Read/Write Operations.

(g) *POSAE (No Postamble Error)

This bit is set to '0' when an illegal postamble byte (all '1':6250, all '0':1600) follows the postamble head (POSA=1). Once set to '0', it will remain in this status till MCY is turned OFF.
It is '1' when MCY is OFF.
When this bit is '1', is is assumed that a postamble error has not been detected.
This bit is not available in 800 RPI mode.

(29) ZETK (NRZ Error Track) : 6C

0	1	2	3	4	5	6	7
ETK0	ETK1	ETK2	ETK3	ETK4	ETK5	ETK6	ETK7

This register corrects errors in the 800 RPI mode Read Operation. The data corresponding to the bit set to '1' is reversed for read operation. This register is also reset by HCLR signal.

(30) ZCTL (NRZ Control) : 6D

0	1	2	3	4	5	6	7
SFCRC	$\overline{\text{LRC}}$	$\overline{\text{CRC}}$	$\overline{\text{HBLKN}}$	$\overline{\text{BLKED}}$	$\overline{\text{CRCHG}}$	$\overline{\text{CRCRG}}$	$\frac{\text{R.RDB}}{\text{RDB.S}}$

(a) SFCRC (Shift CRC Register)

Set this bit to '1' to cause a shift of the CRC register. One CRC data pattern is processed. This bit is reset ('0') after CRC register has been shifted. This bit is '0' while MCY is OFF. In the 800 RPI mode, to set this bit will cause a shift of CRC pattern register upon detecting a data byte.

(b) LRC (LRC Cycle)

This bit is set to '1' in FWD operation after the CRC byte has read. If a CRC byte has not been detected, this bit will be set to '1' after a period equivalent to 5.3 bit cells from the last data byte. Once set, the status of this bit remains unchanged till ROK is turned off.

In BWD operation, this bit is set to '1' as ROK rises. It is reset to '0' on detection of the first data byte (LRC byte). This bit is '0' while ROK is OFF.

This bit indicate that the current data byte is an LRC byte. This bit is valid only in 800 RPI mode.

(c) CRC (CRC Cycle)

During FWD mode processing, this bit is set to '1', if data bytes are not detected in the length of 2 bit cells after the last data byte. This bit remains in this status till 3.3 bit cells or until the detection of an LRC byte.
During BWD mode processing, this bit is set to '1', on detection of the LRC byte (first byte). This bit remains '1' untill the detection of data byte. If a data byte can't be detected within 5.3 bit cells from the LRC byte, this bit will reset to '0'. This bit is '0' while ROK is OFF. This bit indicates that the byte detected is a CRC byte. It is valid only in the 800 RPI mode.

(d) HBLKN (NRZ Block)

This bit is set to '1' on detection of 1 byte when WRS=1 and on detection of 8 bytes (including CRC and LRC bytes) when WRS=0. The byte remains in this status until MCY is turned OFF.
OFF.
This bit is therefore '0' while MCY is OFF.
This bit represents detecting of an 800RPI block.

(e) BLKED (NRZ Block End)

This bit is turned ON ('1') to indicate that the data or check byte was not detected during 10.7 bit cell period in 800 RPI mode processing. Once turned ON, the status of this bit remains unchanged till R.RBD is set to '1' or MCY is turned OFF.
This bit is therefore '0' while MCY is 'OFF'.

(f) CRCHG (CRC Horizon Gap)

In an 800 RPI mode read operation, this bit is turned ON ('1') when a data byte is not detected for a period of 5.3 bit cells after the last data byte. This bit ('1') indicates that a gap exceeding the permissible recording gap for a CRC byte has been detected. Therefore, the CRC byte is either not present, or the CRC byte is all '0' s when this bit is '1'. This bit is reset by turning ON THE R.RDB BIT ('1') or by turning OFF the MCY bit.

(g) CRCRG (CRC Recording Gap)

This bit is turned ON to indicate that a recording gap longer than 2 bit cells has been detected.
The CRC byte should be detected after this bit has been turned ON and before the CRC HG is set.

This bit is reset under the same conditions are that of CRCHG bit.

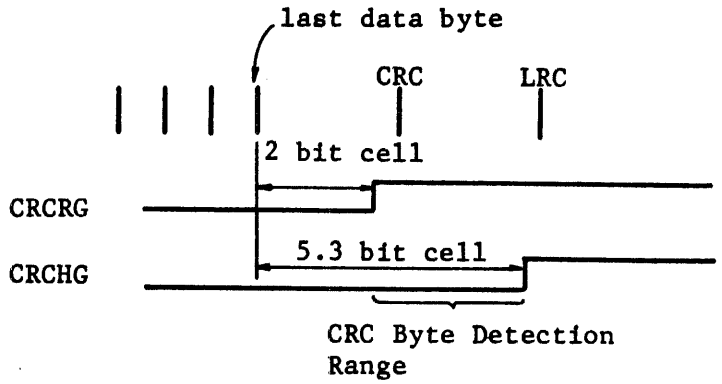


Figure 4.18 CRC & LRC

(h) R.RDB/RDB.S (Reset Read-Data-Byte/Read-Data-Byte Set)

In the 800 rpi mode, this bit is set to '1' by the sampling pulse. Once set, this bit may not be reset until the R.RDB bit is turned ON or until MCY is turned OFF. This bit is therefore '0' while MCY is OFF. When the RDB.S bit is set to '1', RDB.S is reset to '0'.
This bit may be used for counting read data byte in 800 RPI mode.

(31) ZMRG (NRZ Marginal Code) : 6E

0	1	2	3	4	5	6	7
$\overline{\text{*NVRCE}}$	ETK8	$\overline{\text{*NSKWE}}$	SDNT / $\overline{\text{*LRCE}}$	TM0	TM1	TM2	TM3

(a) *NVRCE (No NRZ-VRC-Error)

This bit indicates that a VRC error has not been detected in the 800 RPI Read Operation. **This bit is set to '0' as soon as a** VRC error has been detected. This bit may be reset to '0' by the SDRST bit.
This bit is also '1' while MCY is OFF.

(b) ETK8 (NRZ Error Track 8)

Conforms to the ETK bits (0-7) in section (21).

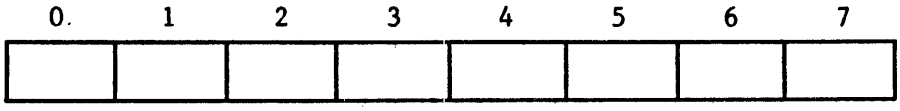
(c) *NSKWE (No NRZ Skew Error)

In the 800RPI write operation, this bit is set to '0' when multiple skew errors are detected in the data read from the Read Head.
This bit is not reset to '1' till the SDRST bit is turned ON or the MCY bit is turned OFF.

(d) SDRST/*LRCE (Sense Data Reset/Not LRC Error)

This bit, when '0', indicates that a parity error has been detected in LRC byte (LRC error).
*LRCE bit is reset ('1') when MCY is turned OFF.
Setting this bit to '1' by up (by SDRST='1'), the *NSKWE, *NWRCE bits will be reset to '1'.

(32) ZOP (NRZ OPTION) : 6F



This register indicates whether the 800 RPI optional PCA circuit (1A01: 512189U) has been installed.
One of the bits in this register is '1' when the above optional PCA is installed, If all the bits in this register are '0', registers 6C-6E are not available.

(33) TMCTL (Timer control) : 70

0	1	2	3	4	5	6	7
TPCNTM	INTVLM	C.QTP	LWRFMT	R.CNT/ S.CNT	R.CTU/ CNTU	R.FTP/ DFTP	R.OTP/ DQTP

(a) TPCNTM, INTVLM, C.QTP (Tacho pulse count mode, Interval count mode, count QTP)

These registers specify timer count modes.

Table 4.20 Timer control modes

TPCNTM	INTVLM	C.QTP	Count mode
0	0	x	1.66 μsec clock timer
1	0	0	FTP counter
1	0	1	QTP counter
x	1	0	FTP period counter (*1)
x	1	1	QTP period counter (*1)

*1 The following shows the count clock of the FTP/QTP period counter.

Table 4.21 FTP/QTP count

Speed (IPS)	Count clock (ns)	Normal FTP period (μs)
200	208	47.1
125	"	75.4
75	"	125.66
50	"	188

These registers are reset by the SERST signals or by the microprogram.

(b) LWRFMT (LOOP WRITE TO READ in Formatter)

If this bit is set on, read signals are looped within the FMT, during a LWR command operation. This bit is reset by a microprogram or a SERT signal.

(c) R.CNT/S.CNT (Reset counter/Start counter)

These counters control the start/stop cycle of the timer. If data is set in the upper area of the timer, then the S.CNT bit is set to '1' so that the timer can start to count. If the timer is then generating a no overflow output (T.TMR='0'), then counting starts. Counting continues until an overflow results. However, even before an overflow, if only this bit is set to '1' (R.CNT='1'), then the S.CNT bit is reset to stop counting. A SERST signal also resets to S.CNT bit.

(d) R.CTRU/CTRU (Reset counter upper entry mode/Counter upper entry mode)

A CTRU signal is set on when data is read/written from/to the timer in the upper R/W mode. If the CTRU signal is reset, the lower R/W mode results.

If this bit is set to '1' (R.CTRU='1'), the CTRU signal is reset.

A SERST signal also resets the CTRU signal. If data is read/written from/into the upper area of the timer (data is read/written at address '71' when CTRU='0'). Then a CTRU signal is set to '1'. Thus a microprogram can read/write data continuously from/to the timer in ascending order.

(e) R.FTP/DFTP

If an FTP is detected after the MCY is set to on, the DFTP bit is set on. The DFTP bit is reset if this bit is set to '1' (R.FTP='1') or the MCY signal is reset.

(f) R.QTP/DQTP

If a QTP is detected after a MCY signal is set to on, the DQTP bit is set to '1'. If this bit is set to '1' (R.QTP='1') or the MCY signal is reset, then the DQTP bit is reset.

(g) DVA0 to DVA2 (Device addresses 0 to 2)

These bits indicate a device address (absolute address) to be selected. They remain unchanged until they are set once more by the microprogram or reset to '000' by a signal.

(34) Time (Timer data) : 71

This register contains data to be read/written from/into the timer. The CTRU signal controls switching between the upper and lower R/W modes.

The timer starts to count (S.CNT='1') when data is set on the upper area. Counting continues until a count overflow (carry output) results and T.TMR becomes '1'.

0	1	2	3	4	5	6	7
CT0 (CT8)	CT1 (CT9)	CT2 (CTA)	CT3 (CTB)	CT4 (CTC)	CT5 (CTD)	CT6 (CTE)	CT7 (CTF)

Counters in parentheses apply to the lower R/W mode.

Data is set on the read register once at the timing of QTP or FTP (only while the timer is operating in the QTP or FTP period counter mode: MCT1='1') and is read later.

Figure 4.19 shows the timer circuit (16-bit counter).

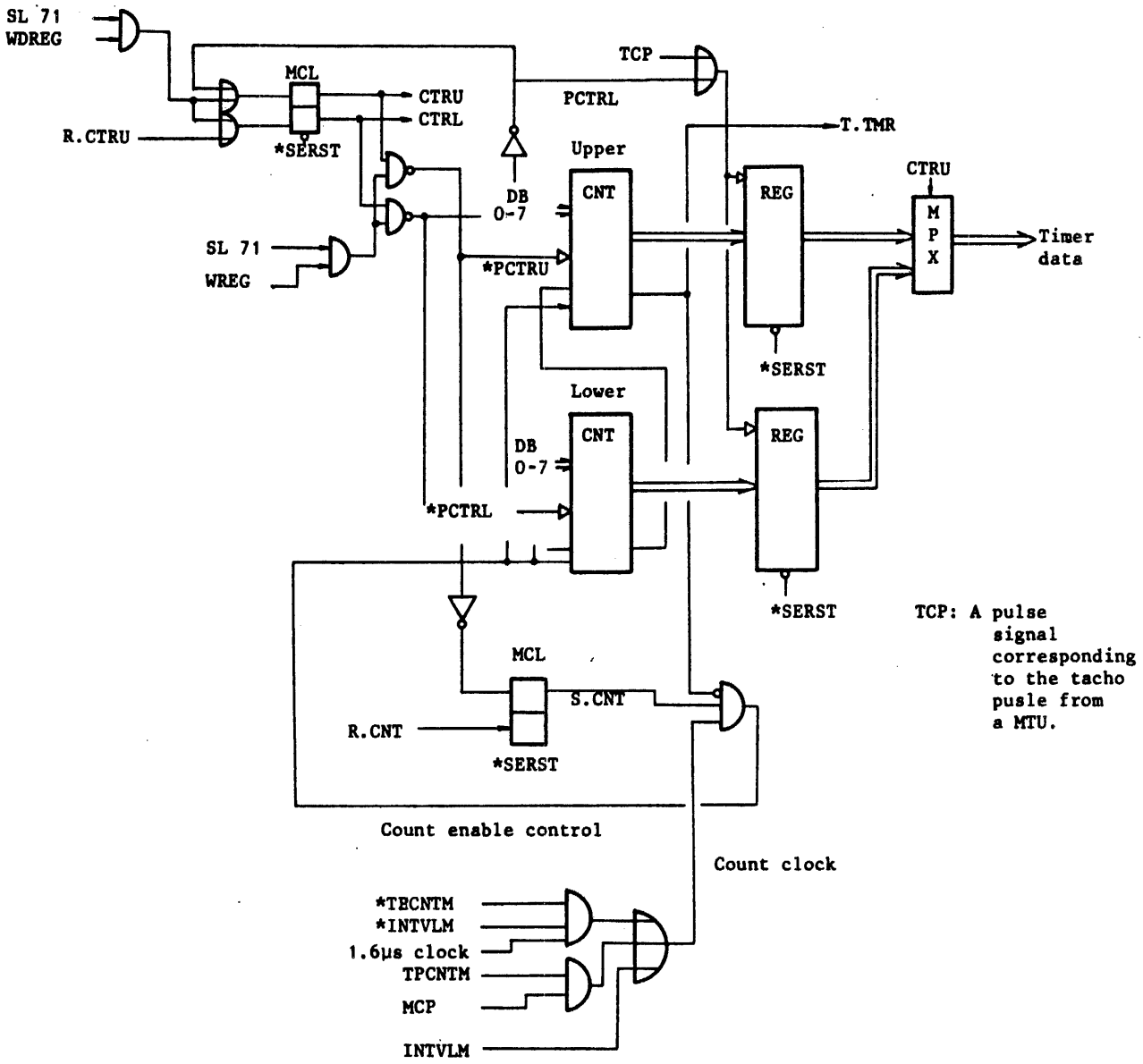


Figure 4.19 Timer circuit

(35) DVSEL (Device select) : 72

0	1	2	3	4	5	6	7
$\overline{\text{TAGI}}$	$\overline{\text{C.CRY}}$	$\overline{\text{*DVENB}}$ / XCAL	SLTAG	$\overline{\text{DVBSY}}$	DVA0	DVA1	DVA2

(a) TAGI (Tag-in)

A Tag In signal from a selected MTU.

(b) C.CRY (Reposition Counter's Carry)

C.CRY is changed to '1' on detection of carry in the above mentioned counter. It remains in this state till MCY is turned OFF or R.CRY is set. C.CRY is therefore '0' while MCY is OFF.

(c) *DVENB (Not Device Enable)

This bit is '0' while the Device Enable Switch on the operator panel (for the MTU selected by the DVA0 to DVA2 bits of the SLTAG) is set to 'Enable'. This bit is always set to '0' if the operator panel in not equipped with an ENABLE switch.

(d) XCAL (X-call)

The XCAL signal, showing that the device crosscall feature is enabled, is '1' when while the distribution PCA is operating in the dual FMT mode (chen DGBMU is installed).

(e) SLTAG (Select tag)

This bit is set to '1' when the MTU with the device address indicated by DVA0 to DVA2 is selected. If DVBSY='0', the corresponding device remains selected by the corresponding until the SLTAG bit is set to '0'. The SLTAG bit is reset by a signal.

(f) DVBSY (Device busy)

When this bit is '1', a device cannot be selected because the device is being selected by the other FMT or has been reserved.

(36) TPCNT (Tacho pulse Counter) : 73

0	1	2	3	4	5	6	7
$\overline{\text{RCCT0}}$	$\overline{\text{RCT1}}$	$\overline{\text{RCT22}}$	S.UCT / $\overline{\text{RCT3}}$	S.DCT / $\overline{\text{RCT4}}$	CTSTP / $\overline{\text{RCT5}}$	R.RCT / $\overline{\text{RCT6}}$	R.CRY / $\overline{\text{RCT7}}$

(a) RCT0 - RCT7 (Reposition counter)

This register represents position check FTP counter status (RCT 0-7).

(b) S.UCT (Start Up Count)

When this bit is set to '1', the Position Check FTP counter starts counting in the UP count mode.

(c) S.DCT (Start Down Count)

When this bit is set to '1', the Position Check FTP counter starts counting in the Down count mode.

(d) CTSTP (Counter Stop)

The Position Check FTP counter is stopped when CTSTP is set to '1'.

(e) R.RCT (Reset Reposition Counter)

R.RCT is set to '1' to clear the Position Check FTP counter to all '0's.

(37) DVTAG (Device tag) : 74

0	1	2	3	4	5	6	7
GO	TAGVL	STS	CTL	DBMPX	TSP0	TSP1	VHSP

(a) GO (Device go)

This bit conveys a GO signal to a selected device.
This bit is reset while MCY is off.

(b) TAGVL (Tag valid)

This bit is valid only while DBMPX='0'. While DBMPX='0', a TAGVL signal is sent as a strobe signal to a device. The contents of DB00 to DB07 are strobed on the device side (at the rise of the TAGVL signal).
This bit is reset while MCY is off.

(c) STS (Status)

This bit conveys a Status Tag signal to a selected device. The FMT detects and sets the status of the selected device with this signal: set DBMPX to '0'; set DB00 to DB07 to status information; set the TAGVL bit to on/off.
The TAG0 bit is reset while MCY is off.

(d) CTL (Control)

This bit conveys a Control Tag signal to a selected device. The MTC detects control information and directs operations: set DBMPX to '0'; set control information to DB00 to DB07; set the TAGVL bit to on/off. The TAG1 bit is reset while MCY is off.

(e) DBMPX (Device bus multiplex)

This bit assigns any of the device-bus-outs 0 to 7 to a selected device and switches. The Write Clock signals.

Table 4.22 Write pulse

Device-Bus-out		WCL	
DBMPX='1'	WMDT0-7	WTPL	When writing
DBMPX='0'	DB00-7	TAGVL	When reading Interfacing with MTUs

This bit is reset by a SERT signal.

(f) TSP0, 1 (Tape speed codes 0 and 1)

These two bits specify a tape speed. These bits are cleared by a SERST signal (TSP0, 1='00').

Table 4.23 TSP code

TSP0	TSP1	Speed
0	0	50 IPS
0	1	75 IPS
1	0	125 IPS
1	1	200 IPS

These bits switch the timing of the read/write circuit and the FMT clocking.

(g) VHSP (VF0 high speed)

The VF0 can accommodate itself to two levels of speed. If this bit is set to '1', the VF0 operates at the faster of the two.
This bit is reset by a SER signal.

(38) DVBO (Device bus-out) : 75

0	1	2	3	4	5	6	7
DBO0	DBO1	DBO2	DBO3	DBO4	DBO5	DBO6	DBO7

This register conveys a Bus Out signal to a selected device. Information set on DBO0 to DBO7 is defined by three tags signals (GO, STS, and CTL). If the GO tag is set to '1', then DBO0 to DBO7 contain status specification information. If CTL is set to '1', then DBO0 to DBO7 contain control operation specification information.

If the three tags are all '0', then the sense byte of an MTU for each of the DBO0 to DBO7 singals is requested to be sent. (The sense information is obtained on the device bus-in.)

Information set on this register is sent to the device only when DBMPX='0'. This register is reset by an SER signal.

(39) DVBI (Device bus-in) : 76

0	1	2	3	4	5	6	7
$\overline{DBI0}$	$\overline{DBI1}$	$\overline{DBI2}$	$\overline{DBI3}$	$\overline{DBI4}$	$\overline{DBI5}$	$\overline{DBI6}$	$\overline{DBI7}$

Three tags (GO, STS, and CTL) define bus-in information. If the GO tag is set to '1' DBI 0 to 7 and P contains read data.

If CTL is set to '1', DBIO to 7 contains MTU control detection information.

If the three tags are all '0's the sense byte of an MTU corresponding to DBOO to 7 is sent to DBIO to 7.

(40) DVSNS (Device sense) : 77

0	1	2	3	4	5	6	7
$\overline{GAPC}$	$\overline{CPFWD}$	MPXBO	M.TCS	$\overline{VLOK}$	$\frac{R.VLC}{VLCHG}$	TCSG	$\overline{TCSP}$

(a) GAPC (Gap control)

This bit sends a GAPC signal to the selected device if the GO tag is set to '1' during a read/write operation or when an IBG is passed over from the end of a block. This bit is always '0' while a SERST signal is set on.

(b) CPFWD (Capstan forward)

This bit is set to when the capstan motor of the selected device is rotating forwards (or the CPA is delayed 90 degrees). This bit is reset while MCY is off.

(c) MPXBO (Multiplex bus-out)

If this bit is set to '1', the contents of DBOO to 3 (upper area) are read into DBO4 to 7 (lower area). When the contents of the upper four bits of byte data are shifted to the lower four bits, this bit is set on. This bit is reset while MCY is off.

(d) M.TCS (Mask tacho-pulse-stop trap)

This bit masks the occurrence of a trap due to a TCSP signal (Tacho Stop) that occurs when the period of arrival of tacho pulses from a MTU has increased. The trap is enabled while this bit is '1'. This bit is reset while MCY is off.

(e) VLOK (Velocity OK)

This bit is set to '1' when the period of arrival of FTPs from a selected device falls within a specified range. This bit is reset while MCY is off.

(f) R.VLC (CLCHG) (Reset velocity change/Velocity change)

This bit is set to '1' when the period of arrival of FTPs from a selected MTU during a write operation of the FMT falls outside a specified range. This bit remains unchanged until MCY is off or it is reset by setting it to '1' (R.VLC='1').

(g) TCSG (Tacho-stop gate)

This bit gates the entry of the TCSP signal. If this bit is set to '1', then no TCSP signal is set even if the period of arrival of FTPs from a selected device increases. This is reset while MCY is off.

(h) TCSP (Tacho-stop)

The TCSP bit becomes '1' when the FTP period counter within the MTC overflows and the TCSG bit is set to '1' (as a result of an increase of the period of arrival of FTPs from a selected device).

The TCSP signal remains unchanged until it is reset by MCY OFF.

The following shows overflow times.

Table 4.24 TCSP overflow time

Tape speed	Nominal period	TCSP detection time
200 IPS	47.1 μs (100%)	208μs x 1 x (2^{12}-1) = 851μs (5.5%)
125 IPS	75.4 μs (100%)	208μs x 2 x (2^{12}-1) = 1703μs (4.4%)
75 IPS	125.7 μs (100%)	208μs x 3 x (2^{12}-1) = 2555μs (4.9%)
50 IPS	188 μs (100%)	208μs x 4 x (2^{12}-1) = 3406μs (5.5%)

(41) DVRSV (Device reserve) : 78

0	1	2	3	4	5	6	7
RSV0	RSV1	RSV2	RSV3	RSV4	RSV5	RSV6	RSV7

This register controls the reserve/release status of devices. All bits of this register are reset when powering on or switching the ONL/OFL switch on the field testers.

While a device is occupied by one FMT, the RSV bit for the device must be set to on. In this case, the other FMT cannot use them. device (DVBSY='1').
The RSV bits remain unchanged until a microprogram resets them.
All RSV bits are reset when powering on or switching the ONL/OFL switch on the field tester.

Each RSV bit is normally set to on while the corresponding device is successfully selected (SLTAG='1').

(42) UQID (Function ID) : 79

0	1	2	3	4	5	6	7
$\overline{\text{FID0}}$	$\overline{\text{FID1}}$	$\overline{\text{FID2}}$	$\overline{\text{FID3}}$	$\overline{\text{FID4}}$	$\overline{\text{FID5}}$	$\overline{\text{FID6}}$	$\overline{\text{FID7}}$

This register indicates the function selected for

FID0 = '1': IB-Retry is executed during write operation.

'0': No IB-Retry during write operation.

Specifies the retry function in case of an IB write error.

FIDI-7: Reserved.

(43) TRAP (Trap Control) : 7C

0	1	2	3	4	5	6	7
/T.INT	/T.TMR	/T.INS	/T.PER	M.INT	M.TMR	M.INS	TMSK

(a) T.INT (Trap by Device Interruption)

This is a DVINT signal from the selected MTU.

(b) T.TMR (Trap by Timer Carry)

This bit represents an FMT timer overflow.
The Timer stops counting while this bit is ON.

(c) T.INS (Trap by Initial Selection)

This bit is set to '1' when the FMT is in an status and the controller is requeting an intitial selection sequence.

This bit is reset when the BUSY bit is ON and the START bit has been reset.

(d) T.PER (Trap by Processor Error)

This bit is set to '1' when the PERR signal has becomes '1' except when the FMT is in the ROSF mode (ROS function).

(e) M.INT (Device Trap Mask)

When this bit is set to '1', a device trap is enabled.
A device trap can occur when the above T.INT='1' and M.INT='1'. This bit is reset by SERST signal.

(f) M.TMR (Timer Trap Mask)

This bit is set to '1' to enable a timer overflow trap.
This trap can occur when the above T.TMR='1' and M.TMR='1'.
This bit is reset by the SERST signal.

(g) M.INS (INS Trap Mask)

This bit is set to '1' to enable a INS trap.
This trap can occur when the above T.INS is '1', and M.INS='1'.
This bit is reset by SERST signal.

(h) TMSK (Trap Mask)

This bit, when '1', enables all the microprocessor traps. As soon as a trap is accepted, TMSK signal is reset ('0').

(44) MPERR (Microprocessor Error) : 7D

0	1	2	3	4	5	6	7
M.RER / $\overline{\text{RENB}}$	R.PER / $\overline{\text{OFL}}$	$\overline{\text{CSPE}}$	$\overline{\text{REGE}}$	$\overline{\text{DIAG}}$	$\overline{\text{VFOH}}$	$\overline{\text{VFOM}}$	$\overline{\text{VFOL}}$

(a) M.RER (Mask Register Error)/RENB (Register Enable)

The RENB bit is reset ('0') by the reset signal when the power supply is turned ON. Parity check is invalid before microprocessor initializes LSR.

MP initializes all LSRs when power on. After this, the M.RER bit is set to '1' to validate the above parity check. Once set, RENB is '1', and may not be reset unless power supply is turned off (MP cannot reset RENB).

(b) R.PER (Reset Processor Error)/OFL ($\overline{\text{Offline}}$)

When the R.PER bit is set to '1', the PERR signal is reset simultaneously. The ALU carry register is also cleared. PERR is caused by an CS parity error or an LSR read parity error, and us reset by the SERST signal. OFL signal is '1' when the Field Tester ONL/OFL.

(c) CSPE (CS Parity Error)

This bit indicates a parity error has taken place during a CS read. PERR is generated if this bit '1'. This bit is reset either by the SERST signal or by the R.PER bit CS.

(d) REGE (Register Error)

This bit indicates that parity error is detected when the microprogram access LSR data (after the M.RER bit has been set to '1').
This generates PERR interruption.
The reset condition of this bit is the same as that of CSPE.

(e) DIAG (OFF Line Diagnostic test)

(f) VFOH/VFOM/VFOL

These three bits select the VFO processing mode.

Table 4.25 VFO available table

VFOH	VFOM	VFOL	Available Speed Mode			
			200	125	75	50
0	0	0				0
0	0	1			0	0
0	1	0		0		0
0	1	1		0	0	
1	0	0	0			0
1	0	1	0		0	
1	1	0	0	0		
1	1	1	-	-	-	-

0...available

(45) CEA (CE Resister A) : 7E

0	1	2	3	4	5	6	7
PEVN	ERRF	EPC5X	TMTS FLAG	-	-	-	-

(a) PEVN (Parity Even)

When this bit is set to '1', an LSR write data parity bit is generated (Even parity). The FMT will report ROMPS status to Controller.

(b) ERRF (Error Flag)

Not used.

(c) EPC5X (Enable Parity Check 5X)

Not used.

(d) TMTS FLAG (Test MTS Flag)

While Test MTS operation of the SDIA command is running, this bit is set to '1'.

This bit is reset by SERST signal.

(e) bit 4 - bit 7

Not used.

0	1	2	3	4	5	6	7
/CEIV	/ACP	/OFSTCAL	/SINH	-	-	-	-

(a) CEIV (CE Intervention)

Reserved future.

(b) ACP (Address Compare)

This bit is '1' when the address compare function is successful.

(c) OFST (OFF LINE Start)

When this bit is set to '1' a processor trap will be occurred. This trap's vector address and level are same as the INS trap.

(d) SINH (Start Inhibit)

This bit suppresses an OFF LINE command initiation.

4.6 Controller Interface Control

4.6.1 Command initiation

The Controller instructs the formatter to initiate a command operation by asserting Initiate Command (START) Line. The START line is recognized by the formatter as a command initiation only when Formatter Busy (BUSY) Line is not asserted, and the START line have been reset once.

As shown on Figures 4.20 and 4.21, the INS signal is set at above-mentioned condition.

A trap to the mircoprocessor is caused by this signal while the trap mask bit is set to on. (See Subsection 4.4.3 for detail.) By this interruption, the microprogram traps from the idle loop routine to fixed address X"0100". The intial selection routine is then executed.

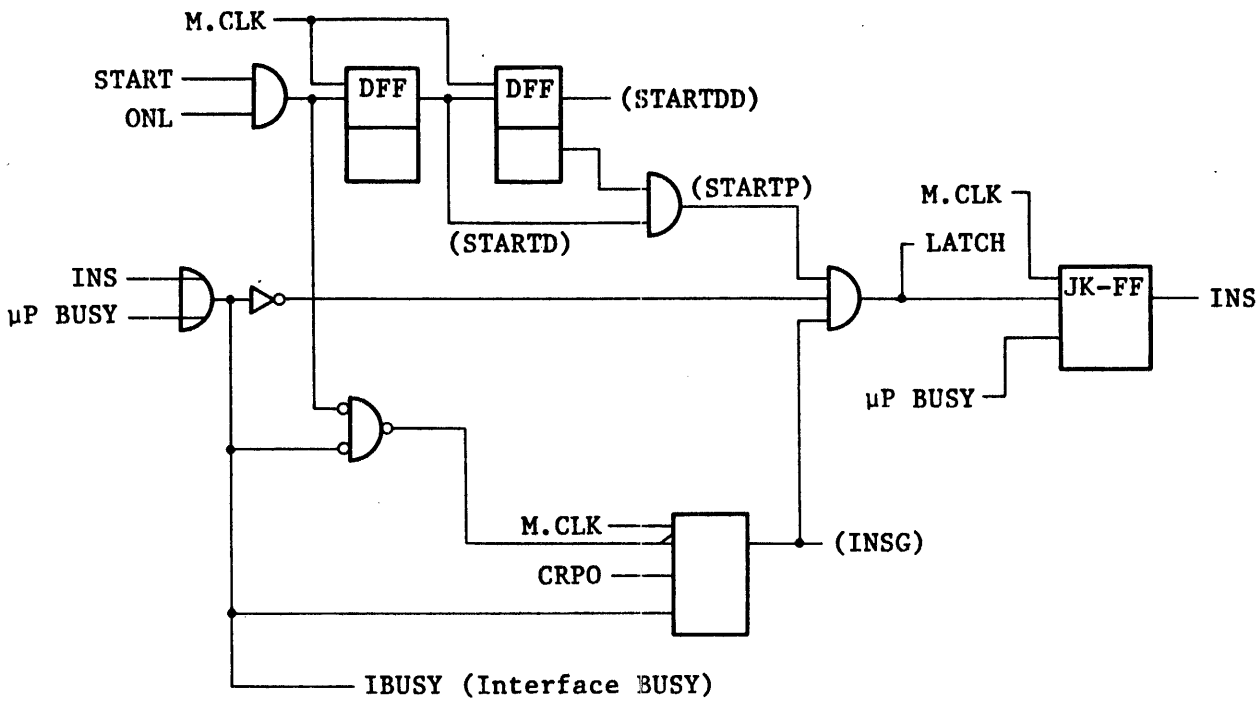


Figure 4.20 Initial selection diagram

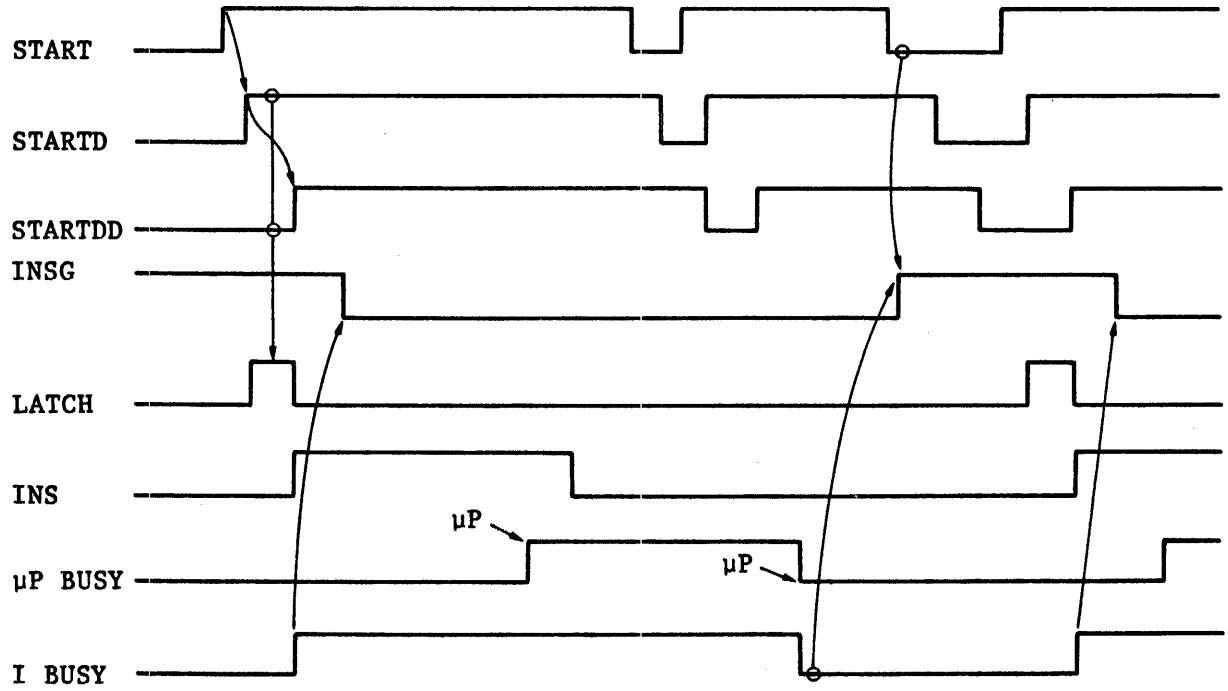


Figure 4.21 Initial selection time chart

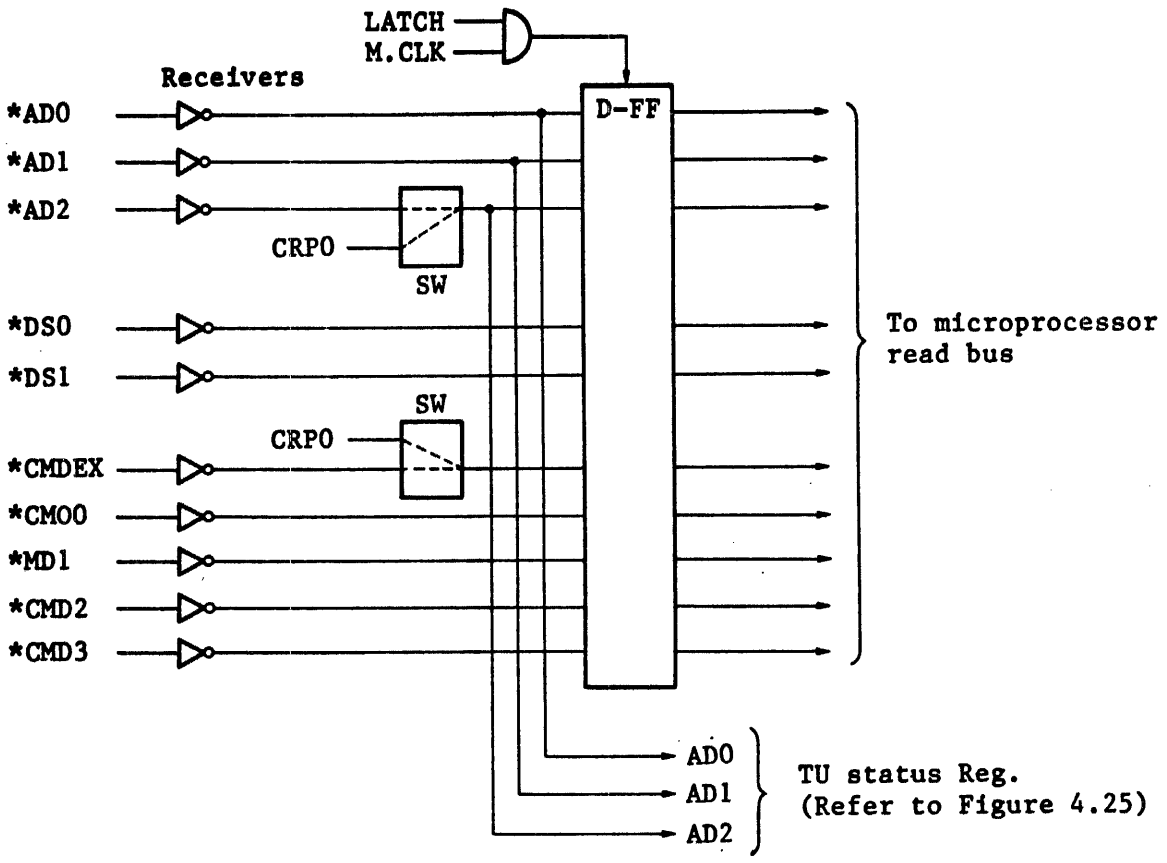


Figure 4.22 Controller output signal

The microprocessor can read output signals of interface receives of of TU Address Lines, Command Select Lines and Density Select Lines.

In an initial selection routine, the command information are stored in Local Stroge Registers and the formatter asserts BUSY Line.

4.6.2 Formatter status lines

All formatter status lines are set or reset by microprogram, except the ROM Parity Error line and the Data Bus Parity Error line.

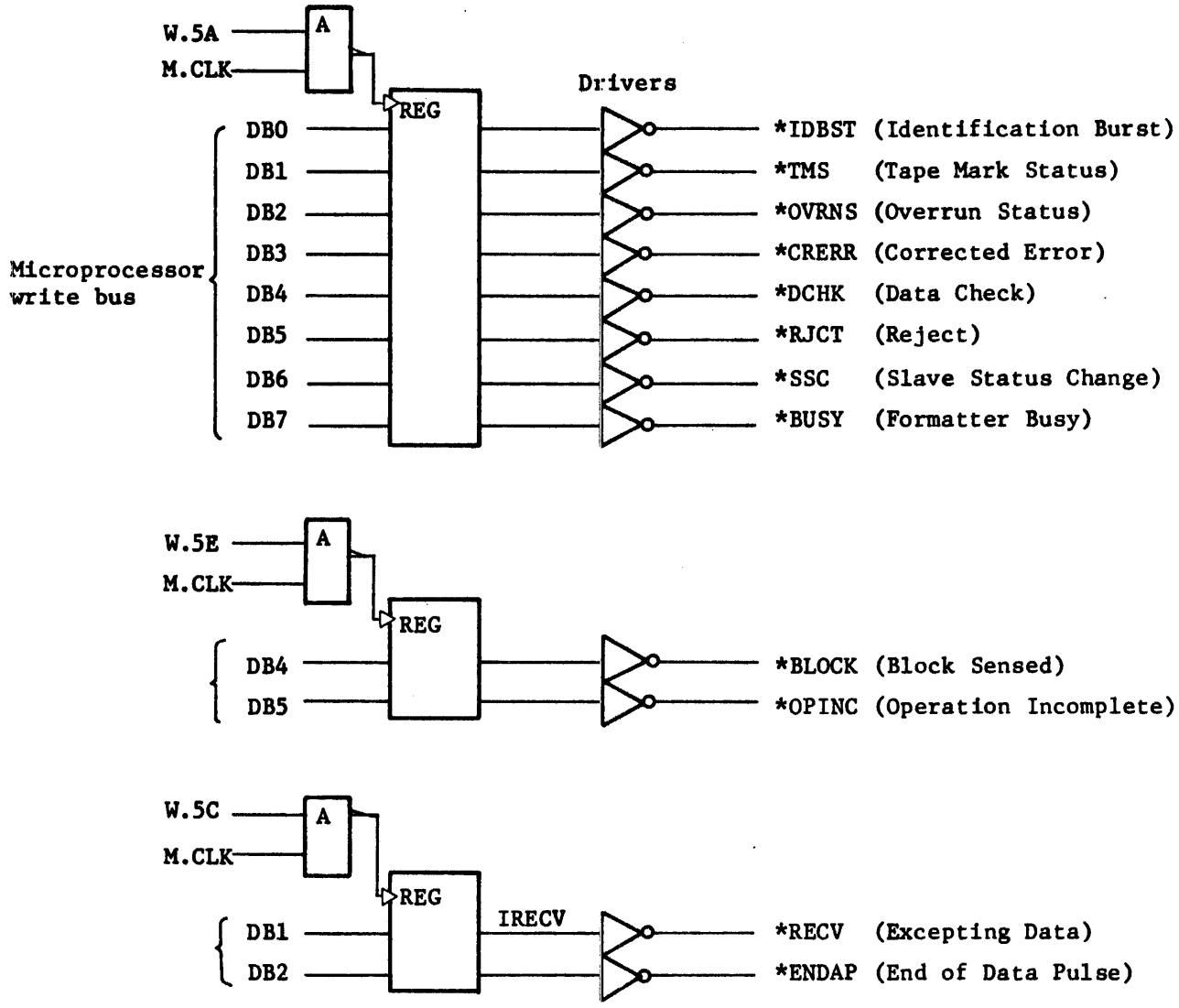


Figure 4.23 Formatter status

ROM Parity Error signal is set by hardware and reset by microprogram. If a parity error is detected in a Local Stroge Register or in Control Stroge, a PERR signal is set and the microprocessor is trapped. (See subsection 4.4.3.)

The ROMPS line is asserted when PERR signal is set. The Line is reset by the next (one or two) command initiation. The Data Bus Parity Error signal is also set by hardware during transfer sequence. This signal is reset by next command initiation.

4.6.3 Error multiplex bus lines

The (nine bits and seven bytes) Error Multiplex Bytes are shown in Figure 4.24. These MUX bytes consist of 9 bits - 8 bytes register file.

While the BUSY line is asserted, the read address of the register is set to the microprogram register address. When BUSY line is not asserted, one of the eight registers is mulTiplexed to the Error Multiplex bus as selected by SLXO, SLX1 and SLX2 lines.

The P biT of the Error Multiplex Bus is selected by the Selected Multiplex Lines when the controller selects Multiplex byte 2.

The MUX bytes are set by the microprogram before the formatter resets the BUSY line. The MUX bytes will remain asserted until the micro-program rewrites these bytes at the next command ending procedure.

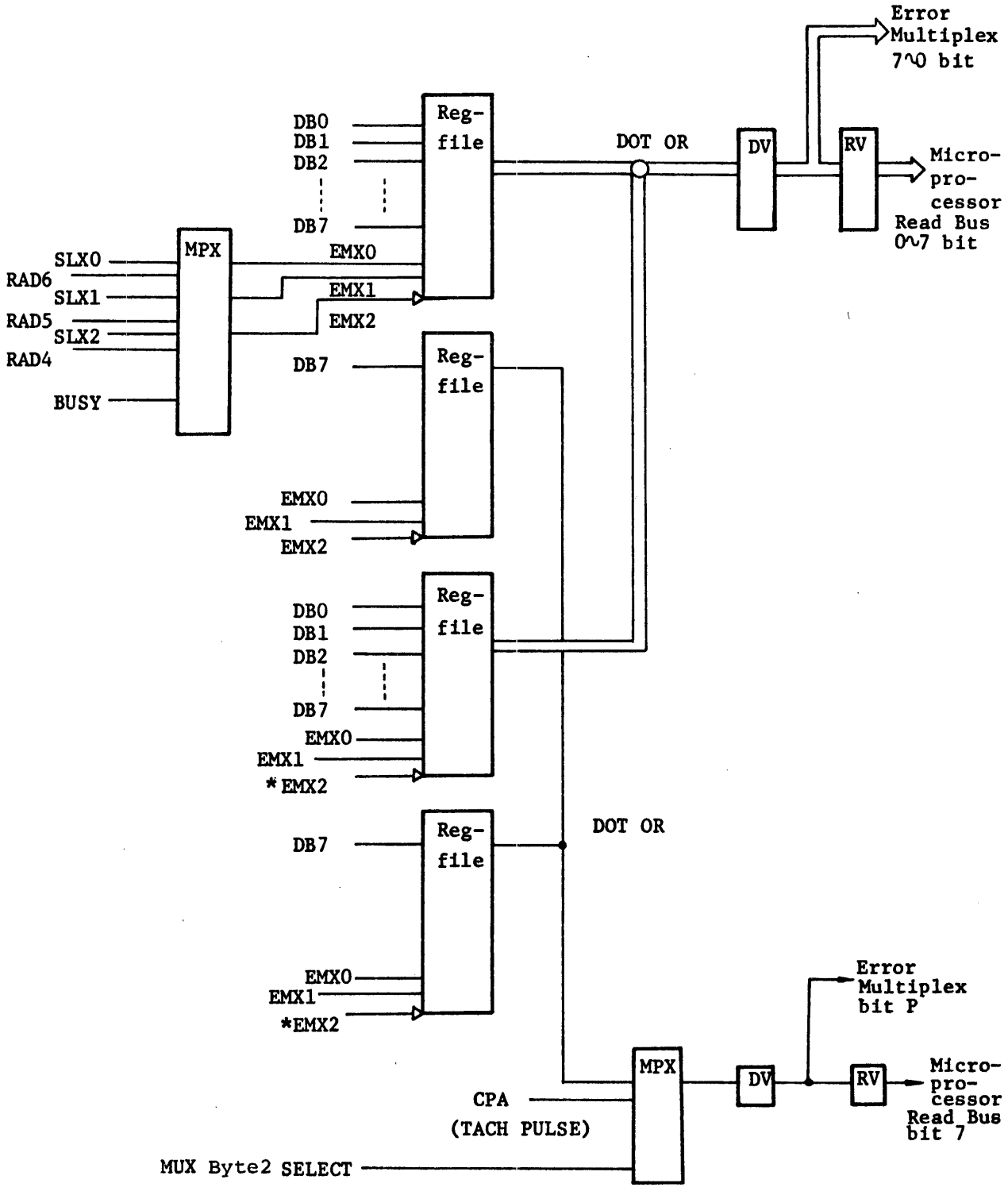


Figure 4.24 Error multiplex

4.6.4 TU status lines

There are 9 Tape Unit status lines.

Ready Status	**(RDYS)**
On Line Status	**(ONLS)**
Rewinding Status	**(REWS)**
Begin of Tape Status	**(BOTS)**
End of Tape Status	**(EOTS)**
File Protect Status	**(EPTS)**
Write Status	**(WRTS)**
High Density Status	**(HDENS)**
NRZI Status	**(NRZI)**

These status lines correspond to each TU address

While BUSY is asserted, these status lines show the status of the TU executing a command. As shown Figure 4.25, there are 8 bytes and 9 bits register files for each Tape Unit.

When the FMT is idle and the microprogram is in a Device Scan Routine, the Tape Unit Status is sensed and the contents of the register file are updated.

When the Controller asserts the START line and FMT initiates the start command, device address are latched before the FMT asserts the BUSY line. The read address of the register file is set to the latched address.

After the command operation, the read address of the register file is set to the TU address line directly and then the BUSY line is reset.

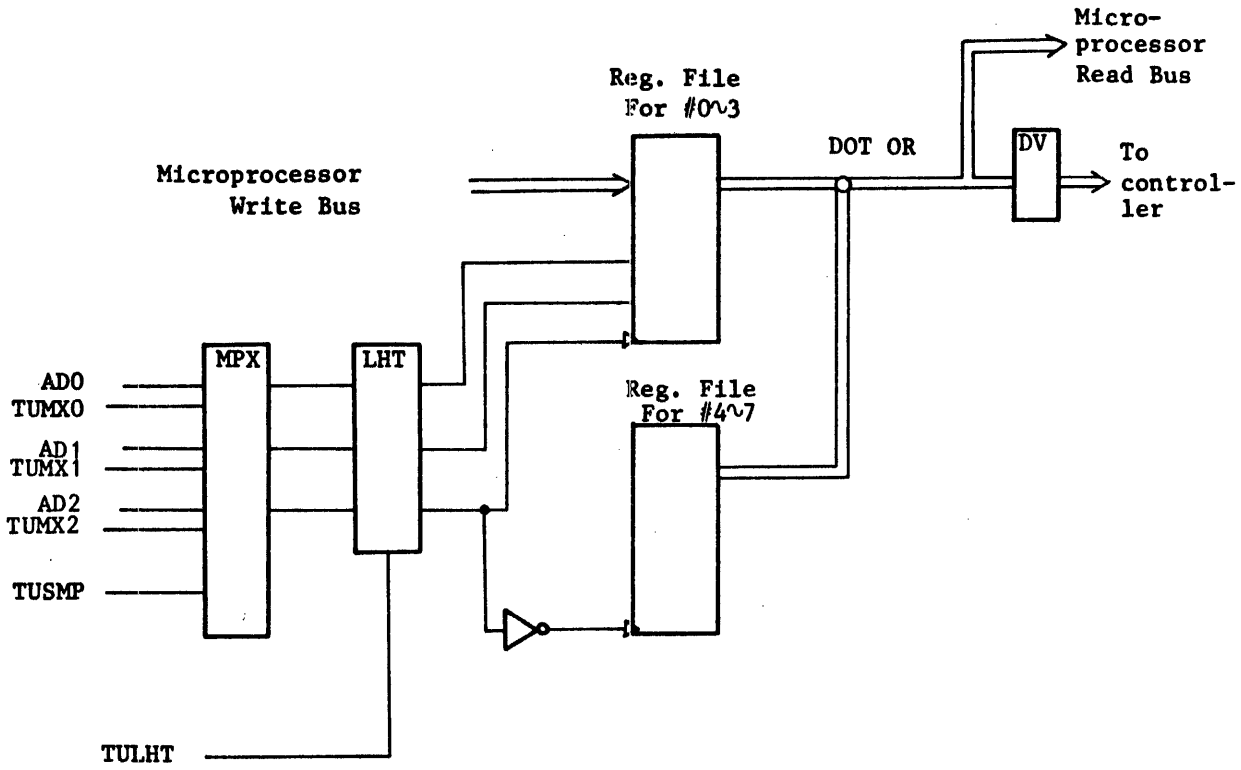


Figure 4.25 TU status register file

The write address line of the register file is always set to the microprocessor register read address.

4.7 Data Transfer Control

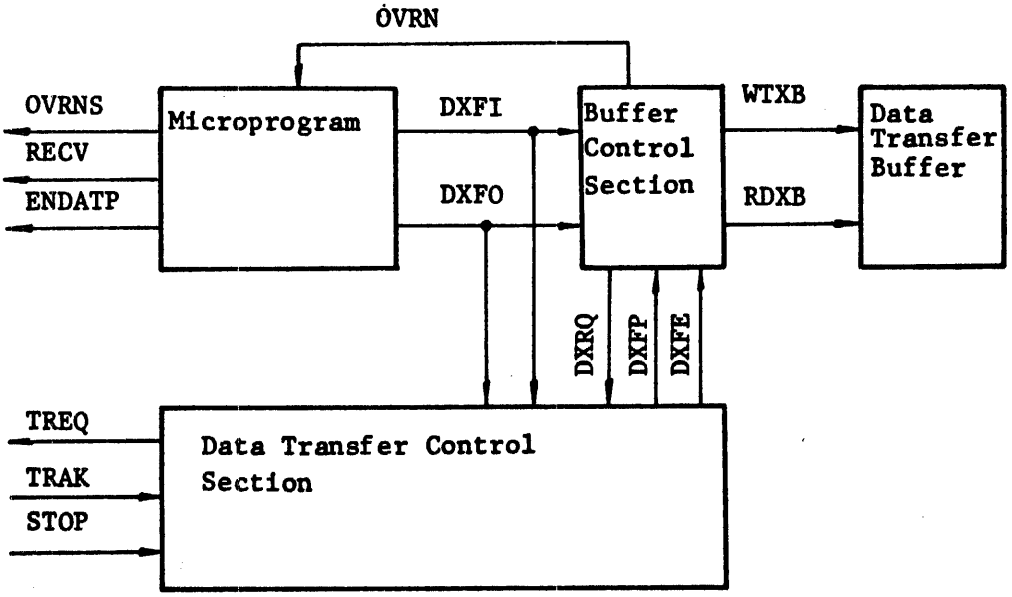


Figure 4.26 Data transfer block diagram

Explanation of abbreviations;

OVRNS	;	Overrun Status	(interface signal)
RECV	;	Excepting Data	(")
ENDATP	;	End of Data Pulse	(")
TREQ	;	Transfer Request	(")
TRAK	;	Transfer Acknowledge	(")
STOP	;	Terminate Command	(")
OVRN	;	Data Overrun	(internal error signal)
DXFI	;	Data Transfer In	(internal control signal)
DXFO	;	Data Transfer Out	(")
DXRQ	;	Data Transfer Request	(")
DXFP	;	Data Transfer Pulse	(")
DXFE	;	Data Transfer End	(")
WTXB	;	Transfer Buffer Write	(")
RDXB	;	Transfer Buffer Read	(")

As shown on Figure 4.26. the data transfer control section deals with control of read, write or diagnostic data.

4.7.7 Write end LWR command

When a command is issued, the command code is decoded by the microprogram. If the command is write or LWR command, the microprogram sets the bidirectional data bus to the data receiving mode, and asserts the RECV signal. The microprogram then sets the DXFO signal and the buffer control section asserts the DXRQ signal to the data transfer section. This means that the formatter initializes the data transfer section. The formatter initiates the data transfer cycle and data is transferred to the data section. Thus, the data section asserts TREQ signal to the Controller and waits TRAK signal. Write data transferred through the bidirectional data bus is set to the Bus OutRegister when TRAK signal is asserted. The exact trigger timing is 90 nsec. after the leading edge of the TRAK signal.

The TRAK signal is synchronized to the Formatter Full Clock (CLF) and the data transfer section issues the DXFP signal to the buffer control section. Write data is set to the data transfer buffer when the WTXB signal is asserted.

The WTXB signal is a one clock (CLF) delay of the DXFP signal. If the data buffer is filled with data, the DXRQ signal is reset and the data transfer sequence is suppressed until the BFUL (buffer full) signal is reset.

The BFUL signal is reset when data is read out from the buffer. The RDXB signal is a timing signal for reading out write data from the data transfer buffeR to the sub data group buffer.

WhenSTOP is asserted instead of TRAK , DXFE is set and the data transfer control section terminates the data transfer cycle. Transferred data (when STOP signal Is asserted) is transferred to the data transfer buffer.

4.7.2 Read and read backward command

When a Read Backward command is issued, the microprogram resets RECV and sets the bidirectional Data bus to a data transporting mode.

The FMT microprogram sets GO and causes the TU to read a block. DXFI is then set and the buffer control section waits to receive data from the read circuit. When data is read out, it is stored in the Data Transfer Buffer at the timing of WTXB. If there is data in the Data Transfer Buffer, DXRQ is set and the data transfer sequence is initiated.

When DXRQ is asserted, the Data TRansfer Control circuit sets the DXFP pulse signal and stores data to A-Register or B-Register alternately. In the Buffer Control Section, the read out counter of the data transfer buffer is counted up by the time of DXFP signal. In the Data Transfer Section, the TREQ and TRAK signal sequence is continued until end of the block is detected or STOP is asserted.

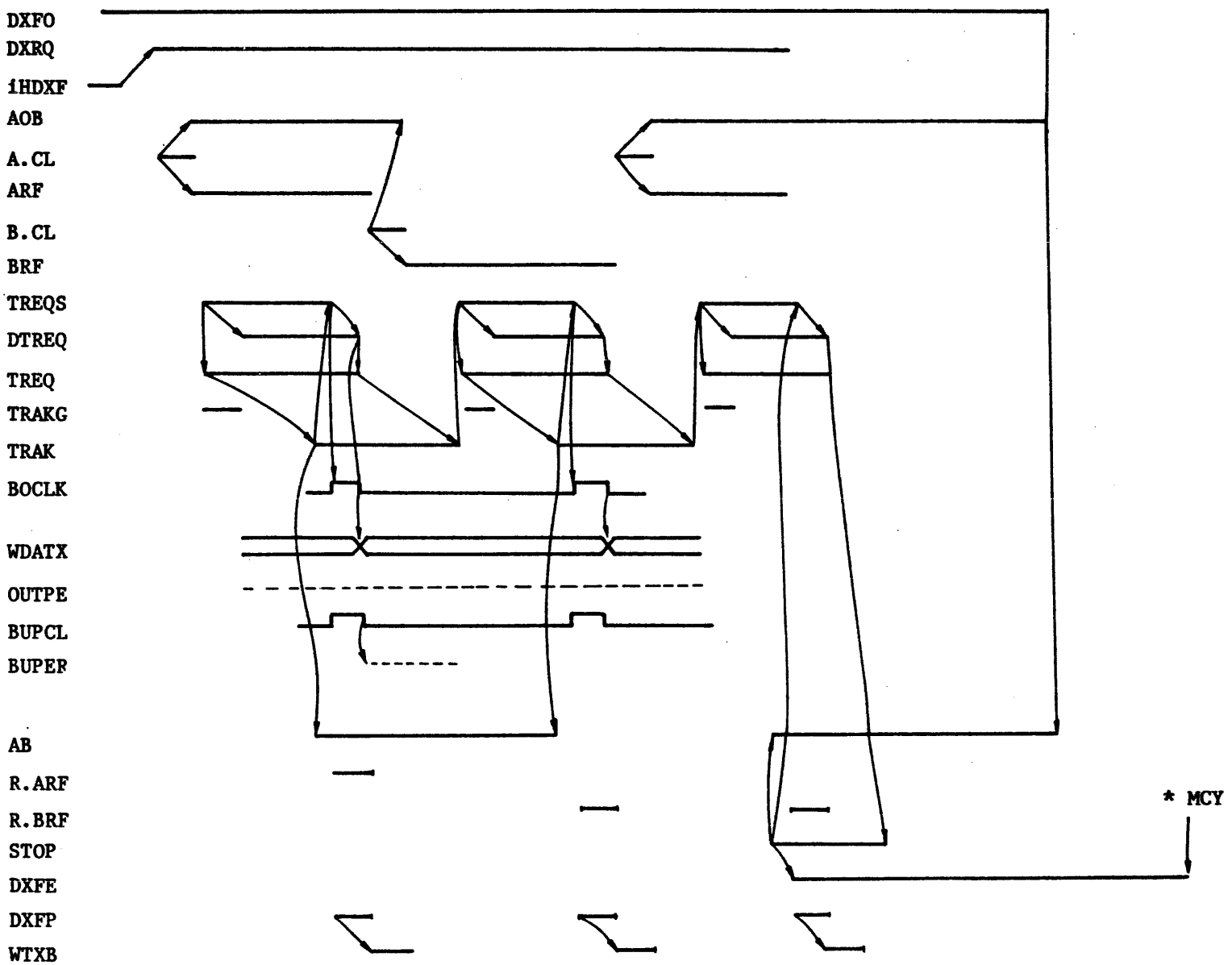


Figure 4.27 Data Transfer Timing of Write Command

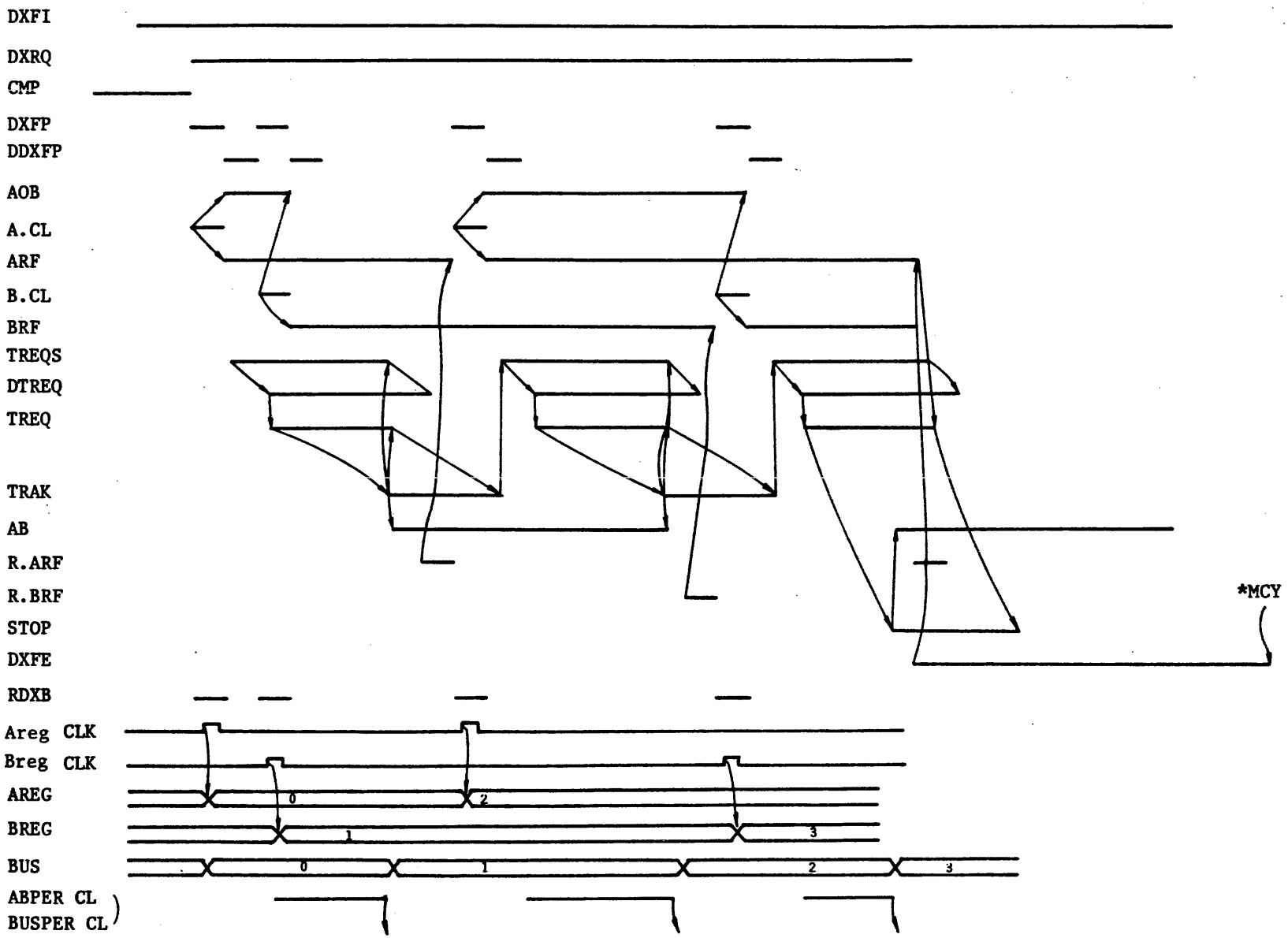
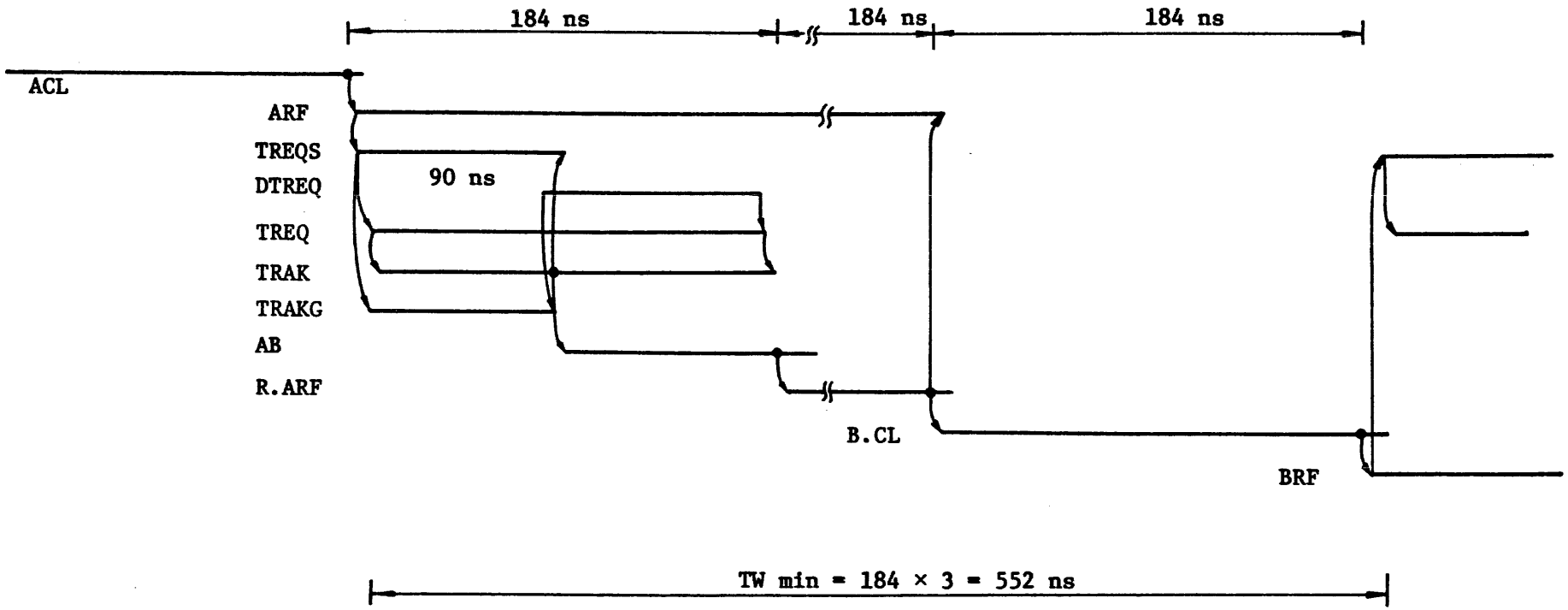


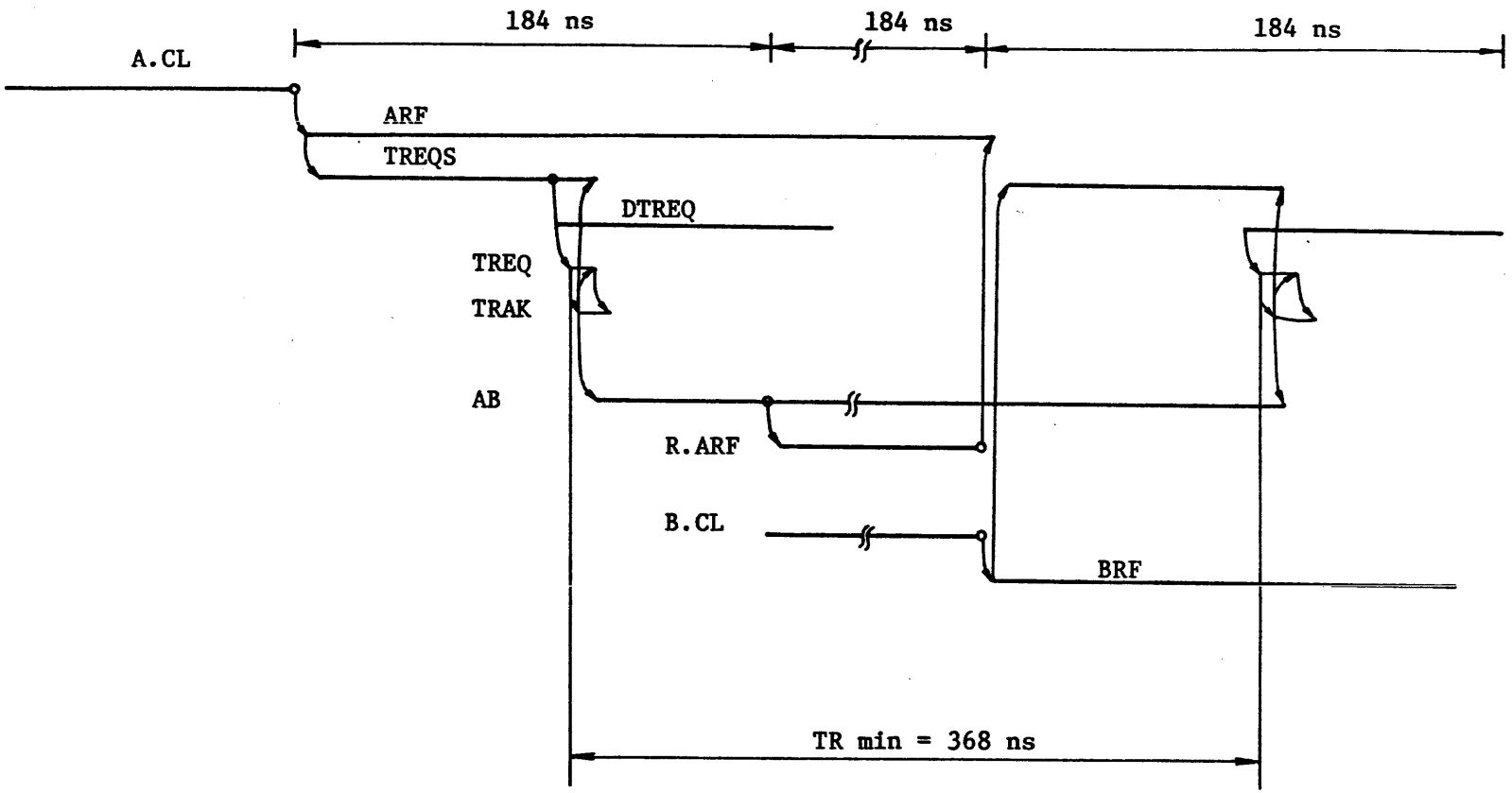
Figure 4.28 Data transfer timing chart of read command



TW min at WRT ----- Cable Length = 0, Controller Loss Time = 0
($T_C = 0_{ns}$) (TA1=0, TA2=0 ns)

TW min = 552 ns

Figure 4.29 Minimum loss time in FMT (for one byte receive at write)

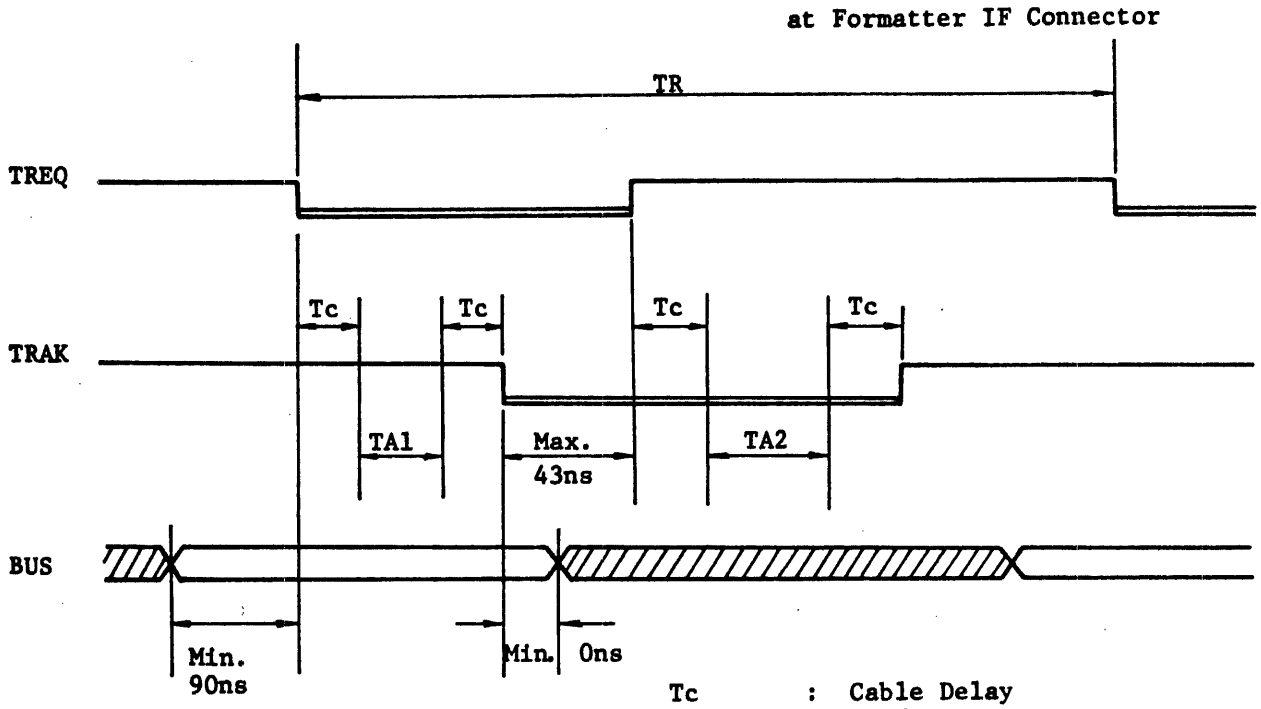


TR min at RD ----- Cable Length = 0, Controller Loss Time = 0
(T_C = 0) (TA1 = 0, TA2 = 0)

TR min = 368 ns

Figure 4.30 Minimum loss time in FMT (for one byte transfer at read)

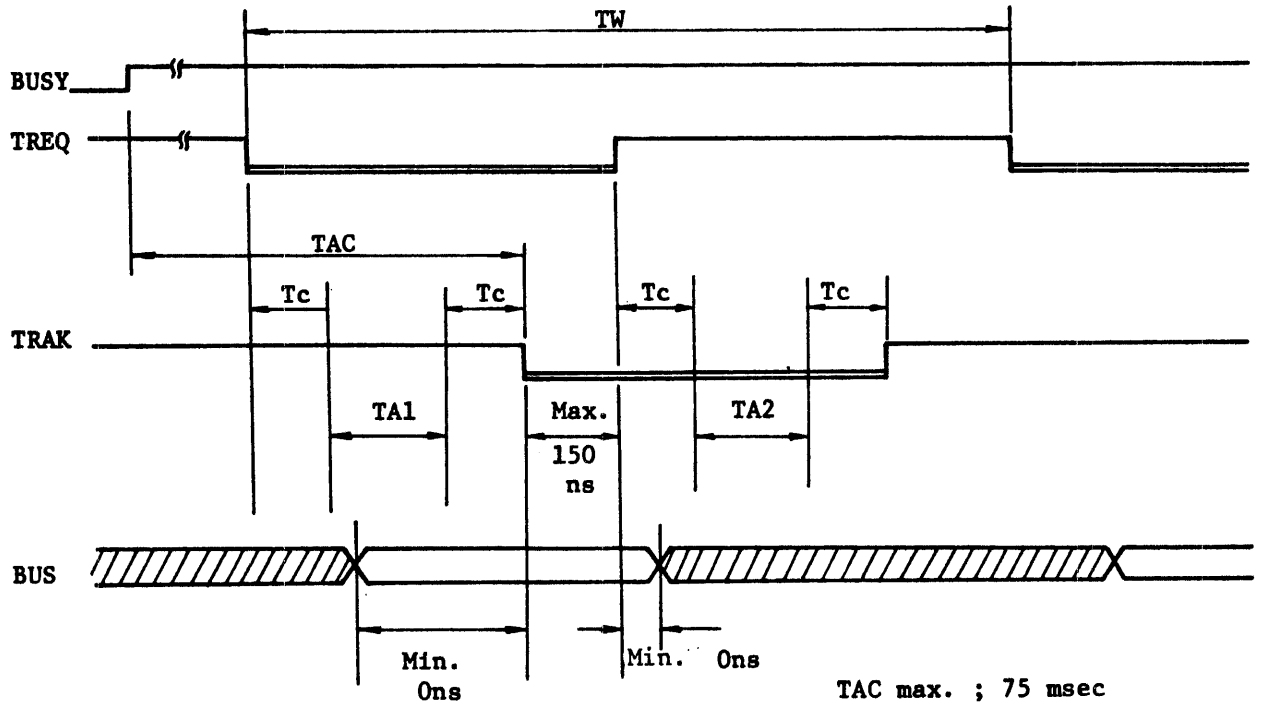
• RD or RDB command operation



Tc : Cable Delay
5ns/mx6m = 30ns

TA1, TA2 : Controller Handling Time
TA1 + TA2 = TAR

• WRT or LWR command operation



TAC max. ; 75 msec

Controller Handling Time TA1 + TA2 = TAW

Figure 4.31 Data handshake timing

4.8 Write Control

4.8.1 Format/Deformat clock

As shown in Table 4.26 the clock cycle of the format/deformat circuit varies with tape speed and recording density. The number of clocks per bit cell are 3τ in 6250, 6τ in 1600 mode and 12τ in the 800 mode.

Table 4.26 Format/Deformat clock

Speed (IPS)	Mode (RPI)	Full Clock (ns)	Half Clock (ns)
200	6250	184	92
	1600/800	521	260
125	6250	295	147
	1600/800	833	417
75	6250	494	247
	1600/800	1389	694
50	6250	738	369
	1600/800	2083	1042

Timing is controlled by the C and D counters. The relationship between the C, D counters and bit cells is shown in Figures 4.32, 4.33 and 4.34. The C-counter is also operational during the idle scan status.

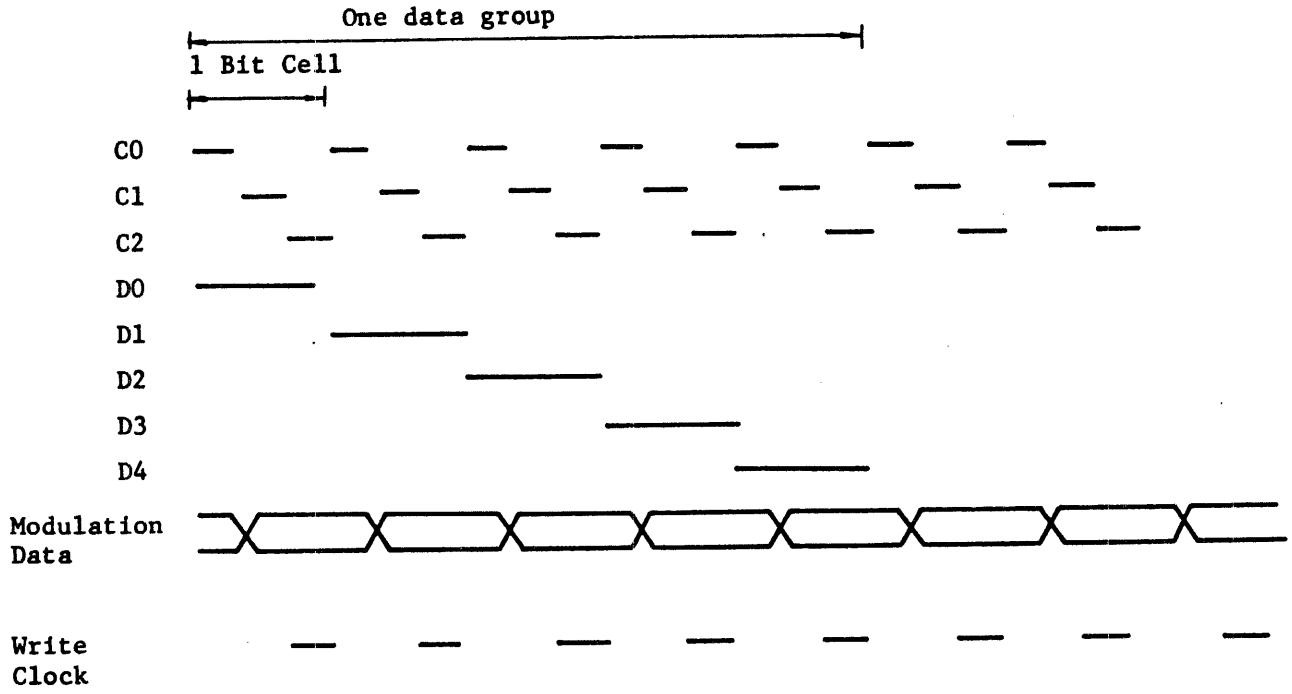


Figure 4.32 C, D counters in 6250 mode

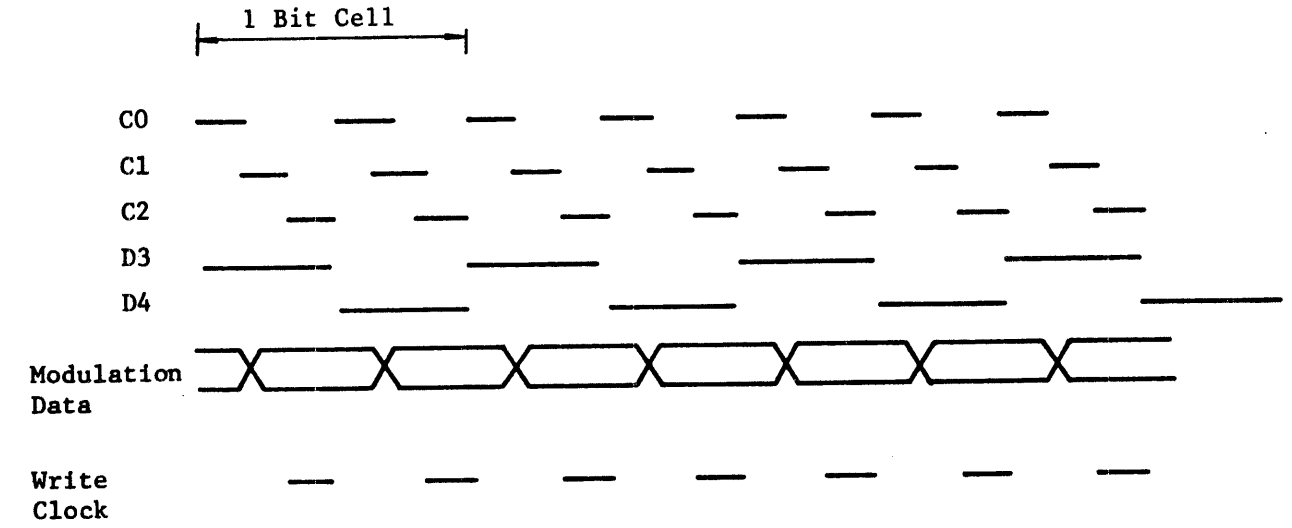


Figure 4.33 C, D Counters in 1600 mode

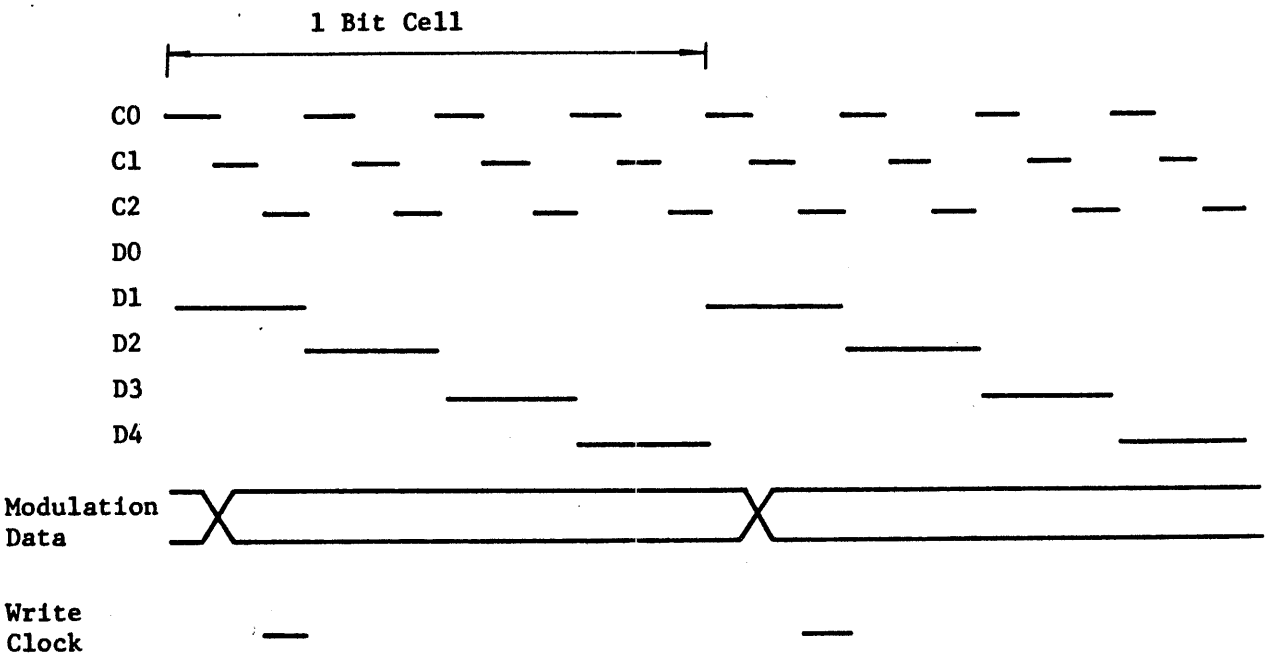


Figure 4.34 C, D Counters in 800 mode

4.8.2 Start write operation

Write processing is started when the microprogram sets a Writer OK signal (WOKA). As soon as the WOKA signal is set, the WOKD signal synchronized with the formatter clock is set. The D-counter starts as soon as WOKD is set. At this stage, the format counter starts. The Writer format is controlled by this format counter. WOKD is set as in D4 (D-counter) timing as follows: FCO(Format) in 6250 mode, FCI in 1600 mode, and FC4 in the 800 mode. The Writer clock sent to the MTU is gated by WOKD.

4.8.3 Format control

Write operation of preamble, postamble and data field is controlled by the format counter and the Group Counter (used to count data groups).

Table 4.27 Format counter

Format Counter	6250	1600	800
FC 0	TERM	PREA ALL "0" x 1	START
FC 1	SECOND	PREA ALL "0" x 1	-
FC 2	SYNC	PREA ALL "0" x 38	-
FC 3	MARK 1	PREA ALL "1"	-
FC 4	DATA GROUP	DATA	DATA
FC 5	MARK 2	-	-
FC 6	END MARK	POSA ALL "1"	CRC GAP 1
FC 7	RESIDUAL A	POSA ALL "0" x 1	CRC GAP 2
FC 8	RESIDUAL B	POSA ALL "0" x 1	CRC GAP 3
FC 9	CRC A	POSA ALL "0" x 1	CRC
FC10	CRC B	POSA ALL "0" x 1	LRC GAP 1
FC11	MARK 2	POSA ALL "0" x 1	-
FC12	SYNC	POSA ALL "0" x 32	-
FC13	SECOND	POSA ALL "0" x 1	LAC GAP 2
FC14	TERM	POSA ALL "0" x 1	LRC GAP 3
FC15	(WOK RESET)	POSA ALL "0" x 1	LRC

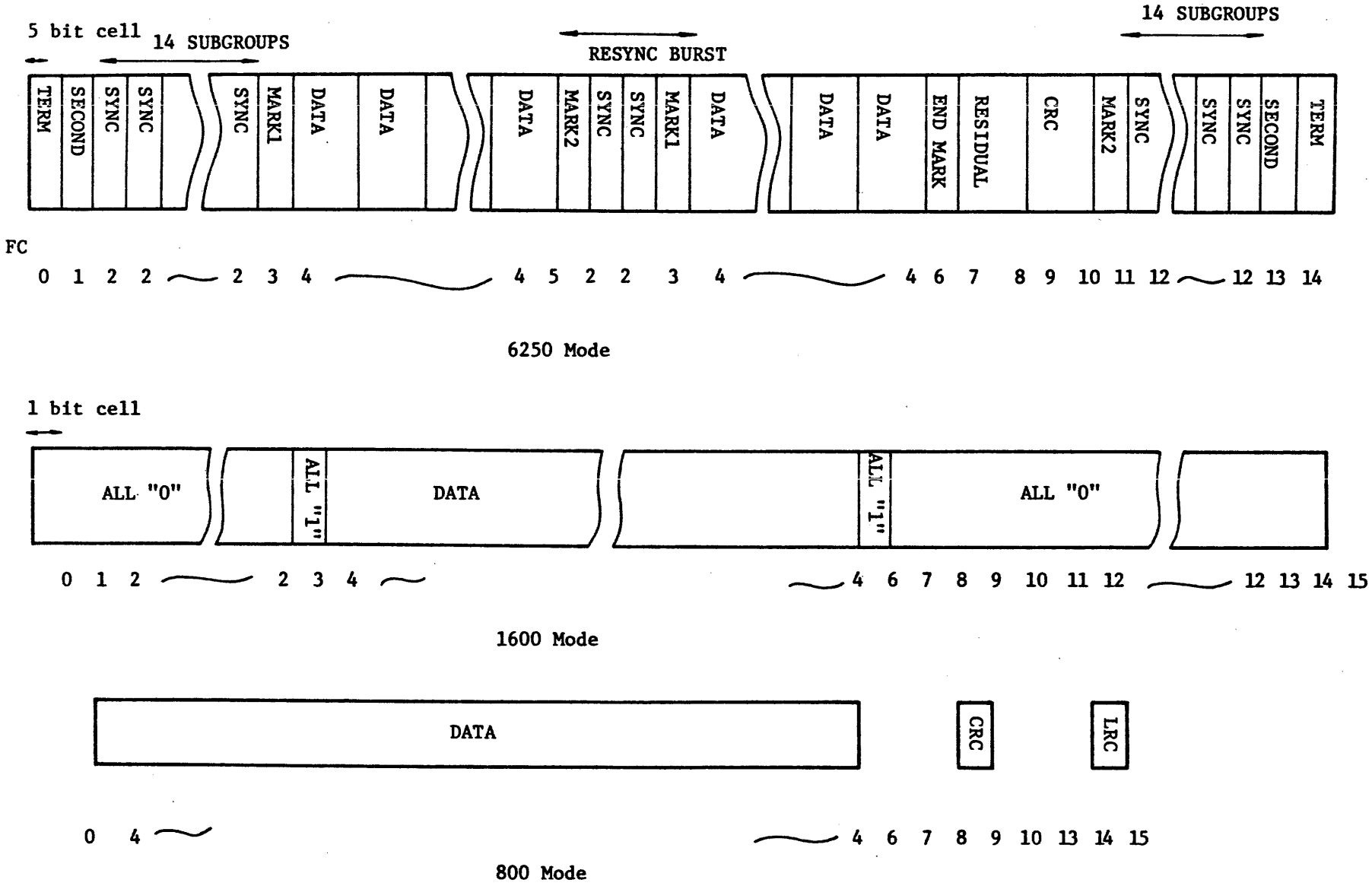


Figure 4.35 Data Format

4.8.4 Data bus

The Write data received from the Controller is entered into the transfer buffer when the WTXB signal obtained by delaying DXFP signal by 1 pi is set to ON. First, DXFO is set by the microprogram, and after data is stored in the transfer buffer, the WOK signal is set. Then the Write operation is started. First the preamble is written, and data is read out from the buffer at C2 timing after the format counter becomes "4" and R0+1W signal be comes "1". The data readout from the buffer is entered into the CRC LSI.

In CRC LSI, the data passes through the Write Bus Multiplexer. Here ECC characters, padding characters, etc. are added and are output from the LSI by both buses. The relationship between Selector Signals WBSL1, 2, and 4 on the Write Bus Multiplexer and WDAT 0-8 signals is shown in Table 4.28.
When WBSL1, 2, are all '1's, the CRC Check circuit status passes through the Write Bus Multiplexer (instead of Write Data).

The parity bit of Write data is obtained from the Write Bus Multiplexer output. This bit is compared with the parity bit from the buffer out register. If they do not match, the Write Bus Out Check signal (WTBOC) is set to '1'.

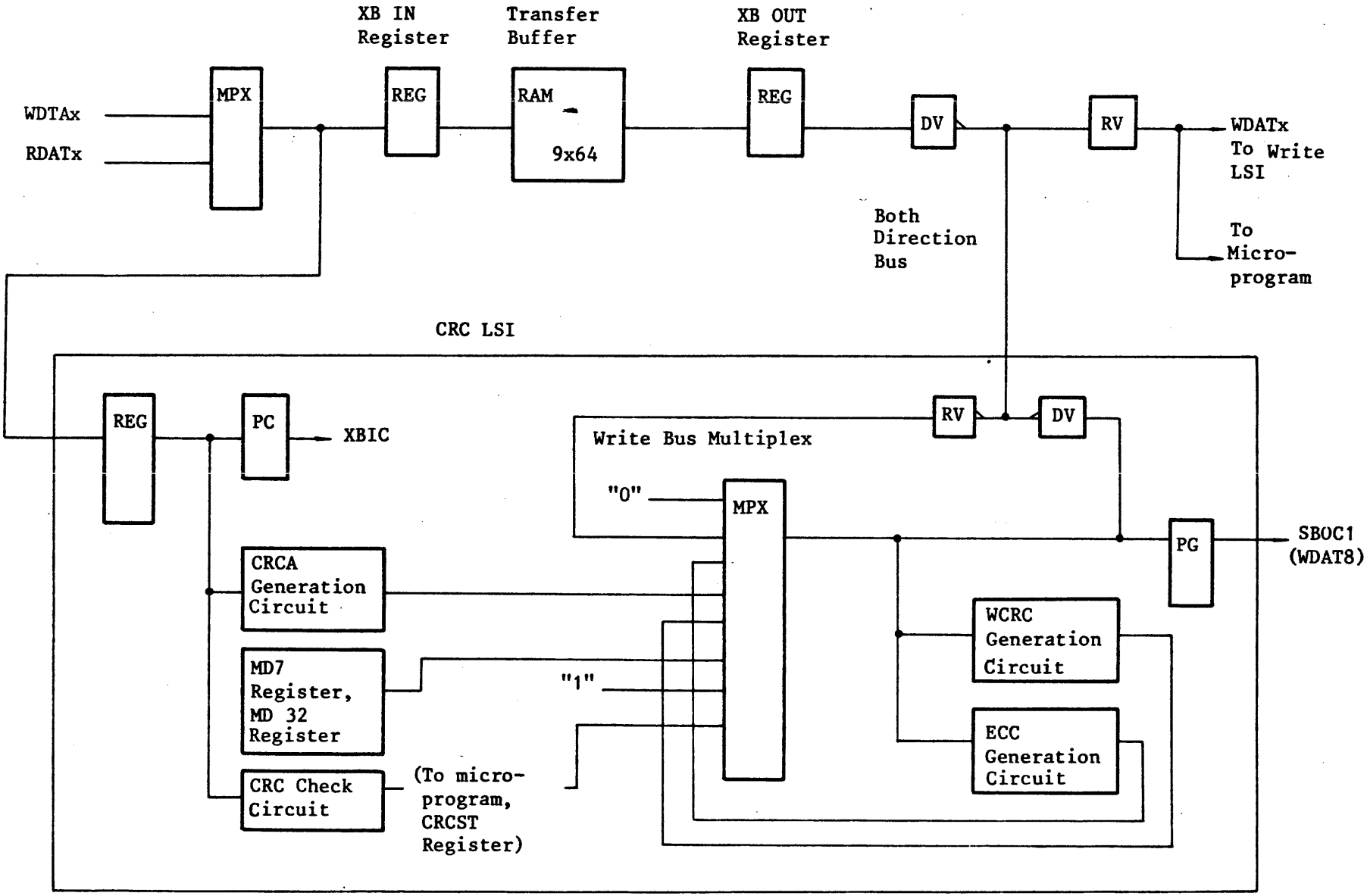


Figure 4.36 Transfer buffer and write bus selection

Table 4.28 Write bus selection

WBSL 421	Input Data	WDATX Description
000	"0"	Padding Character
001	XBOx (Transfer Buffer Output)	Data Character
010	ECC Register	ECC Character
011	CRC Register	Aux, CRC Character
100	WCRC Register	CRC Character
101	MD7, MD32 Register	Residual Character
110	"1"	1600 mode Preamble, Postamble All '1'
111	CRC Check Circuit Error	Data Sensed by the Microprogram, CRCST Register

Transfer Buffer input data is subject to a parity check in the CRC LSI. Parity bit is not generated but bit 8 in the Bus Out register (BO-reg) is entered to the transfer buffer.

4.8.5 Write modulation circuit

In the 6250 rpi mode, the data output by the Write Bus Multiplexer is fed to the WRT LSI. The first four bits (one subdata group) are set in the sub-group register. The four bit data is converted into five bits and is set in parallel in the five-bit shift register. The data is then read out serially and fed to the modulation register. The data from the modulation register (the JK flip-flop) is applied to the JK input to generate NRZ data.

The MSEL signal is set to '1' for Writing SYNC, MARK1, MARK2, TERM, SECOND and END MARK. In this case, the FM0-4 signal is preset in the shift register instead of a 4-5 conversion data.

The INHGC signal in the data field is set ('1') when DMW mode is specified. At this stage, subgroup register bits 1, 2 (CVR1, 2) are also set to '1' simultaneously. All '0's are set in the serializer to inhibit entry of the subdata group. If INVLD signal is ON under the above conditions, all '1's are preset and invalid code of all '1's is entered in its subdata group.

When a Mask is specified, modulation register output is gated and all '0's are entered.

If the inhibit preamble or inhibit postamble is specified, the IHAMB signal is set to '1' during preamble or postamble processing and the modulation register output is gated as in mask processing.

In the 1600 rpi mode, MSEL is set to '1' when the format counter is between 0-2 or 7-15. Whenthe counter is 3 or 4, '1's are set in the lower two serializer bits. MSEL is '0' when the format counter is 3, 4, or 6. At this stage, the data from the Write Bus Multiplexer is set in the subgroup register, bits 3-4 are sujected to PE conversion, and are set in the lower two serializer bits (if D4 signal is '1').

In the 800 rpi mode, MSEL is turned ON ('1') when the format counter is at 6, 7, 8, 10, 13, 14, or 15. At this stage, CRC gap and LRC gap ('0') are preset in the serializer. When the format counter is 4 or 9, the data or CRC Byte from the Write Bus Multiplex is set in the subgroup register. Bit 4 will be set in the lowest bit of the serializer if signal D4 is '1'. The data in the modulationl register is entered as an LRC byte.

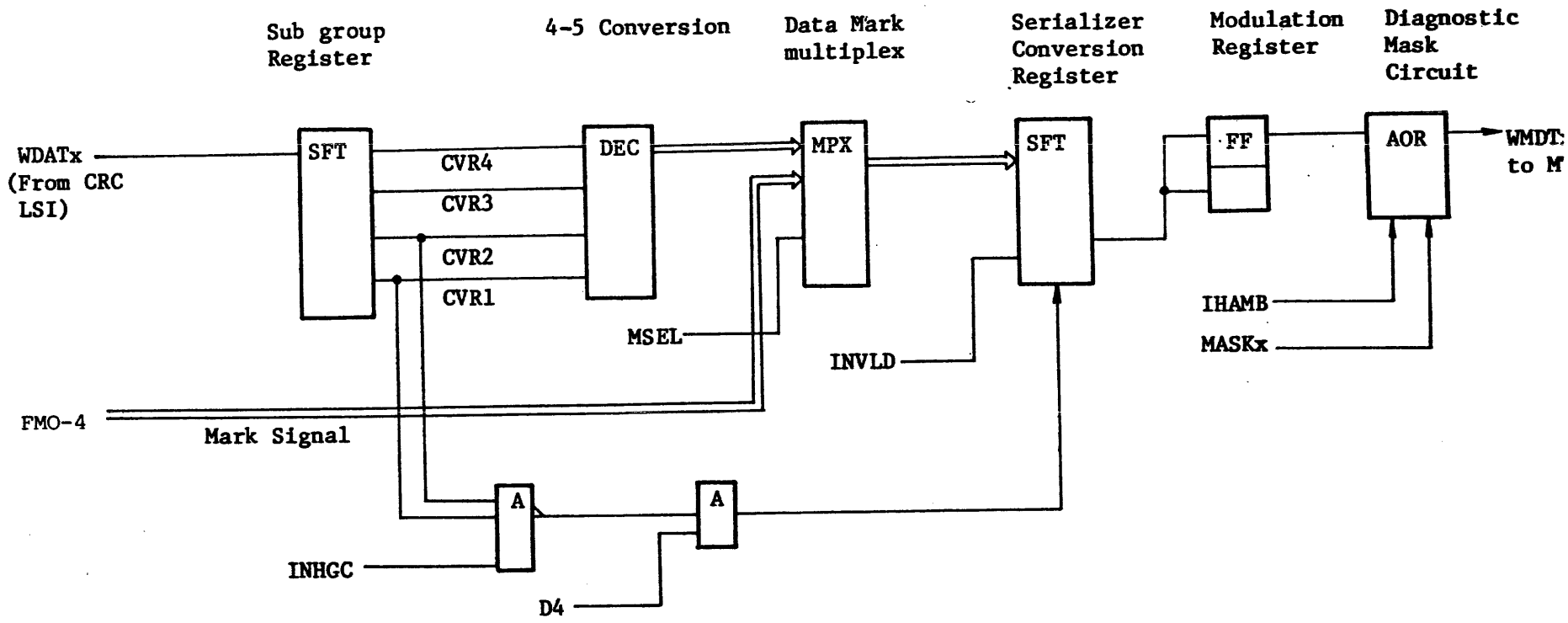


Figure 4.37 Write modulation circuit (one track)

4.8.6 Write VRC check

A parity check on the Write Modulation Wave Form is performed when the Write Pulse is '1' (WTPL signal) and ALlWT signal is "0'.

In the 6250 mode, the 9 track parity at the end of NRZI subdata group (D4 signal = 1) confroms with predetermined conditions. The subdata groups of residual data and CRC data Have odd parity. The subdata group of the data has even parity. SYNC in the mark field is a repetition of even and odd parities. OtHer mark fields may have uniform pArity depending how they are entered.

In the 1600 rpi mode, when the subdata group of the daTa is transferred, a check is executed to confirm odd parity after inVerting the phase. In the PE mode, data is '1' when the Write Modulation Wave changes to '0' from '1'. Data '1'1 is checked to be level '1'.

In the 800 rpi mode, onlY the data field is checked (format count: 4). Odd bytes are at odd parity while even bytes are at even parity. DEVN is set to '1' for odd bytes.

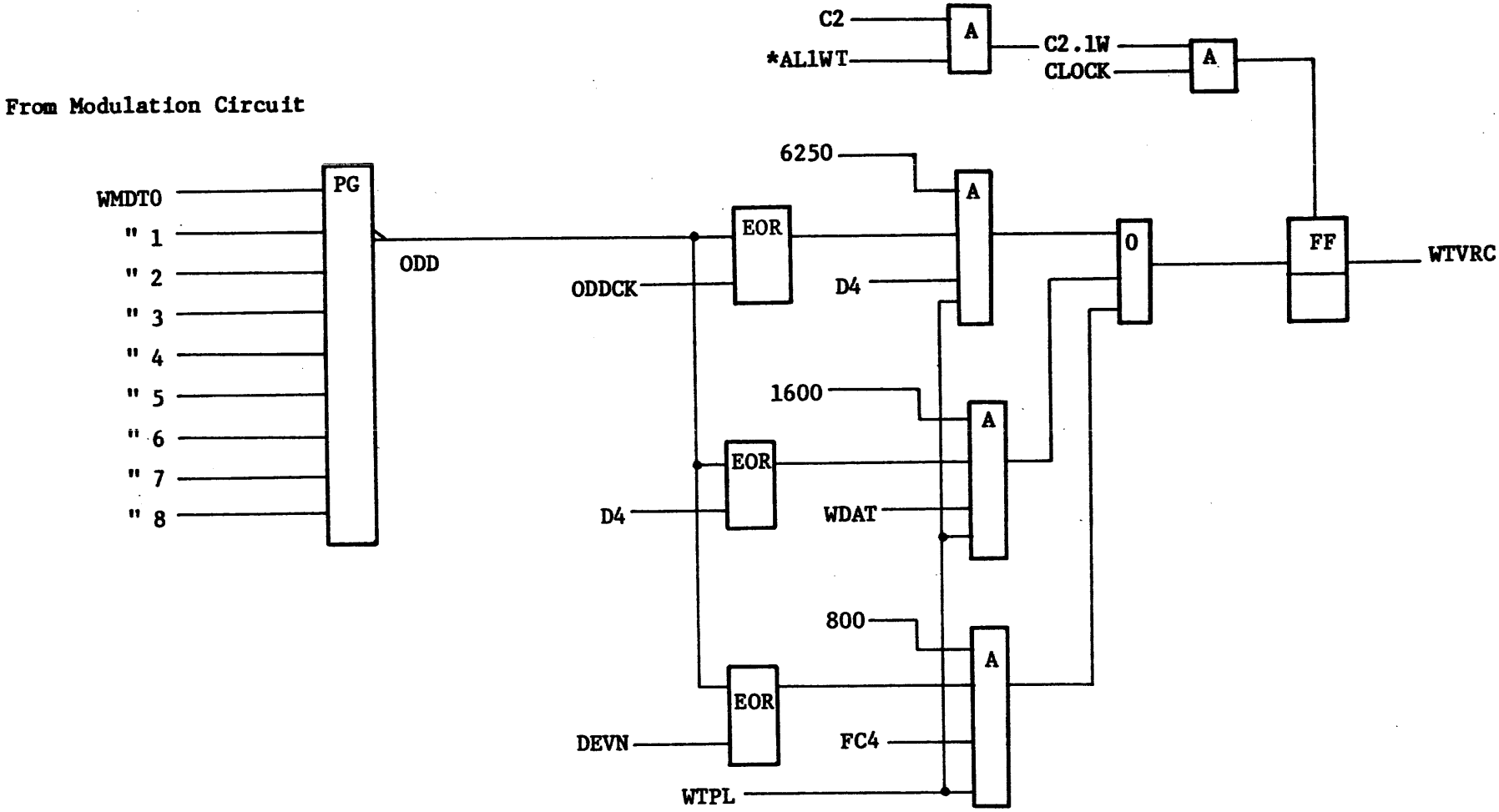


Figure 4.38 Write trigger VRE circuit

4.9 Read Control

This section describes operations of Read Command, Read Backward Command and Read after Write Check of Write Command. The Bus In Data (VBI0-8) passes through the analog circuit, and is converted into Modulated Data (DEMD 0-8), Read Clock (SRIC 0-8), Phase Error (PHER 0-8), and Peak Pulse (PEKP 0-8) signals, respectively.

As shown in Figure 4.39, these signals are transfer to Read Circuit, as detection of blocks, check format, modulate data, check data and error correction signals.

The Mard DeTection circuit, Skew detection circuit and 5-4 conversion circuit correspond to three tracks each and are made up of 3 LSI's.

Pointer circuits are made of three LSI's (3 tracks) while the error correction and detection circuits consist of one LSI each.

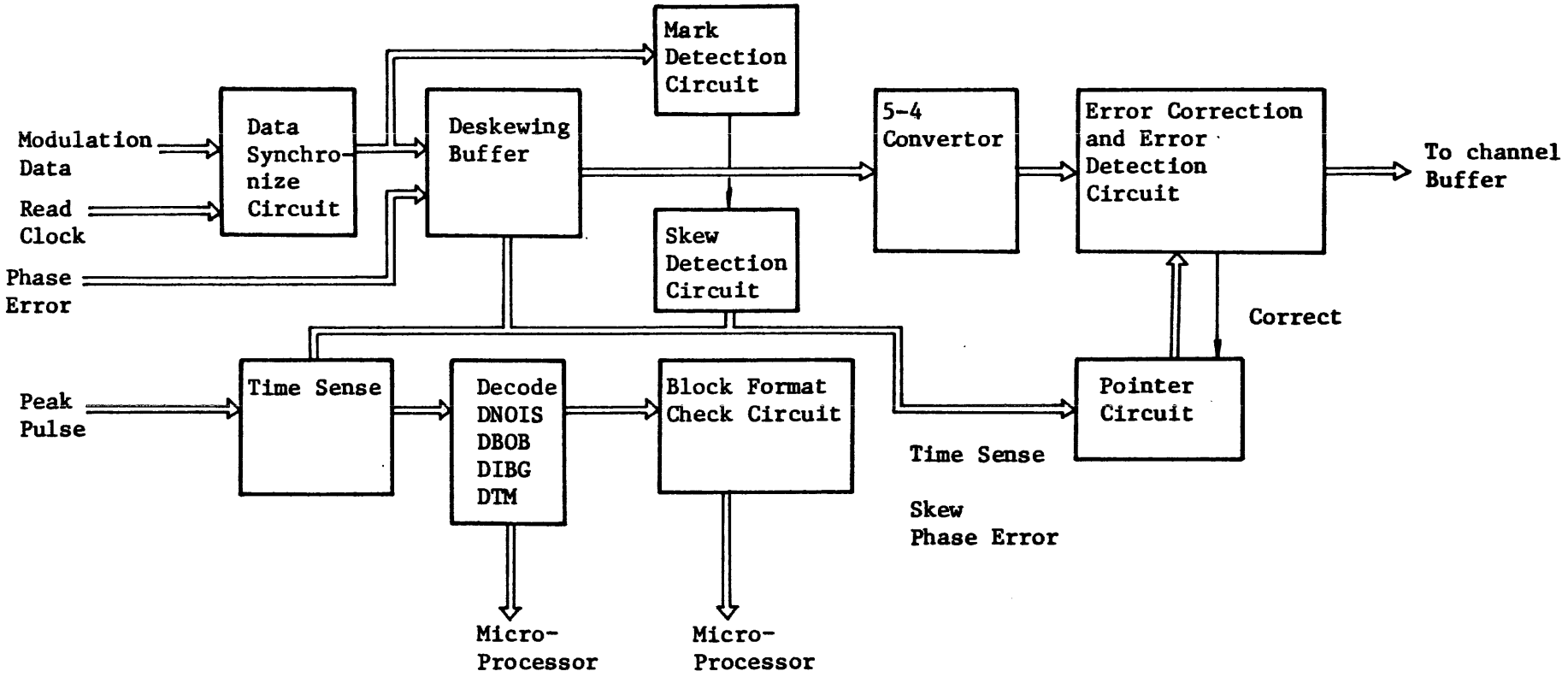


Figure 4.39 Read block diagram

4.9.1 Time sense

As soon as the Read OK signal (ROK) is set, the Peak Pulse signal (PEKP0-8) which is the differential signal from Bus In data (DVBI0-8) is generated.

In the 6250 rpi mode, if the peak pulse is detected for a ten bit cell period, Time Sense is set (TSNS 0-8). On the other hand, if the peaK Pulse is not detected for a 5 bit cell period, the time sense signal is reset. In the 1600 rpi mode, the time period for setting the sense signal is 5 bit cells and for resetting it is 2.5 bit cells.

The time sense values of each tracks are decoded to generate Clock detection (DBOB), IBG detection (DIBG) or Tape Mark Detection Signals (DTM). Signal detection logic is shown below in the form of a logical equation.

TSNS0-8 shows 0-8.

DBOB = (4.1.3+6.2.7+0.8.5).(4+1+3).(6+2+7).(0+8+5)

DIBG = $\overline{0}.\overline{1}.\overline{2}.\overline{3}.\overline{4}.\overline{5}.\overline{6}.\overline{7}.\overline{8}$

DTM (For Write) = $0.\overline{1}.2.\overline{3}.\overline{4}.5.6.7.8$

DTM (For Read in 1600 RPI mode) = $\overline{1}.\overline{3}.\overline{4}(2.6.7+0.5.8)$

DTM (For Read in 6250 RPI mode) = $1.3.4\{2.6.7.(0+5+8)+(2+6+7).0.5.8\}$

DARA (For Write) = $\overline{0}.1.2.3.\overline{4}.5.6.7.\overline{8}$

DARA (For Read) = $\overline{0}.\overline{5}.\overline{8}\{1.3.4(2+6+7)+(1+3+4).2.6.7\}$

DNOIS = 0.4.6+1.2.8+3.5.7+(0+4+6)(1+2+8)(3+5+7)

4.9.2 Block format check

The following function are described in this section:

a) HNIS signal for identifying a block in Write Command, and Back Read type Command after write Command.
b) HBLK signal for detecting a block in Read type Command.
c) HTM signal for detecting a Tape Mark.
d) EPOSA signal that resets the PHOK signal.
e) End Data Check Counter.
f) Start Read Check Counter.
g) Slip Check Counter.
h) Noise Check Counter.

When the DBOB signal is set to '1' on decoding the time sense, it is counted to WOS1 signal set to '1' on decoding the time 6250 RPI mode and 1 bit cycle in 1600 RPI. As soon as a carry is generated at the 12th clock, HBLK signal is set along with PHOK signal.

The Read circuit is activated as soon as PHOK is set to '1'. The PHOK signal is reset and the Read circuit is cleared when the bit cell count shown in Table 4.29 is completed (after postamble is detected and POSA signal is set to '1'.

Just as the HBLK signals; HNIS, HTM, EDDCK, STRDC, NOISC and SLIPC signals are counted by WOS1-16 signals. The are reset By the bit cells shown in Table 4.29.

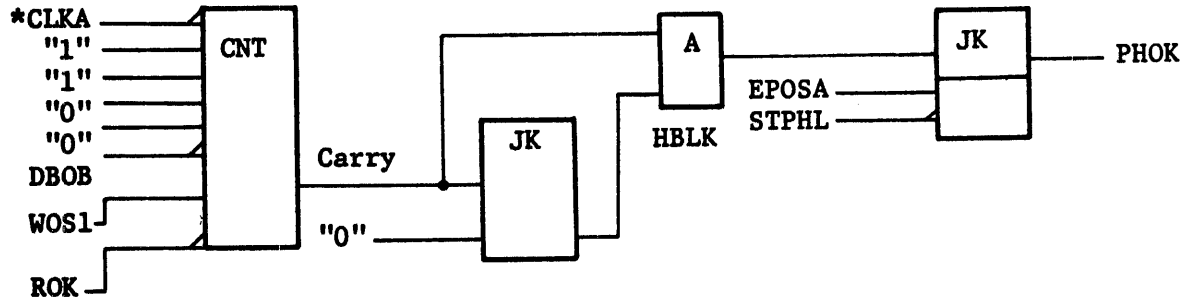
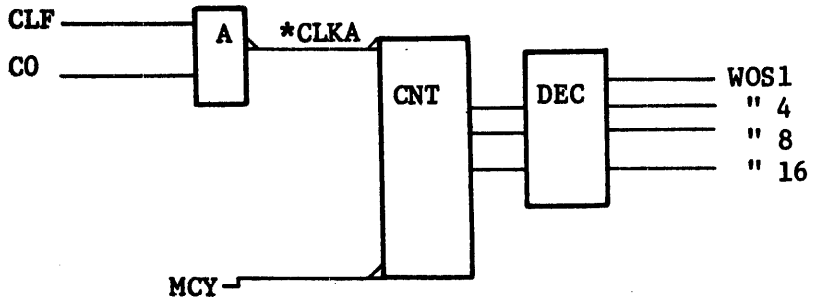


Fig. 4.40 HBLK and PHOK signal



	6250 Mode	1600 Mode	800 Mode
CO	1	1/2	1/4
WOS1	2	1	1/2
WOS4	4	2	1
WOS8	8	4	2
WOS16	16	8	4

bit cell

Figure 4.41 Check count values of block format

Table 4.29 Check values of block format

HNIS	GCR	Write Read	46 ±2 22 ±2	Counts DNOIS Signal.
	PE	Write Read	23 ±1 11 ±1	
HBLK	GCR	-	25 ±1	Counts DBOB Signal.
	PE	-	12.5 ±0.5	
HTM	GCR	Write Read	304 ±8 42 ±2	Counts DTM Signal.
	PE	Write Read	84 ±4 21 ±1	
EPOSA	GCR	Write Read	34 ±2 6 ±2	Set if POSA are detected in series for the bit cells on the left.
	PE	Write Read	31 ±1 21 ±1	
EDDCK	GCR	Write Read	88 ±8 248 ±8	Set if DIBG signal is not turned ON Upon expiration of the bit cell period (mentioned on left) after starting EPOSA Count.
	PE	Write Read	20 ±4 36 ±4	
STRDC	GCR	Write Read	120 ±8 168 ±8	Set if PREA signal is not detected upon expiration of the bit cell period (noted on the left) after detecting HBLK.
	PE	Write Read	52 ±4 63 ±4	
NOISC	GCR	-	1084 ±4	Set if DBOB is detected with the bit cell period (noted on the left) after WOK signal.
	PE	-	192.5 ±0.5	
	-?0% for RW Head Gap			
SLIPC	GCR	-	1448 ±4	Set if DNOIS signal is not detected within the bit cell period (noted on the left) after WOK signal.
	PE	-	268 ±0.5	
	+7% for RW Head Gap			

4.9.3 Basic read timing

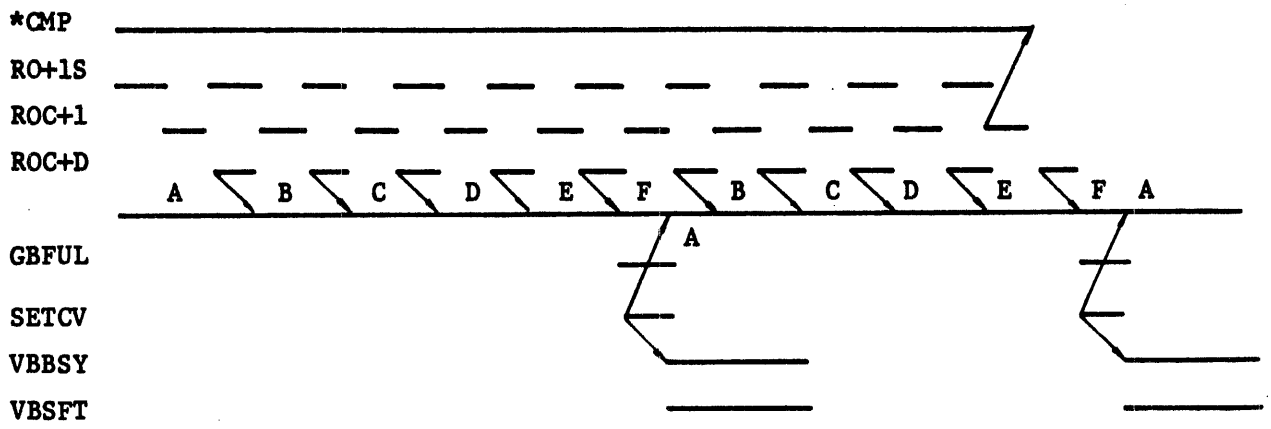


Figure 4.42 6250 RPI basic timing (1 of 2)

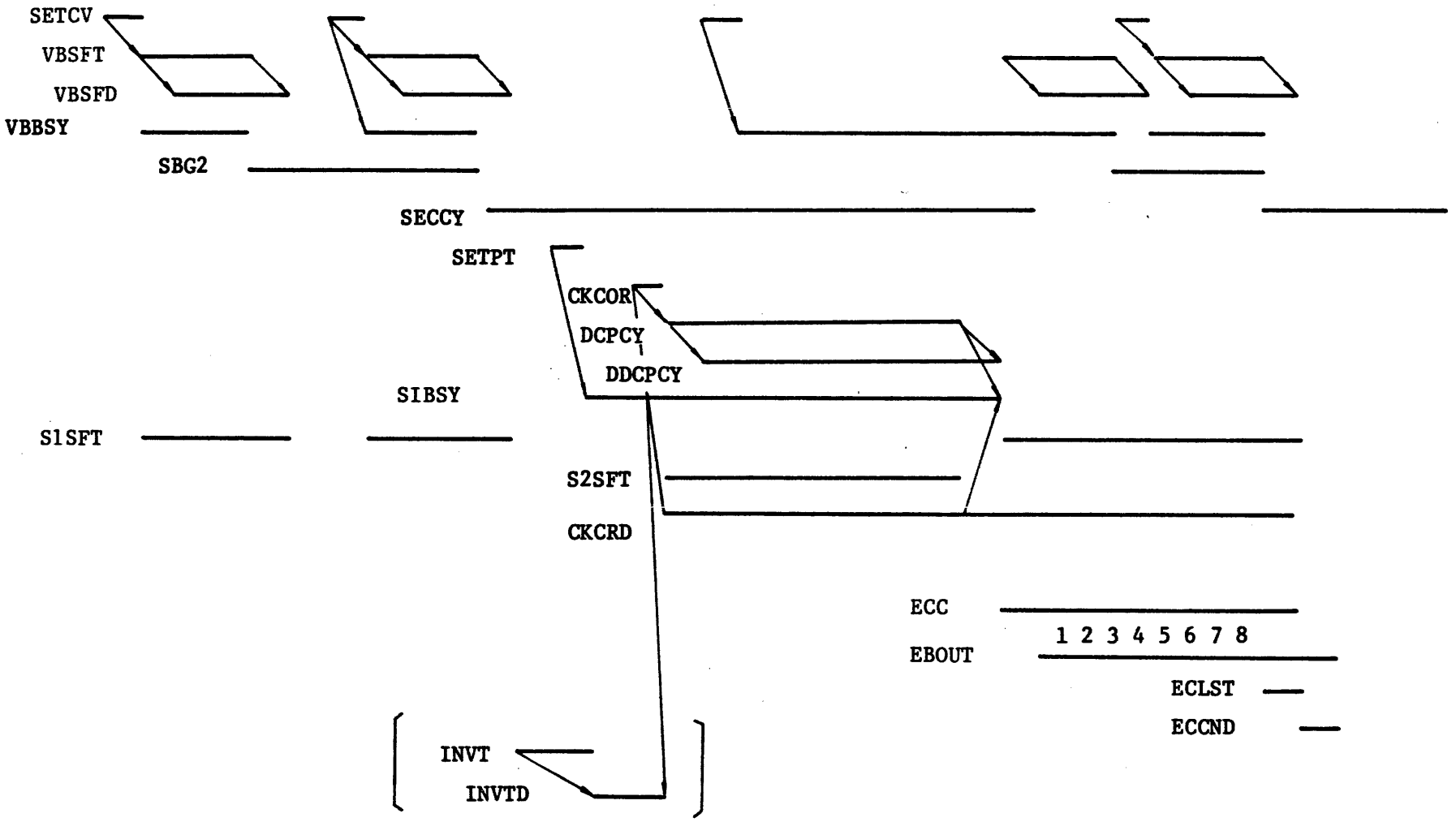


Figure 4.43 6250 RPI basic timing (2 of 2)

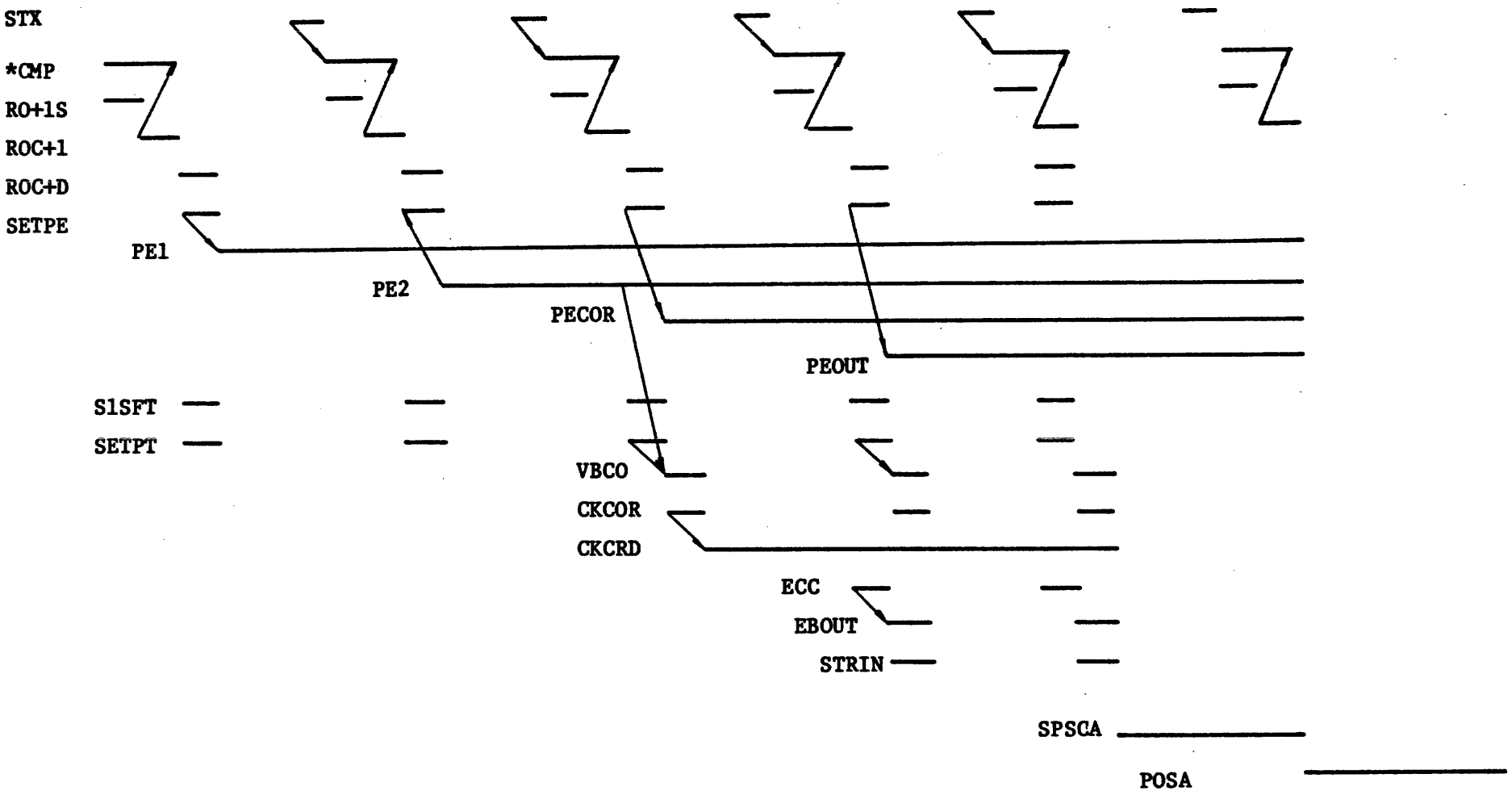


Figure 4.44 1600 RPI Basic Timing

4.9.4 Deskewing buffer

Modulation data is set in the deskewing buffer after synchronization with the formatter clock. The Phase Error detection signal is stored at the same timing as the data.

Data is entered into the buffer trackwise. However, it is read out simultaneously. The buffer capacity is equivalent to 32 bit cells.

The Read In Cycle (RICY) signal will be set after mark '1' is detected and after a series of '1's (for 10 bit cells) in the 6250 mode, or if a 00001 pattern is detected in the 1600 rpi mode. When data is detected after RICY has been set, the Read In CountEr is advanced and the CMP signal of the track is reset. CMP is reset as soon as the Dead Track Pointer is set. The Read Out Counter is activated as soon as the CMP signals of all the tracks are reset.

4.9.5 Skew control

Pointer and skew errors are set in the up/down counter used for indicating the volume of data in the deskewing buffer.

(1) Pointer in 6250 mode Read Command

The Dead Track Pointer for indicating skew of less than 2 bits is set if a track with skew in excess of 26 bits (STMP signal: '1') and seven tracks with skew of more than 4 bits (LAG signal: '1') are detected. If less than 6 tracks are involved (LED: 1), the Dead Track Pointer for skew in excess of 26 bits is set.

(2) Pointer in 1600 mode Read Command

The Dead Track Pointer indicating skew of under 2 bits is set if a track with skew exceeding 14 bits and more than 7 tracks with skew exceeding 4 bits are detected. The Dead Track Pointer indicating skew of over 26 bits is set if less than 6 tracks are involved.

(3) Skew Error

Skew Error is set in the following cases:

1600 mode Write: over 2 bits.
6250 mode Write: over 14 bits.

When skew marginal has been specified, skew error is set under the following conditions:

1600 mode Read : over 4 bits.
1600 mode Write: over 1 bit.

Skew marginal is invalid in 6250 mode.

4.9.6 Error correction

In the 6250 mode, error correction is determined with reference to Syndrome 1 (S1), Syndrome 2 (S2) and the number of pointers.

As shown in Figure 4.45, S1 indicates the parity check status of each bytes. S2 is generated by a logic similar to that used to generate ECC bytes. S2 byte is generated from data byte 7 and the ECC byte.

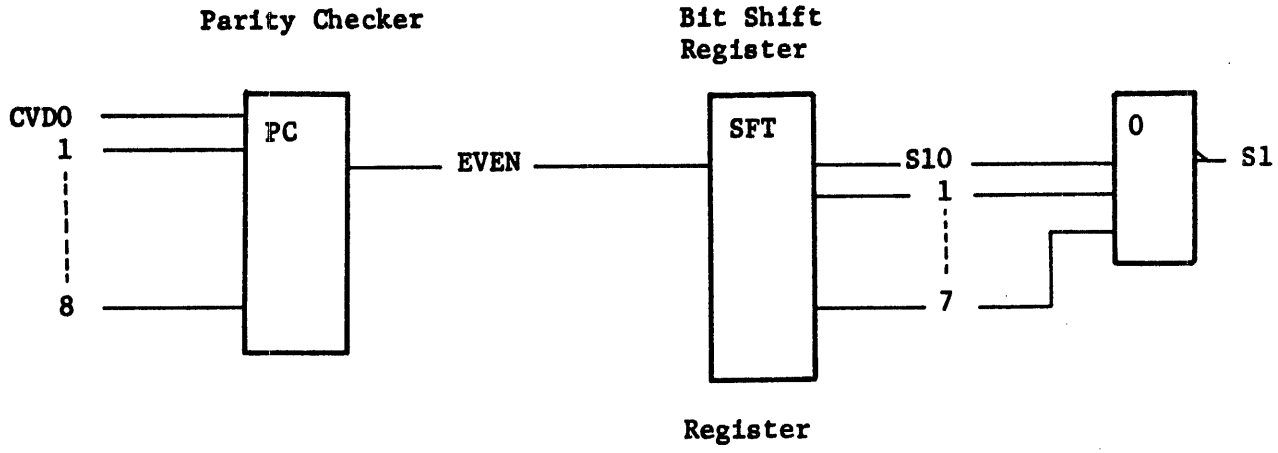


Figure 4.45 S1 generation circuit

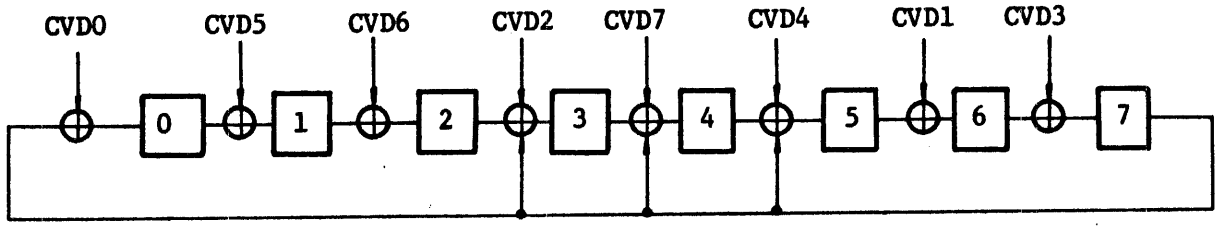


Figure 4.46 S2 generation circuit

The S1 and S2 registers are shifted S1SFT, S2SFT) in synchronization with the convention buffers. All the pointers related to the data group are sampled if the SETPT signal (for pointer set timing) is '1'. Now, S1, and pointers are checked when CKCOR (used for decision during error correction) is '1'. Error correction conditions are listed next.

(1) Write Command

It is not an error when S1 and S2 are simultaneously '0'. However if the pointer indicates more than two tracks, a Multi-Track Error is indicated.

When S1 ≠ 0, S2 = 0 and only the parity track pointer is ON, only the parity track is corrected.

When S1 ≠ 0, S2 ≠ 0 and the pointer of only one track (other than parity track) is ON, S2 is shifted by an amount determined by reference to the pointer track. Then correction is executed when S1 = S2. However if S1 ≠ S2, VRC Error is indicated.

In cases other than the above, data check is executed assuming it to be a VRC error. In this case, when the number of pointers is 0 or 1, VRC Error is set. If more than 2 pointers are involved. Multitrack error and VRC error are set.

(2) Read

It is not in error of both S1 and S2 are '0'. If more than 3 track pointers are set, a Multitrack error is assumed to have occurred. This does not result in data check.

Two track error correction is executed if S1 = 0, S2 ≠ 0 and two pointers are ON.

Parity track correction is carried out in the following cases:

a) S1 ≠ 0, S2 = 0, No pointer
b) S1 ≠ 0, S2 = 0, One pointer
c) S1 ≠ 0, S2 = 0, Two pointers (including parity track).

Two track error correction is executed if S1 ≠ 0, S2 = 0 and 2 track pointers are set (excluding parity track).

If S1 ≠ 0, S2 ≠ 0, and two pointers are 0 or 1; S2 or shifted until S1 = S2. Error track is then identified from the number of shift operations and one track error correction is executed. If S1 ≠ S2 after 8 shift operations. VRC error is set.

If S1 ≠ 0, S2 ≠ 0, and two pointers are set; error correction is executed for the pointer track. If the pointer is 0 or 1 in cases other than the above, VRC error is set. If more than three track pointers are set, VRC Error and Multi-track Error are set.

4.9.7 Pointer

(1) 1600 Mode

There are two types of pointers in the 1600 RPI mode. They are Dead Track and Valid Track Pointers.

a) Dead Track Pointer

- Track in which time sense signal has been reset while PHOK signal is '1'.
- Track with excessive skew.
- Track (read only) subjected to 8 bytes of serial correction with reference to the valid pointer data (this correction is after the valid pointer has been set).

If any of the above three conditions are set, they will not be reset during the processing.

b) Valid Pointer

Normally this pointer is set in a track in which a phase error has been detected and is set unconditionally in Write Operation. It is set during preamble and postamble in Read operation. It is also set unconditionally if other track pointers have been set, but it may only be set in data if parity error has been detected.

Once the valid pointer is set, it may only be reset if 8 bytes (or more) of serial error correction is not executed and the data is changed from 0 to 1 or 1 to 0 (in read only).

(2) 6250 Mode

There are three types of pointers, Dead Track Pointer, Valid Pointer and ECC Group Buffer Pointer the 6250 mode.

a) Dead Track Pointer

The condition for setting this pointer are the same as that in 1600 mode. In Read Operation, if the time sense is '1' when resynchronous burst is detected, this dead track pointer is reset.

b) Valid Pointer

- Track subjected to error correction.
- A track in which an invalid data pattern and mark is not detected in the mark field.

This pointer is set under any of the above two conditions. If a pointer is set in a track in which a dead track pointer has already been set, it will be reset automatically. It is also reset if 8 data groups or more of serial error correction is not performed during a Read Operations.

c) ECC Group Buffer Pointer

This pointer is set if a phase error is detected in a data group to be processed. If dead or valid track pointers of more than three tracks have been set, the ECC group buffer pointer is not employed as a pointer.

In Read Operation, this pointer is reset on detection of resynchronous burst and on completion of processing of a data group. data group.

4.9.8 Data flow

The data deskewed at the deskewing buffer (PD0-8) is set in the sub group buffer when the ROC+D signal (which is a step delayed from ROC+1) is set ('1'). As soon as the five bit data counted by the group counter is set in the buffer, the group buffer full signal (GBFUL) is set.

The five bit output from the group buffer is subjected to 5-4 conversion to obtain 4 bit data.

At this stage, Mark 1, Mark 2, or All 1 mark is detected. The 5-4 conversion data is preset in the conversion buffer at SECTV '1' timing when GBFUL is '1' and the conversion buffer bysY signal (VBBSY) is '0'. The data from the conversion buffer shift signal (VBSFT) is output serially by the conversion buffer shift signals. This CVD 0-8 output data is stored in the ECC buffer by the S1SFT signal (S1 register shift timing signal). This buffer is made up of an 8 bit serial in/serial out register. The ECC register output data is subjected to error correction and then set in the ECC buffer out register. The output data (EO 0-8) from this register is set in the transfer buffer as Read Data when STRIN is '1'.

Read system data flow is shown in Figure 4.47.

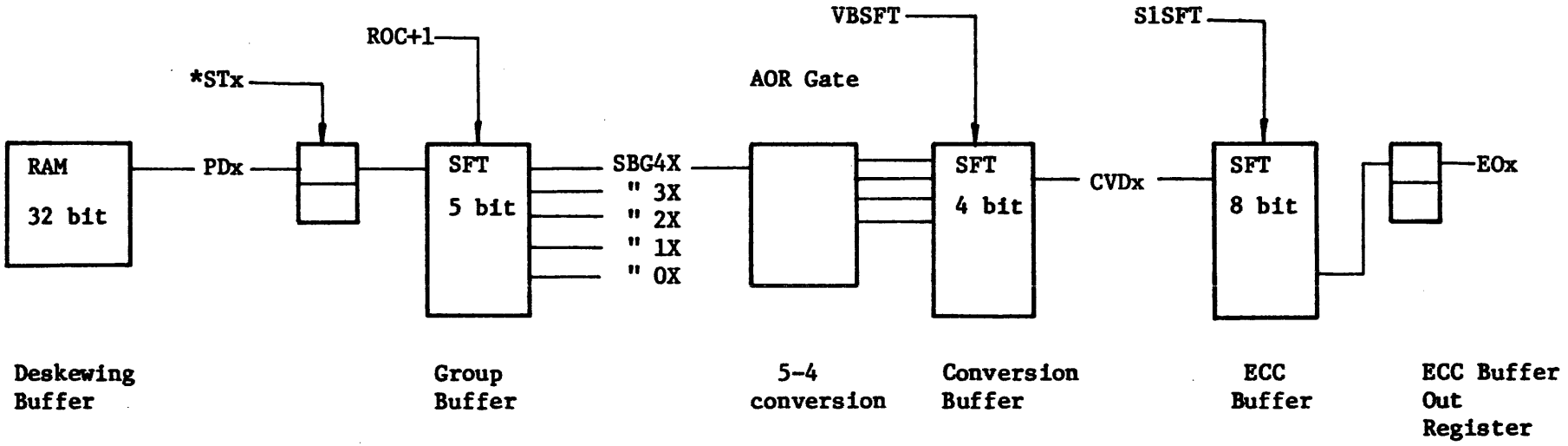


Figure 4.47 Read circuit data flow

4.9.9 CRC check

The following data check circuits are provided: CRCA, CRCB, CRCC, CRCD and CRC. CRCA is generated from the transfer buffer input data.

CRCB is generated from the transfer buffer output data. CRCC is generated from the data and Aux-CRC byte. CRCD is generated from the Aux-CRC byte.

CRC is generated from data, padding characters, Aux CRC byte and one CRC byte.

Details on checks in each mode are given in Table 4.30.

Table 4.30 CRC Check

		6250			1600			800			Error Multiplex or DSB
		WT	RD	BR	WT	RD	BR	WT	RD	BR	
CRCA ≠ CRCB	Transfer Buffer Input/Output does not match	o	o	o	o	o	o	o	o	o	P Compare
CRCB ≠ CRCC	Write Data and Read after write Data do not match				o			o			CRC CRC III
CRCB ≠ CRCD	R/W data and the Aux-CPC Data read out do not match	o	o								CRC CRC III
Unmatch CRC	Required pattern not obtained in Read data CRC Check	o	o	o				o	o	o	CRC
Unmatch CRCC	CRCC generated from Read data does not have the required pattern		o								CRC CRC III

4.10 800 RPI Read Circuit

As soon as ROK signal is set ('1'), the Read data from the MTU is integrated in the Analog circuit and thus converted into a peak pulse (PEKP0-8). An OR of PEKPX of nine tracks is obtained to generate a Read clock signal (RCL signal). It is then synchronized with internal clocks to obtain a RCVD signal.

The 800 RPI circuit internal clock is equivalent to one quarter of formatter full clock. One bit cell in 800 RPI mode is equivalent to 48 clocks. Count is started after RCVD is set to '1'. Sampling pulse (SMPP), skew gate (SKWG), HRCRG, HRCHG and block end (BLKED) is generated by decoding the counter value. In write status SMPP is set ('1') at 33% of the bit cell. It is executed at 48% of the bit cell in read status. If skew is detected and RCL signal is set again ('1') (after TRCD signal) the signal will also be '1' (MLTB signal). In this case, the sampling pulse will slip 9% and will therefore be set (1) at 57%.

Table 4.31 NRZI clock

Tape Speed (IPS)	Clock Cycle (ns)
200	130
125	208
75	347
50	521

Marginal sampling timing varies with TM0-3 specification. HRCRG is turned ON (1) and CRC is set in forward status, if RCVD is not set (1) within a two bit cell period.

HRCHG is turned ON, if the RCVD signal is not set ('1') during 5.33 bit cell period. If this signal or the NSPT signal is set ('1'), the CRC and LRC signals will be reset.

NSPT1, CRC, and LRC signals are synchronized with formatter full clock. STRIN are is set (1) if both LRC and CRC signals have been '1'. At this stage, data is stored in the transfer buffer.

Data is set in the register so that the track (the peak pulse of which is '1') is also set to '1'. EOR of the RAx, output from RA register , and ETRKx (error track register signal set by RTIE command), are set in the RD register when SMPP is '1'. The NRZDx signal from the RD register is stored in transfer buffer when STRIN signal is set(1).

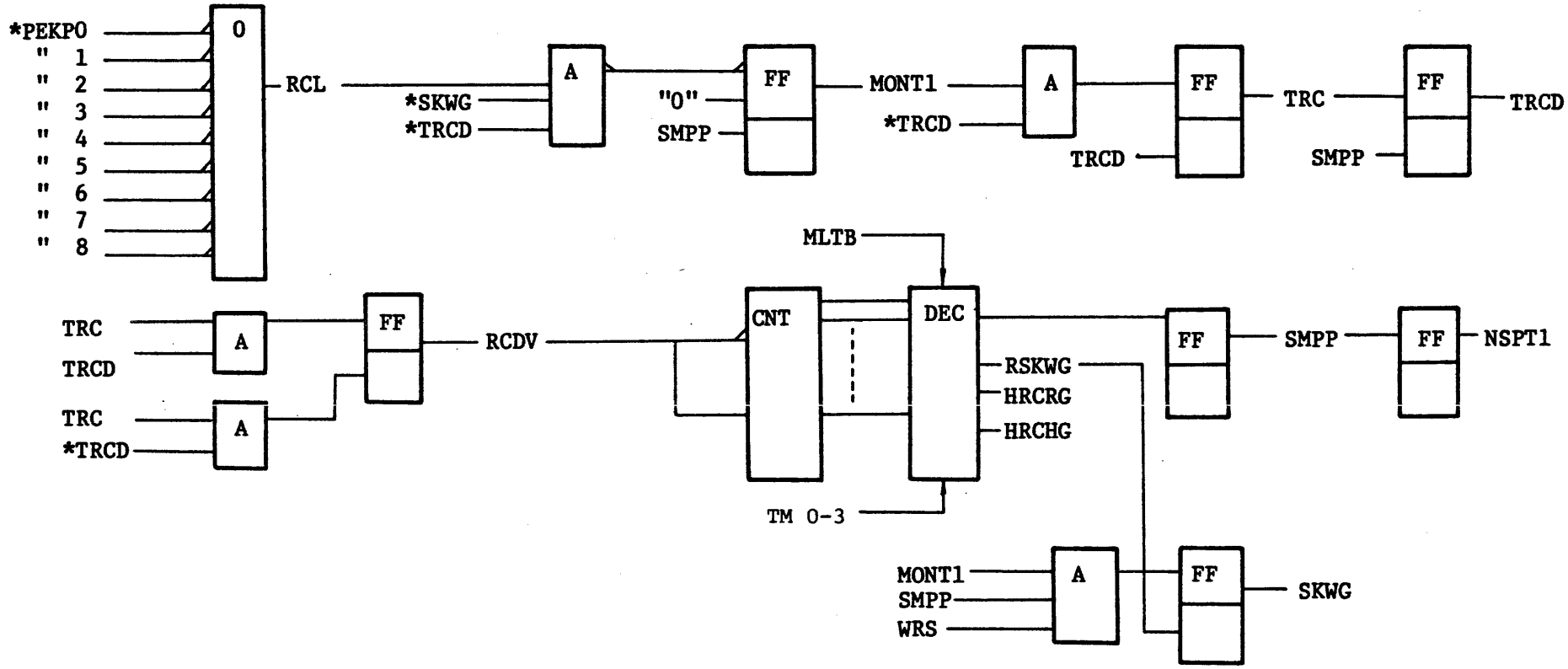


Figure 4.48 800 RPI Basic Circuit

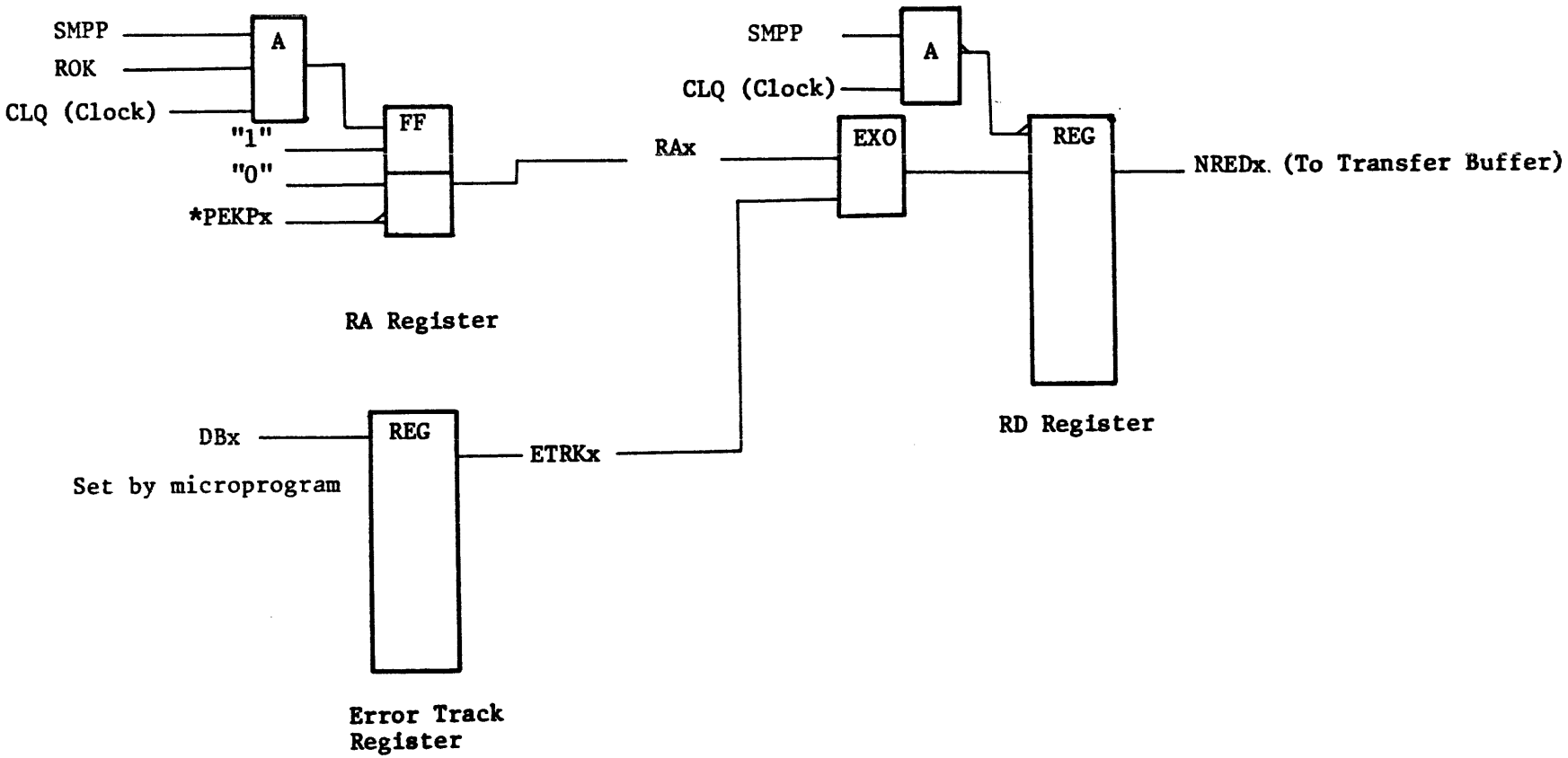


Figure 4.48 800 RPI Read data flow

4.11 Demodulation Circuit

4.11.1 Principle

The peak signal that indicates the position of the peak of the read signal in the MTU is sent to the FMT after being gated by the amplitude sense signal. The peak signal is input to the variable frequency oscillator (hereafter referred to as VFO) and the VFO outputs the reference signal. The phase of this reference signal is compared with that of the peak signal to check the phase difference. The information (1, 0) is then demodulated.

PE and GCR mode timing charts are shown in Figures 4.50 and 4.51 respectively and the block diagram is shown in Figure 4.49

Numbered waveforms in the timing chart represent the waveforms on the signal lines of the same number in block diagrams.

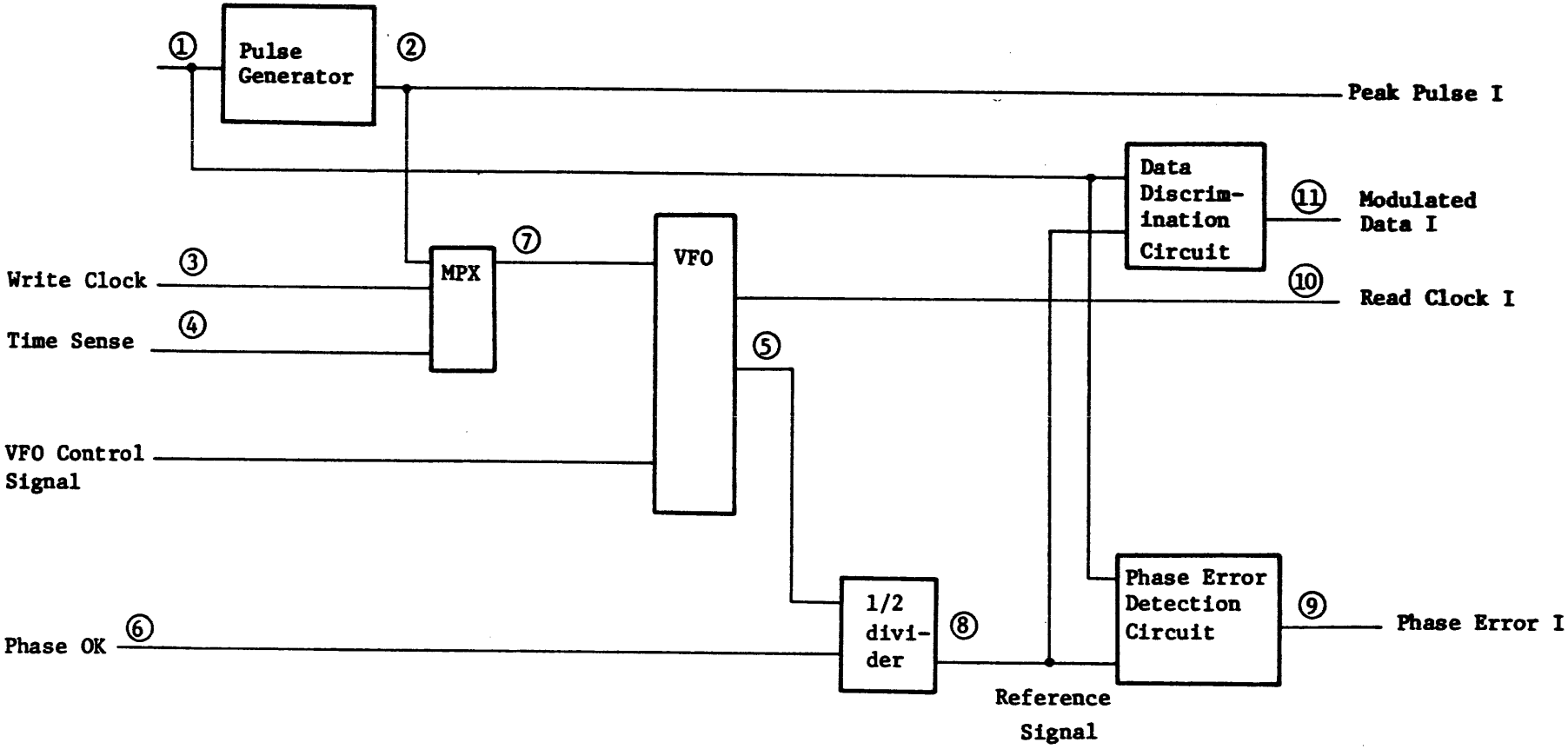


Figure 4.49 Block Diagram of Demodulation Circuit in GCR and PE Modes

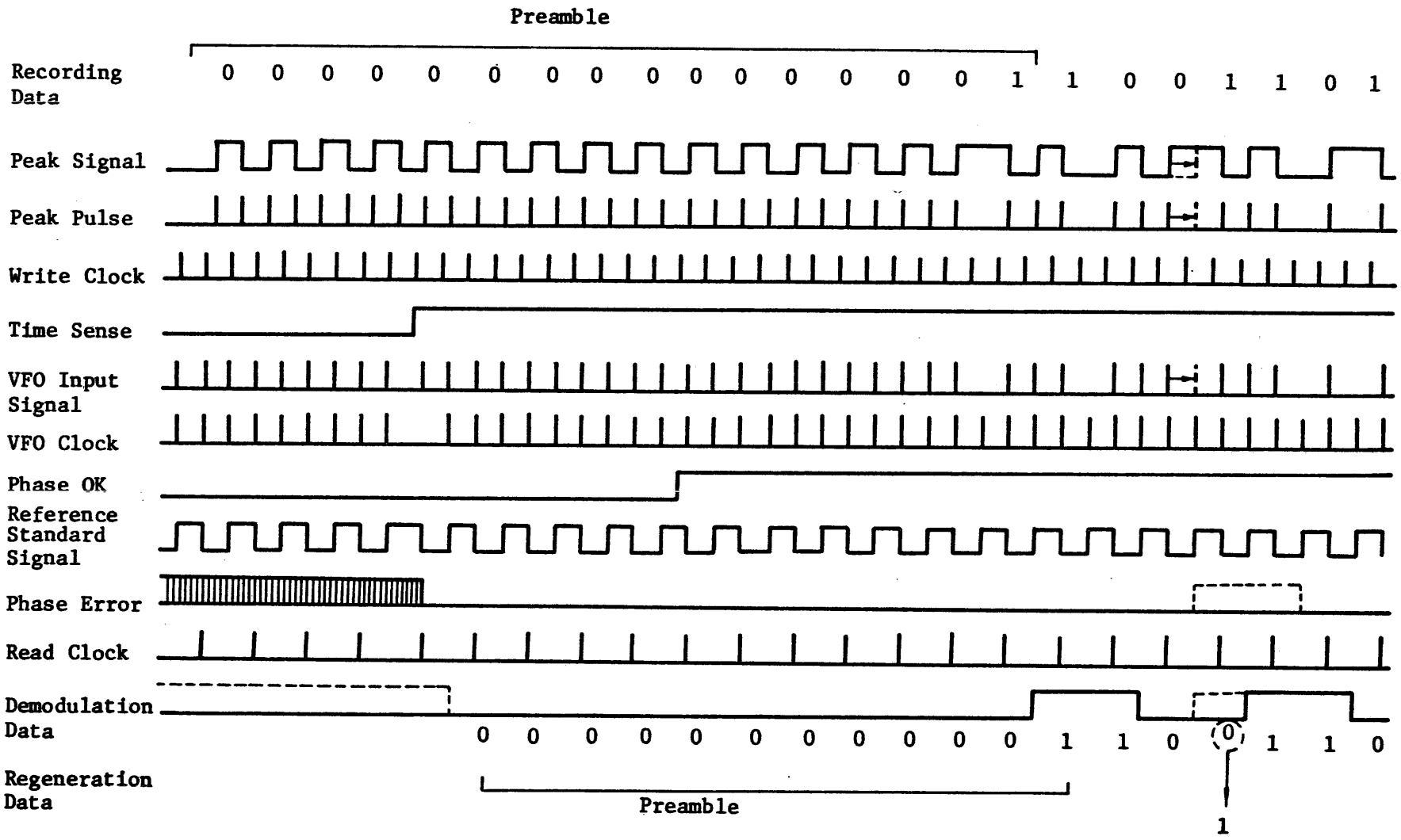


Figure 4.50 Demodulation Timing in PE mode

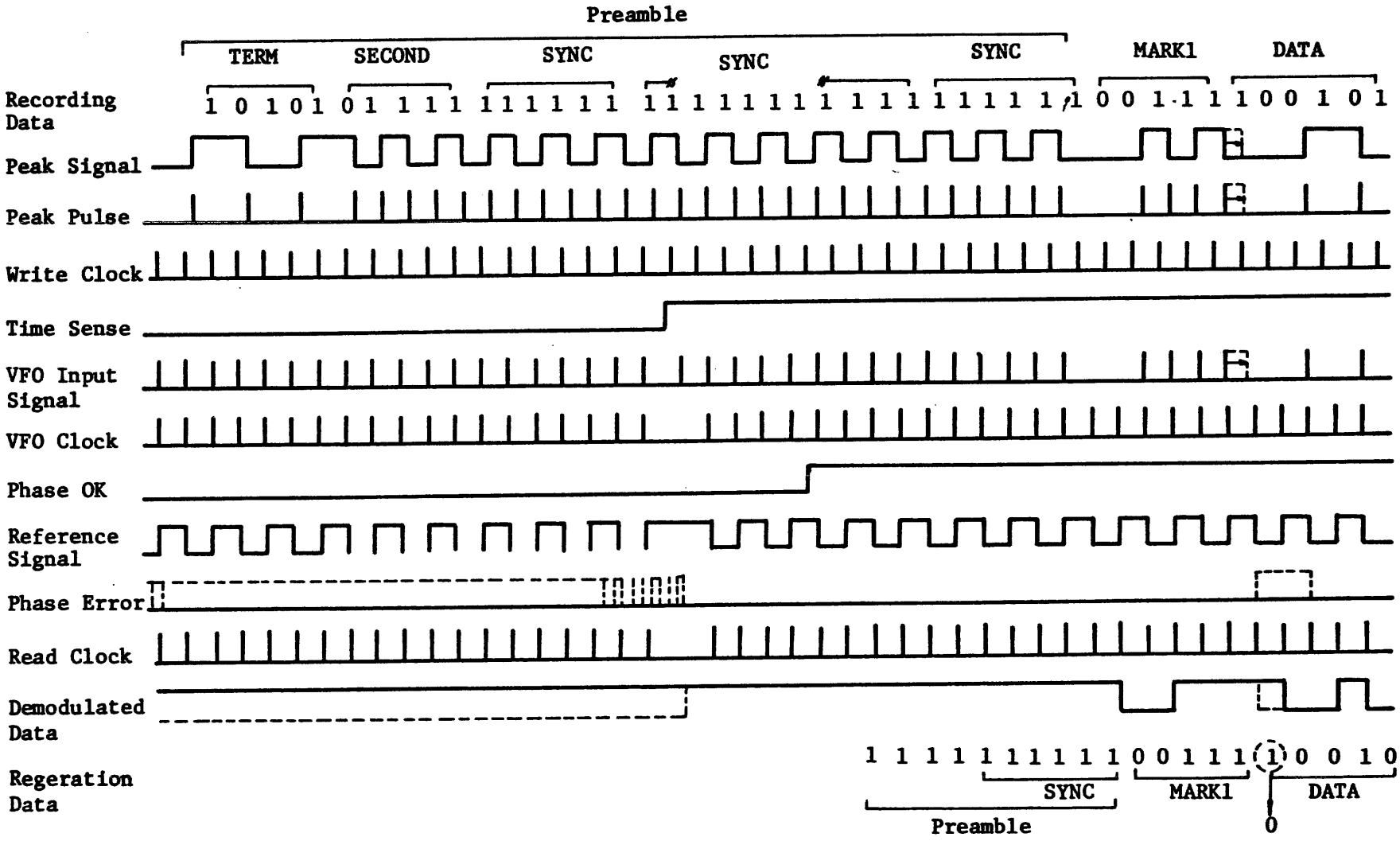


Figure 4.51 Demodulation Timing in GCR Mode

4.11.2 Demodulation circuit signals

(1) Peak Signal 0-8

These signals indicate the peak of read data from a magnetic tape.

(2) Peak Pulse 0-8

Pulse corresponding to the leading and trailing edge of the Peak Signal (1).

(3) Write Clock

Standard clock for holding VFO in a normal condition.

(4) Time Sense 0-8

This signal rises if the peak pulse (2) continues over a specified time period. It is used to alter VFO input signals.

(5) VFO Clock 0-8

VFO clock synchronized with VFO input.

(6) Phase OK

Demodulated data and phase errors become effective after this signal is issued.

(7) Reference Signal 0-8

Signal divided VFO Clock.

(8) Phase Error

This signal indicates that the peak pulse is missing or the phase of Reference signal and that of Peak Signal are remarkably different.

(9) Read Clock 0-8

Clock signal for processing Demodulated Data (10) data.

(10) Demodulated Data 0-8

Data identified by 1, 0 codes.

4.11.3 Demodulation in PE mode

The data in 1600 RPI mode is recorded on magnetic tape in PE format. The VFO is synchronized with the Write Clock (3) in order to adjust the free-running frequency while waiting for data block Peak Signal.

As soon as a data block is detected, peak signal (1) is transformed into peak pulse (2) by the pulse generator and the time sensor generates time sense (4). Then the VFO input signal (7) is converted from Write Clock (3) to a peak pulse (2). Thus the VFO which has been synchronized with Write Clock (3) is sychronized with peak pulse (2), and a VFO clock (5) synchronized with peak pulse (2) is generated. Reference signal (8) is generated by subdividing this VFO Clock (5).

By comparing the phase of peak signal (1) with the Reference signal (8) at each bit cell, the data is identified as "1", "0". The demodulated data (11) is output at the read clock to obtain regenerated data.

Phase error signal (9) is generated if the phases of peak signal (1) and Reference signal (8) are remarkably different due to phase shift, missing bit, etc.

4.11.4 Demodulation in GCR mode

In 6250 RPI mode, the data is subjected to GCR processing and recorded on magnetic tape in NRZI mode. In NRZI mode, '1' represents reversed polarity while 0 represents original polarity.

As in PE mode, VFO generates VFO clock (5) in synchronization with peak pulse (2). Peak signal (1) and Reference signal (8) phases are compared (from the center of a bit cell to the center of the next bit cell) to identify data (1 or 0).

Regenerated data is then obtained by outputting this Demodulated data (11) at Read Clock (10).

A phase error signal (9) is generated if the phases of peak signal (7) and Reference signal (8) are remarkably different due to phase shift, etc.

4.12 MTU Interface Circuit

Interface circuit for interface with an MTU is shown in Figure 4.52.

The interface signals to various MTUs are illustrated in Figure 4.53. The distribution PCA and MTUs are connected by a flat cable. Two types ofdistribution PCAs are available. They are the distribution PCA for MTU cross call (DGBMU), and single FMT (DGAMU). Distributor issused to logically link one of the 8 MTUs and one of the two FMTs. The is selected by DVSEL register, (select tag) and DVAO-2 (device address 0-2) bits. As soon as SLTAG bit is set, the DVAO-2 bits are decoded. Then, HSLNA or HSLNB corresponding MTU is set and a control signal is transmitted. A Selection latch is employed for controlling MTU cross call operation. If an FMT from the opposite side has been selected first, the latch is not set and therefore the control signal is not sent to MTU. This latch also enables MTU reserve/release and online/offline control from the operation panel.

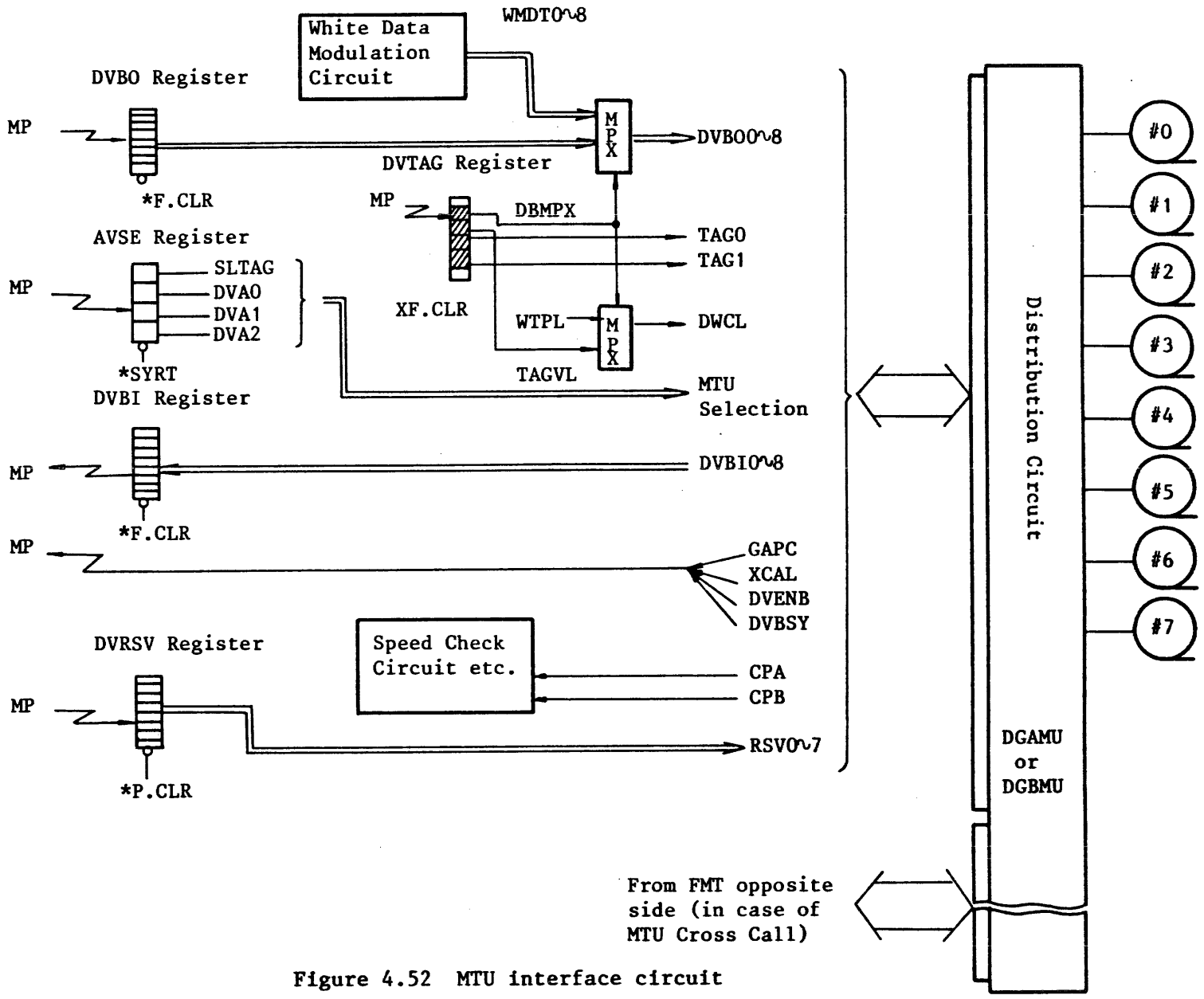


Figure 4.52 MTU interface circuit

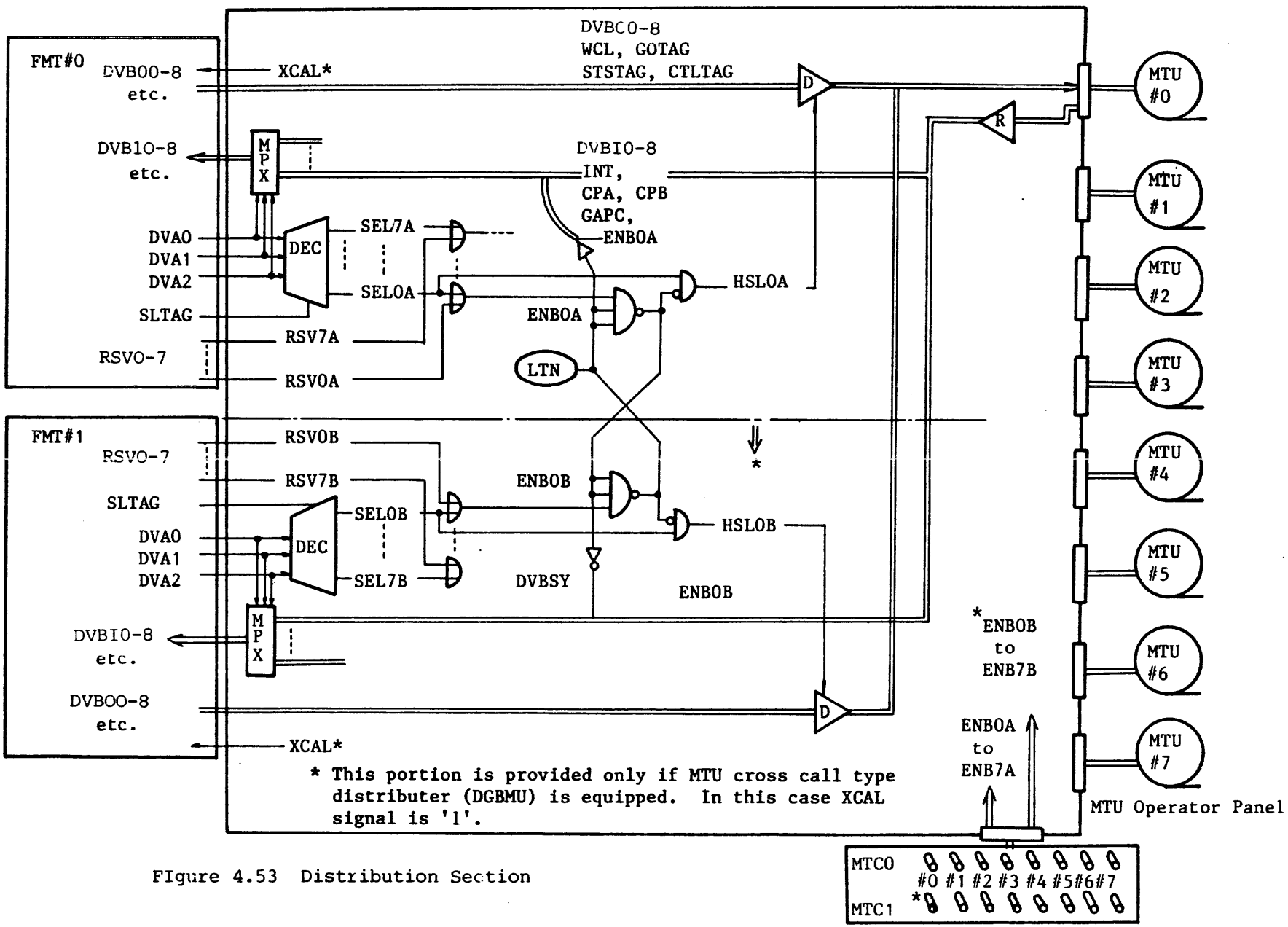


FIgure 4.53 Distribution Section

4.13 Power Supply Section

The FMT power supply supplies the required AC and DC power to the FMT section of the magnetic tape subsystem.

4.13.1 Function

(1) **Acceptable AC power input specification is shown in Table 4.36.** This input power is converted to a stable DC power (+5V, -5.2V).

Table 4.36 Input standards

Item	UL power supply			
Input voltage	200V	208V	220V	240V
Phase	Single-phase			
Frequency	50/60	60	50	50
Input current	3.6	3.4	3.2	2.9
Rush current	25A			

(2) **Provided with an overload protection circuit.**

(3) **Features DC output sequence operation function as well as a warning display for abnormal power supply.**

(4) **Features a power supply control interface.**

(5) **Automatic breaker activated by temperature alarm, etc.**

(6) **Emergency breaking by power switch.**

(7) **Illustrated in Figure 4.54.**

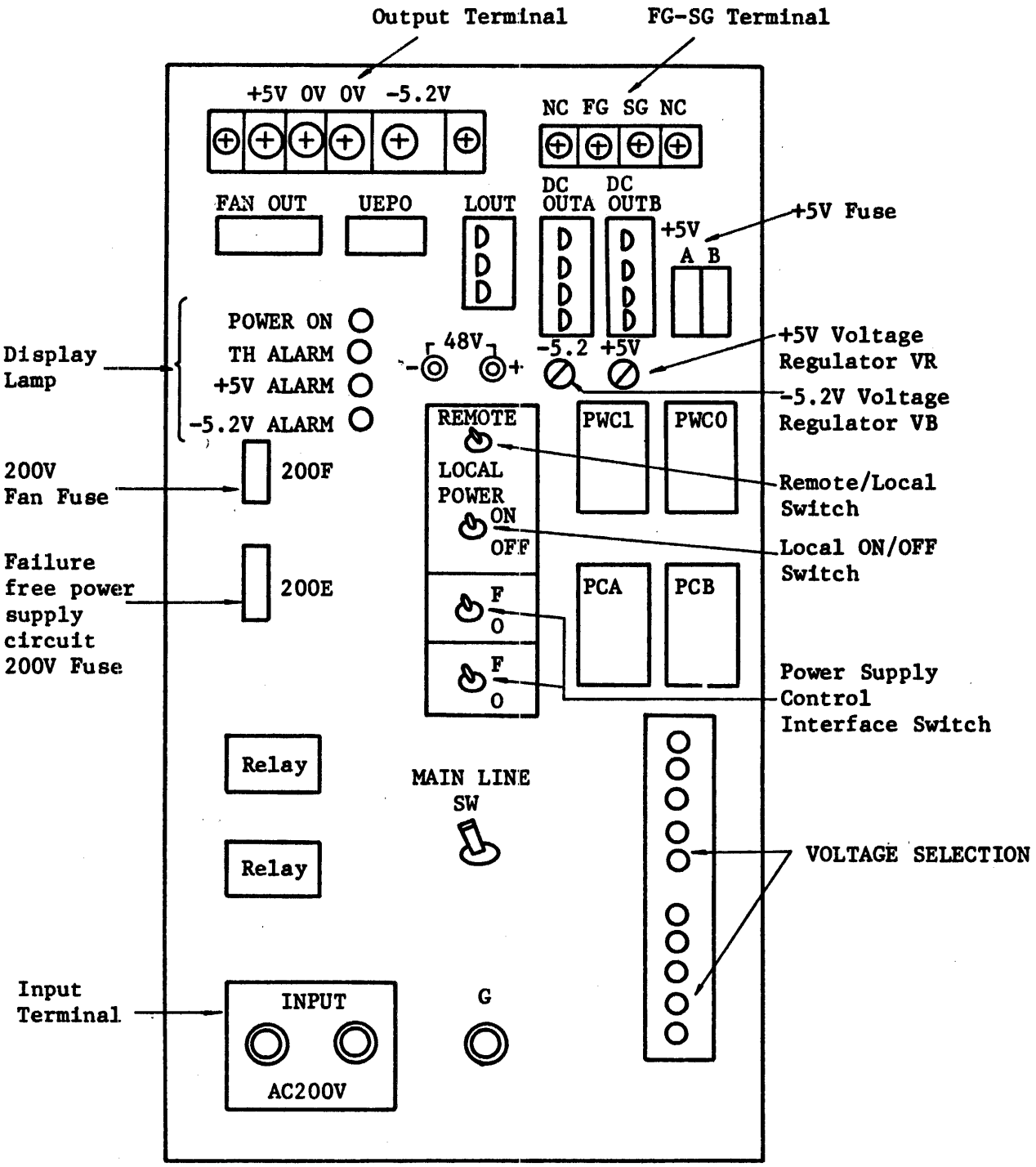


Figure 4.54 External view of power supply operation panel

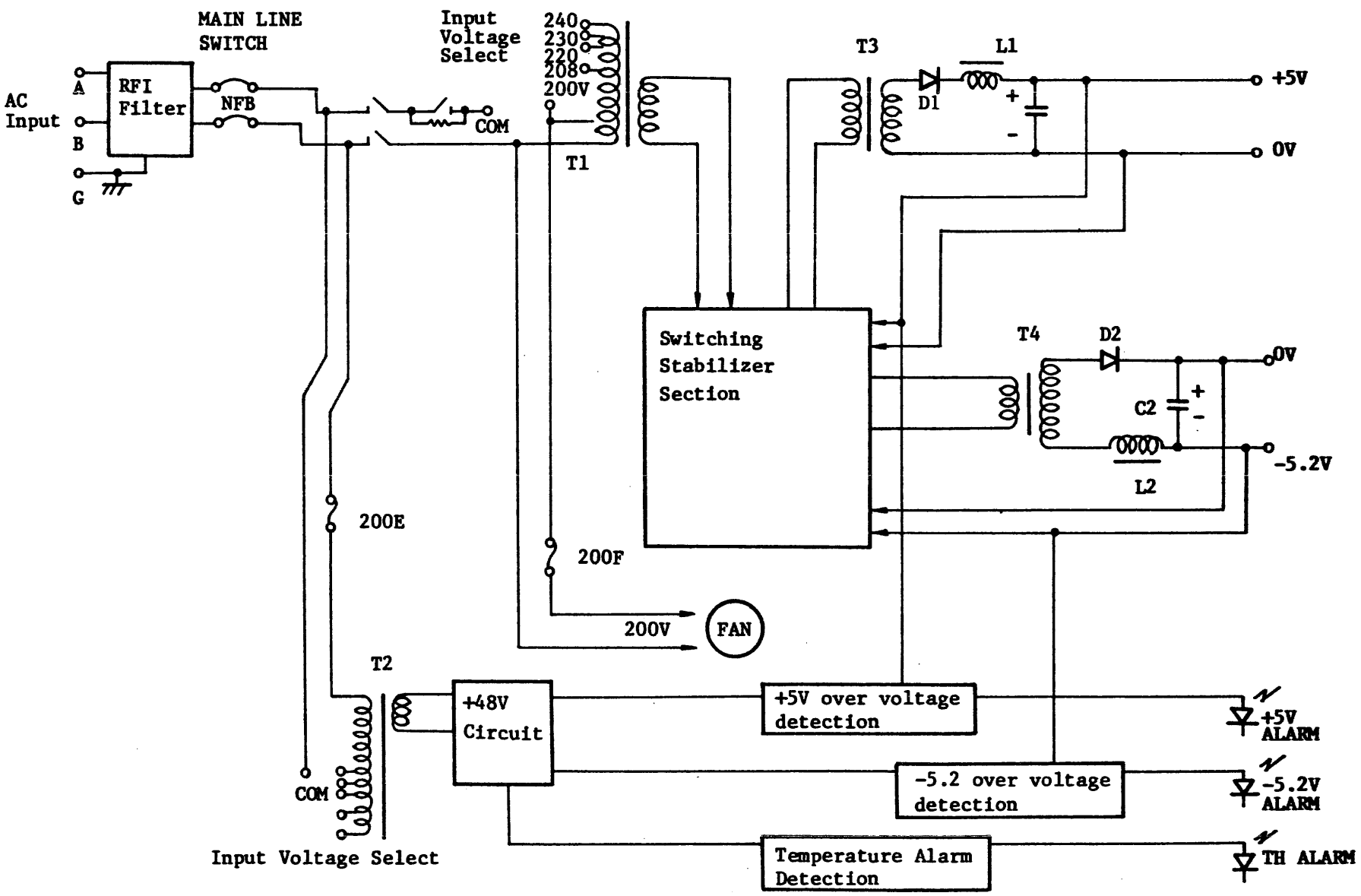


Figure 4.54 Power supply circuit configuration

4.13.2 Configuration

Configuration of the power supply section is shown in Figure 4.55.

(1) +48V Circuit

The input power is applied to transformer T2, then rectified and smoothed to obtain a +48V supply. The +48V power supply is used as failure free supply for driving relays.

(2) +5V/-5.12V Circuit

The input 50/60 Hz is applied to transformer T1 then rectified and smoothed to obtain a DC supply. This DC supply is then switched by the transistor at 50 KHz to obtain a high frequency AC supply. This high frequency AC power is transformed, rectified and smoothed by T2 and T4 to obtain +5V and -5.2V supply. The output voltage is stabilized by feedback to the above switching section to meet load fluctuations in +5V, -5.2V supply.

4.13.3 Power ready signal

This power supply section generates PRDY signal to be sent to FMT for resetting. The timing chart of this output signal is shown in Figure 4.56.

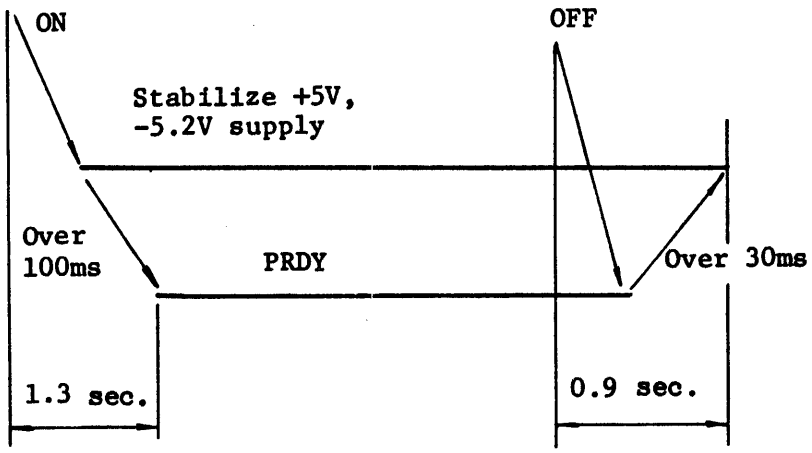


Figure 4.56 Power ready timing

CHAPTER 5 MICROPROGRAM

5.1 Outline

The FMT microprogram is described in this chapter. It controls all FMT operations. The signals and bits handled by the microprogram are the LSR and EXR described in section 4.5. For the purpose of description in this section, it is assumed that the read is familiar to a certain extent with the hardware and the magnetic tape control unit.

The overall microprogram is shown in Figure 5.1. The microprogram starts from address '000' (hexadecimal) in the folling cases: power supply is turned ON, system reset from the Controller, field tester panel ON/OFF switch operation, ect. At this stage, the program executes the self test rountine, followed by the reset rountine. As soon as all the reset procedures are completed, the subsystem enviroment us checked by the SETUP routine and the system is initialized. Next, as device scanning is completed by the device scan, routine, the system becomes ready to receive commands.

At this stage, the FMT goes into as idle status until the Controller starts. As soon as this sequence is started, as INS trap is generated and the initial status is checked by the initial selection routine.

At this stage, if commands are ready for execution, command operation is performed by the MCY group of routines.

On completion of command operation, sense data for DSBs and Error Multiplex bytes are generated in the states handling routine, then the FMT transmits an end status.

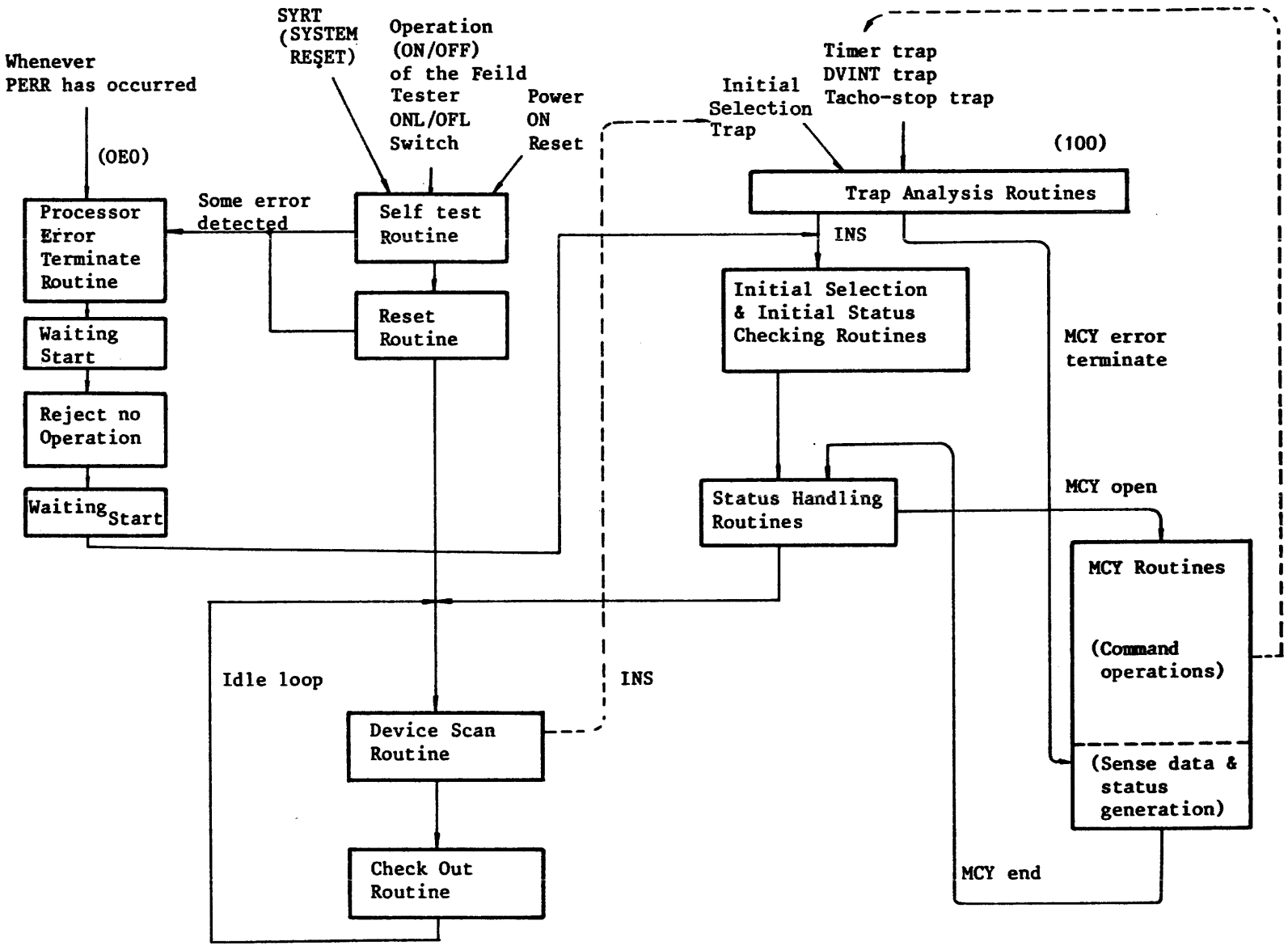


Figure 5.1 Microprogram Structure

5.2 Self Test Routine

This routine is provided to confirm normal operation of the processor prior to starting microprocessor control..

(1) All commands are attempted in the test (various combinations of OP code and EOP code field).

(2) Tests on the hardware related to the processors.

(3) Tests source register address field, destination address field, immediate data field, etc. by altering the field values to confirm normal detection of address line, register address line, processor write bus, and processor read bus.

(4) Tests all ALU operation codes, branch codes, etc.

(5) This test routine confirms error mode which affects only processor hardware. This test is so designed that EXR is used and registers using LSR are limited to a minimum.

(6) Carries out tests starting with basic branching systems through complicated systems command (systems which involved extensive hardware).

(7) This routine displays the errors thus detected on FRU (DSB 14,15). However Processor Error sequence is employed for the following operations in on-line mode.

5.3 Reset Routine

The conditions for execution of reset routine and its operation is shown in Table 5.1.

(1) After a reset operation is initiated the FMT will wait for the initial selection request from the Controller.

(2) If the microprogram detects an error during reset cycle, the cycle is aborted and the FMT waits subsequence initial selection.

(3) Power ON Diagnose Routines execute the following tests:

a) Write/Read tests with specific patterns to LSR.

b) Scan In/Scan Out test for all LSI's.

c) External register bit ON/OFF test.

d) Timer function Test.

Table 5.1 Reset Routine Execution Conditions

Operation destination \ Cause	Power ON	Field Tester ONL ↔ OFL	Interface System Reset
Inquiry Register 00; DVENQ#0 07; #7	Resets all the inquiry flags about all MTUs.		
Command sequence memory 09; SCANP	Resets the flags.		Resets the flags
MTU Reserve RSV, 0 7 DVRSV	Releases the all MTU reserved from the FMT.		
Sense hole of MTU	Resets all MTUs, except the MTUs that cannot be selected by the FMT (MTU's linked to other FMT).		
High speed mode of MTU	Not Changed		Not Changed
Sense Byte Stack Area	Cleared		Cleared
Diagnostic Flag Byte Stack	Cleared	Not Cleared	Not Cleared
Off Line Service Control Register	Cleared	Not Cleared	Not Cleared
Power on Diagnose Routines	Executed	Not Executed	Not Executed
Other LSR	Cleared		

5.4 Device Scan

This routine Scans the status of the MTU and updates the contents of MTU status register file. Then each bit of Device Inquiry Reigster and MTU status are compared, SSC is asserted if necessary.

(1) M.INS is reset and microprogram interuption of command initiation is suppressed from the period of setting the device select bit to the completion of updating of the device status register file and inquiry register. During this interval, command start is recognized by INS in a microprogram step.

(2) If a command start is indicated, the microprocessor will trap immediately and then the Initial Selection Routine will be performed in the interval of M.INS being ON.

5.4.1 Device Inquiry Registers

Device Inquiry Registers are prepared one byte for each device address. These are DVENQO- DVENQ7

Table 5.2 Device Inquiry Register

Nick Name	Name	Description
BINQ	Rewind Inquiry	This bit is set when the FMT ordered a MTU to rewind, and reset when SSC line is reset at the device address. When this bit is ON, rewind operation has been initiated at MTU and now the MTU is busy or ready but the SSC line is not reset. In a two FMT type, the MTU is reserved by the FMT until BINQ is reset.
SINQ	Skip Inquiry	This bit is set when the FMT ordered a MTU to space a file or to backspace a file. (Only a MTU which has SKIP FILE feature.
DINQ	DSE Inquiry	This bit is set when the FMT ordered an MTU to perform Data Security Erase. SINQ and DINQ are the same as BINQ in the reset condition.
SSCM	SSC Memory	This bit is set when the SSC line is asserted and reset when any command except a NOP, SNS and DMS command is issued to the MTU which SSCM has been set. This bit is used to reset the SSC line. The SSC line is reset when all SSCM bit are reset.
USEM	Used Memory	This bit is set when a command is issued to the MTU which is used by another FMT. (Reject Code 101). This bit is reset when the MTU is free.
ONLM RDYM	Online Memory Ready Memory	These two bits are the MTU status. These are updated the Device Scan Routine and when BINQ, SINQ or DINQ are set.

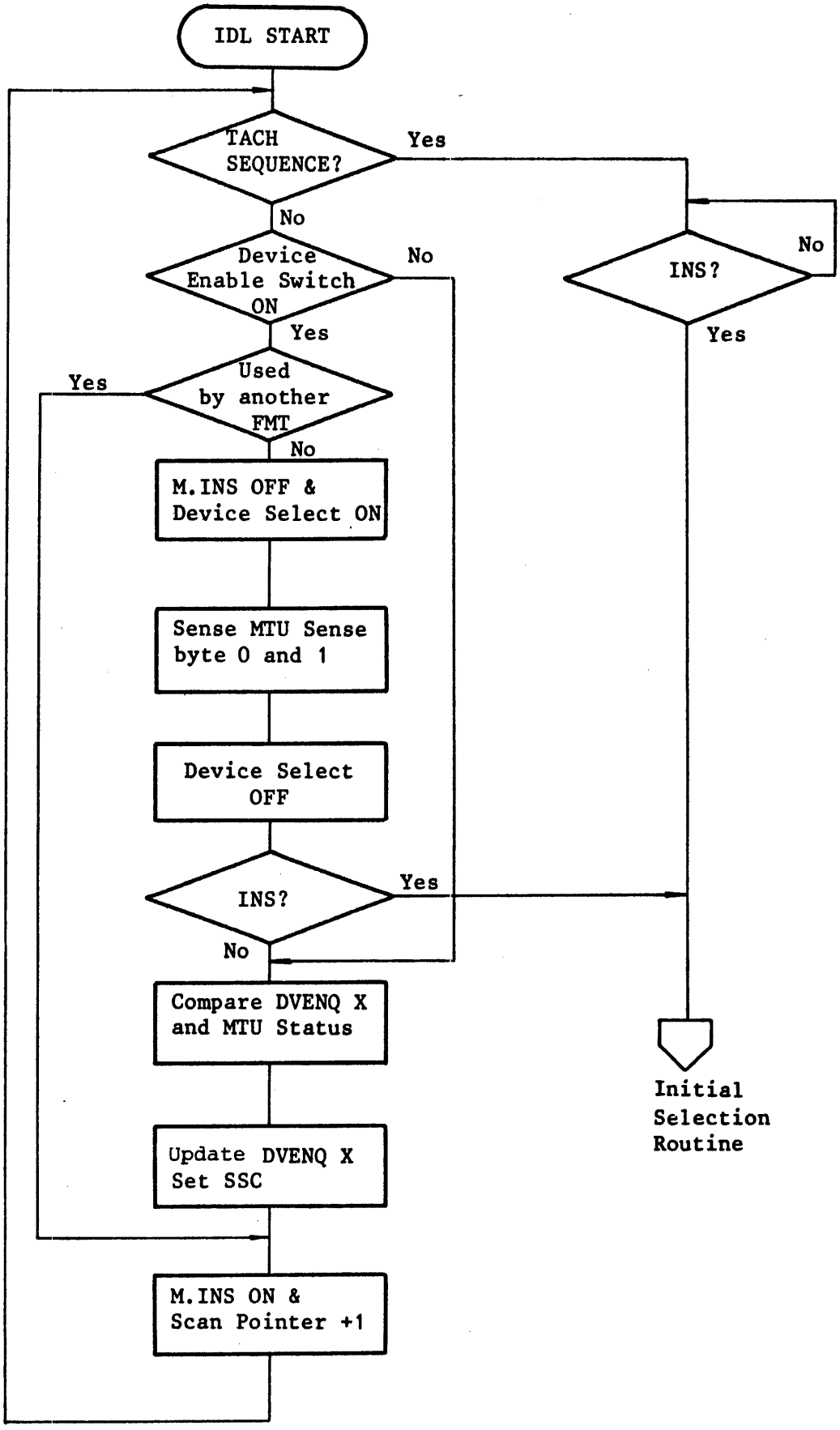


Figure 5.2 Device scan routine

5.4.2 SSC signal

SSC signal is set under the following conditions in the Device Scan Routine.

(1) DVBSY signal is not ON when USEM bit is asserted.

(2) There is a difference between RDYM/ONLM and the current MYU Status

5.5 Initial Selection

After the FMT recognized a command initiation by an INS trap or by checking INS signal, Initial Selection Routine checks the status of the FMT and the MTU to be selected, and determines if a command can be executed.

When any command except a NOP, SNS and DMS command is issued, FMT status, pending sense data, and SSCM bit of the MTU are reset.

When any command except a NOP, SNS, DMS, CLR and LWR command is issued, the MTU status is checked. If the MTU is not ready or used by another FMT, the Reject line is asserted.

If the selected MTU is ready, the FMT checks the MTU status and FMT condition for each command respectively.

5.6 Status Handling Routine

After Initial Selection Routine in NOP, SNS, DMS and CLR command, or after a Machine Cycle Routine in another command, this routine is performed to generate and the status of the command.

Error Multiplex bytes are generated from sense byte stack registers. (SB0 - SB23, RJC Register)

FMT status is generated from DSB registers and sense byte stack registers.

MTU status is sensed in this routine, so indicated status is the status after command execution.

Error Multiplex byte 3 indicates any of the DSB0-DS15. The number of DSB is decided according to the value of the SNSCNT (SNS-NOP counter) register. Contents of DSB0-DSB15 are the end status of the MTU and the stacked sense data of the FMT.

DSBs are updated only during this routine. DSBs are not changed until next command end status.

5.7 Machine Cycle

In this cycle, a command is executed for the selected device and the result is set in the device status byte. MCY remains '1' while this cycle is executed.

The Format Clock should be set depending on the tape speed and the mode of the selected device.

5.7.1 Command operation in SDIA, LWR

Diagnostic flag bytes for SDIA commands are received using a M.SVI bit by the Microprogram which accepts the 4 byte data into SDIA0-3 registers. When GDT flag is specified, a time delay from 50μs to 3.3 sec (approx.) can be elapsed. The time delay is determined by the status of flag bytes 2 and 3.

The LWR command sets the LWRFMT bit and executes a write operation. Write data is returned in the PCA of TUIF without moving tape. The data thus returned is received as read data.

All the error checks except slip check, (like slow begin, slow end, and early begin check) are the same as in Write command.

5.7.2 Command operation in REW, UNL

When REW or UNL commands are started, the write Error Count is reset. If the preceding status is a Write Status, a fixed length (additional erase) erasing is executed. The REW command sets the BINQ flag bit and reserves the MTU. UNL command sets the DINQ flag bit and reserves the MTU.

5.7.3 Forward type commands

This type of command includes the WRT, WTM and ERS commands as RD, SP and SPF commands. The former are Write type commands while the latter are Read type commands. If any of these commands are received at the beginning of tape (BOT), they are executed after BOT processings (IB, ARA, etc.). If a Write type command is received at a point other than BOT while the MTU is in Read Status, these command are executed after positioning.

WTM command writes the tape mark after erasing a fixed length.

In WRT type commands, a velocity retry procedure is executed (after receiving GAPC signal) and then WOK is set for the required Write operation. In Read type Command, the tape is moved by 20 QTP in the same direction and then ROK is set for executing the Read operation.

5.7.4 Backward type commands

Reject and Reject Code 023 is generated if BRD, BSP and BSF commands are received on BOT.
If a Backward type command is issued to a MTU in the Write status, the required operation is carried out after erasing the fixed length (additional erase).

In these commands, the tape is driven through 20 QTP, before setting the ROK signal.

5.7.5 Positioning

When a Write Command is issued to a MTU stopped in backward status or forward status, the area to which data is to be recorded is erased by the erase head as follows.

The MTU is set to backward status. Then the Write head is moved backward to a point to cover the entire length to be erased by the erase head. Next the device is set to the erase status and an erase operation is carried out with the erase head only up to the data to be retained. The device is then set to the Write status and a short erase is executed by the Write head or erase head. This erase is carried out so that the erased length is slightly longer than normal IBG. Then a block write operation is started.

5.7.6 Velocity retry

This feature is provided to confirm that the tape speed has reached the required level prior to starting a Write operation in WRT or WTM. Tach pulses are counted after GAPC in order to assure normal IBG.

If the tape speed is not normal, velocity retry is repeated up to the specified count. In this case, sense data velocity retry is set However this does not cause data check.

If the speed has not reached the required level even after the designated retry count, velocity check and equipment check are set and Write operation is not executed. Tape speed is continuously measured by the SPOK signals during a write operation

5.7.7 BOT processing

When a Write type command is received at BOT, recording density is determined by the Density Select Lines (SCMD Register) and the MTU model. Then the recording density identify burst is recorded.

If the SCMD register is in conflict with the MTU model or FMT option, the write operation will be carried out in a higher recording density.

In case of Write type commands, the tape is moved back in the fixed length. The status is then changed to Write status and the length is erased by Write Head or Erase Head.

IB is then recorded in the length of 15 cm. In the 6250 RPI mode, only bit 1 is recorded. Only bit 8 will be recored in the 1600 RPI mode. All other bits are masked in both cases. All bits are masked in the 800 RPI mode.

If ALlWT, IBW and WOK bits are set by the microprogram, a write operation **will be executed in 3014 FCI** (repetetion of '100) in the 6250 RPI **mode, and in 1600 FCI** (repetetion of '10) in the 1600 RPI mode.

In the 6250 mode, GO is released and SAGC is specified to the MTU as soon as WOK is released. Then ARA burst (all '1's) is recorded in all the tracks for a length approx. 15 cm. This is following by ARAID burst for approx. 5 cm. The MTU starts processing after the specified time delay when SAGC us specified. As soon as SAGC check is generated, the DVINT signal is set ('1') and the microprogram is trapped. After the trap recording, Write processing is termination and the tape is stopped. At this stage, ID Burst check and SAGC checks are set as sense data.
GO tag is reset upon completion of IB, ARA, and ARAID processing.

Both the FMT and MTU are set in 1600 RPI mode and driven in the forward direction when a read command is to be executed. When the Read Head reaches a point approx. 43 cm before the BOT mark, ROK is is set and IP an read operation is commeneced. The microprogram checks the time sense signals of all the tracks. The program detects IB when the time sense of a particular track remains '1' for a particular length.
Both the FMT and MTU are set to the NRZI mode if IB is not detected. However, the Reject Line will be set if the MTU model or FMT option does not allow setting of this status. (Not Capable)

Reject Code 111 is also set if GCRIB is detected without a 6250 TU. In all other cases, after the tape is driven forward by 7 cm from the BOT, GO TAG is reset, and SET SAGC is specified to the MTU. Then GO tag is set again and a check is made to determine if DBOB is detected (after approx. 3 com passing). During this period, the MTU executes a SAGC operation. If the SAGC check is generated, DVINT signal will be set. At this stage, the microprogram sets the trap to stop the tape and execute a retry. The FMT may retry and ARA Reading for up to three times. An IB read operation will be resumed again after Rewind is executed and after the MTU becomes ready on detection of Bot. If DBOB has been detected when retry limits, SAGC check and MISC DATA Error is set and DCK is generated.

If DBOB signal has not been detected, Reject code 124 and SAGC checks are set and Reject is generated.

The FMT is set to the 6250 RPI mode when set SAGC is specified.

If an IBG is not detected within a designated period after PEIB or ARA **burst, Reject Code 034 is set, and Reject is generated.**

5.7.8 Read operation

As soon as the RD and BRD commands complete preprocessing, GO tag is set, the tape is moved for 20 QTP in the same direction, DBMPX bit is reset ('0'), all '0's are set in the DVBO register, not zero threshold status is specified, and ROK is set, STPHK signal is also set in the 1600 or 6250 modes. If HBLK is detected, the data block is assumed to have been detected and DXFI is set.

At this stage, all '1's are set in the DVBO register and zero threshold is specified for the MTU. If the Dbig signal is found prior to detecting the preamble, a partial-record-check error will be set. If the SRDC signal is set prior to detecting preamble, a start Read check error will be set.

If SRDC is set prior to detecting preamble, a start Read check error will be set. If DIBG is set after preamble is detected but before PHOK is reset, a partial-record error will be set. Zero threshold will be specified when PHOK signal is reset ('0'). At this stage the system waits for DBIG. If EDCK signal is set before DBIG, postamble error will be set. In the 1600 rpi mode, end-data-check is set in addition to the above. If all the above checks turn out to be normal, ROK is set along with the Go tag. Crease check Operation is executed if an error is detected.

If HTM and DIBG are detected prior to HBLK, UEX is set and a crease check operation is executed. If HBLK is detected during this process, it is assumed to be a data block and DXFI is set. (cancel tape mark block)

The SPF and BSPF commands exexute a crease check operation after detecting HBLK, Processing is same as that in a RD command operation when HEM is detected.

During SPF and BSPF commands, the tape is driven until DTM is detected.

In a forward type command, if HTM or HBLK are not detected within 20 m, a tape-overrun error is set, and Reject Code 025 is generated.

In the 6250 RPI mode Backward Command, if BOT is not detected within the specified length and the trap is not set (after DARA signal has **been detected), Reject signal and Reject Code 115 will be set. The tape is stopped and Reject is asserted if when BOT is detected.**

5.7.9 Crease Check

This check is executed if a block format error is detected during RD, BRD commands and if HBLK is detected during SP, BSP commands.

When DBIG is detected due to tape crease, etc., the tape should be moved to a correct IBG.

In the BSP command following the WRT command, the tape is moved until detecting IBG (continuous DBIG signal of approx. 5 mm in the 6250 mode and approx. 7 mm in the 1600 mode). In this case, the tape may have passed IBG. Therefore, the tape is run back through a few TPs and the head is stopped at a midpoint in the IBG. In all other cases, the crease check is carried out for approx. 2 mm. In this case, IBG is confirmed duringf MTU-stop-delay.

5.7.10 NRZI Read

If it is not a tape block, data transfer request will be issued. Identification of data, CRC and LRC bytes are performed gy the hardware.

5.7.11 Write operation

After detecting a GAPC signal, (also may execute a velocity retry), WOK is set and the write processing is started.

First the timer is set to the tachopulse count mode. Overflow of this timer can occur if WOK is not reset (0) within 15 m.

If HNOIS is not set within 70 QTP after WOK has been reset, a No-Block-Detect error (Reject Code 037) is set. After detecting HNOIS, the microprogram will wait for PREA signal ('1'). If DBOB is reset before PREA, STRDC is set (1). Start Read Check is set in this case.

If DBOB is reset after PREA but before POSA, a partial-record error is set and the Write operation is terminated.

The postamble error will be set if DBOB is reset after POSA bu before EPOSA, or if EDC is set after EPOSA by before DIBG.

On completion of a Write operation, if SLIPC has been set, a Slow Begin Read Back check will be set. On the other hand, an Early Begin Read Back Check will be set if NOISC has been set.

All the tracks are masked and the tape is stopped if a format error is detected during Read Back checking. Also, envelop check and IBG detect is set in ghe sense data.

5.7.12 Write tape mark operation

During a write tape mark operation, WTM, ALlWT, WEC, and WOK bits are set for 18 QTP (378 bit cells) in the 6250 mode and for 36 QTP (126 bit cells) in the 1600 mode. Bits 1, 3, and 4 are masked and the tape mark code is recorded.

A check is thn carried out to make sure that HTM is detected within 70 QTP

Here the retry operation is done up to 7 times, if an error is detected. In case of Retry Over, Write Tape Mark Check and Reject and Reject Code 137 are set.

In the 800 RPI mode, the two bytes of tape mark code are recorded by the hardware. Bits 0, 1, 2, 4, 5 and 8 are masked, and the WTM and WOK bits are set for this purpose.

5.7.13 Sense data generation

All the hardware bits related to execution of the WT, LWR, RD and BRD command are checked. Then the appropriate sense bits for the recording density and commands (as shown in Table 5.3) are set in the sense byte stack area (SB0-SB23 Register).

Table 5.3 Summary of sense generating (1 of 4)

Register Bit	Check Description	6250			1600			800			Consequent Sense Bits	Note -(): Release Check, +(): Additional Check
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
BUSPE	(Bus out parity check) Parity Error in Controller Data	o			o			o			BUSER	+(XBIC) + (WBOC) +(CRC)
	Parity Error in the feed back		o	o		o	o		o	o	BUSER	
ABRPC	(A/B Reg parity check) Parity Error in Send Data		o	o		o	o		o	o	DCK, PCMP MISC DATA E	-(VRCE)
XBIC	(XFR Buffer input data check) Parity Error in Buffer Input Data	o	o	o	o	o	o	o	o	o	DCK, PCMP MISC DATA E	-(VRCE) for RD
WBOC	(Write bus out check) Parity Error in Write Data Bus	o			o			o			DCK, PCMP MISC DATA E	
WTVRC	(Write Trigger VRC) Parity Error in Modulated Data	o			o			o			DCK, WVRC MISC DATA E	
DROE	(Drop out error) TSNS=0 with more than 1 Track while PHOK=1	⊖			o						DCK, EVC MISC, DATA E	⊖ : does not cause DCK.

Table 5.3 Summary of sense generating (2 of 4)

Code	Check Description	6250			1600			800			Consequent Sense Bits	Note -(): Release Check, +(): Additional Cehck
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
DBCK	(Deskewing Buffer Check) R0 Counter ≠ 00 at the time of resynchro burst	o	o								DCK, PCMP MISC DATA E	
SKWE	(Skew error) Skew greater than 14 bit cells	o									DCK, SKWE MISC DATA E	
	Skew greater than 2 bit cells				o							
	Excessive skew on 1ST bit							o				
	Skew greater than 30 bit cells		o	o		o	o					
MLTE	(Multi track error) Pointer = 1 for more than 2 tracks	o		o	o	o	o				DCK MLTE	
	Pointer = 1 for more than three tracks		⊖	⊖								⊖ : does not cause DCK.
PSAE	(Postamble error) Without Dead Track, '0' data detected within 34 bit cells after POSA for WT and LWR and 6 bit cells for RD/BRD	o	o	o							DCK EDC	
	Data '1' detected within 31 bit cells for WT, LWR and 21 bit cells for RD/BRD after POSA				o	o	o					

Table 5.3 Summary of sense generating (3 of 4)

Code	Check Description	6250			1600			800			Consequent Sense Bits	Note -(): Release Check, +(): Additional Cehck
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
VRC	(VRC) Uncorrectable data byte	o	o	o		o	o				DCK UCE	
	Parity Error in data after correction								o	o		
	Parity Error in Data				o			o				
LRCE	(LRC error) Track Direction Parity Error							o	o	o	DCK LRCE	
1 or 2	When 1, 2 track correction is executed	⊖	⊖	⊖		⊖	⊖				CRERR	⊖ : Does not cause DCK.
A ≠ B	(CRCA ≠ CRCB) Input/Output data from or to the buffer does not match	o	o	o	o	o	o	o	o	o	DCK JSC DATA E PCMP	-(OVRN)
B ≠ C	(CRCB ≠ CRCC) Write data does not match with after read data				o			o			DCK CRC CRC III MISC DATA E	
B ≠ D	(CRCB ≠ CRCD) Aux CRC read out does not match with Write/Read Data	o	o								DCK CRC CRC III MISC DATA E	-(OVRN)
*MCRC	(Unmatch CRC) CRC Error in Read Data	o	o	o				o	o	o	DCK CRC	
*MCRCC	(Unmatch CRCC) CRCC Error in Read Data			o							DCK CRC CRC III MISC DATA E	

Table 5.3 Summary of sense generating (4 of 4)

Code	Check Description	6250			1600			800			Consequent Sense Bits	Note -(): Release Check, +(): Additional Cehck
		WT LWR	RD	BRD	WT LWR	RD	BRD	WT LWR	RD	BRD		
OVRN	(Over Run) Loss of data in XFR buffer before completion of data transfer	o			o			o			OVRN	+(DCK)
	Buffer Overflow		o	o		o	o		o	o		

5.8 High Speed Mode

An MTU with the High-Speed feature, on receipt of a set high speed command (SHSP), sets the MTU to the high speed mode.

An MTU is in the normal mode when the power supply is turned ON. High speed mode is reset after unloading or if the load button is pressed after the vacuum has dropped. If a set normal speed command is issued when an MTU is ready, the high speed mode will be reset. The tape speed in the start/stop mode (normal speed mode) is increased to 125 ips in a 75 ips device and to 200 ips in a 125 ips device. The speed is also increased for Read/Write processing. If a command is reissued within the reinstruction time, the processing is not stopped as IBG streaming operation is continued.

5.8.1 Start/Stop characteristics

The time and distance required by a tape to achieve stable speed from stop position to normal speed and vice-a-versa are shown in Table 5.4.

Table 5.4 Start/Stop Characteristics

MTU Type	Operation Mode	Start Characteristics		Stop Characteristics	
		Time(ms)	Length(QTP)	Time(ms)	Length(QTP)
200/125	Normal Mode	1.2	32	1.4	36
	High speed Mode	2.5	106	2.5	106
125/75	Normal Mode	2.0	32	2.3	36
	High speed Mode	3.3	88	2.7	106

In normal speeds, the Write or Read head may be stopped the IBG area. However in the high speed mode, as the braking distance is greater (start/stop), repositioning of the head must be performed (unless streaming operation is continued). In this case, the Write head stops within 0.5 inches from the starting point of the next block towards the BOT side.

5.8.2 High speed operation

(1) Read Status

If the next command is received within the time required to pass IBG, streaming operation can be continued without a repositioning cycle. However, is the next command is not received until the Read head detects the next block, a repositioning cycle is activated and the tape is wound back to wait point. Moreover, if the next block cannot be detected within 0.6 inches, a repositioning cycle is activated.

The FMT reads data only while the gap control signal (GAPC) is '1'. A data block transmitted to the FMT from the MTU GAPC is '0' does not after operation. This is data block during a reposition cycle.

(2) Write Status

End Status is not reported until the Read Head detects IBG (in Write processing). The command reinstruction time equals the time required to run the distance obtained by deducing R/W head gap from IBG length.

The tape is stopped after a certain length passing wher a command overrun condition is occurred. At this stage, the current applied to the Write or Erase Head is cut off and a degause operationis performed for about 3 ms. This degause point is such that the erase head will be capable of erasing the write head trace of the degause when the erase current is turned on at the next operation.

The tape is then moved back to the wait point. At this stage, the MTU external and internal status are Write and Read respectively. If GO Tag is set after the command instruction time has elapsed, the tape is then driven forward. Erase current is turned ON at this time. As the tape runs through a predetermined legth, the read head passes over the previous block, IBG is detected, and write current is turned ON. Thus, the can start a Write operation after the WOK and GAPC signal.

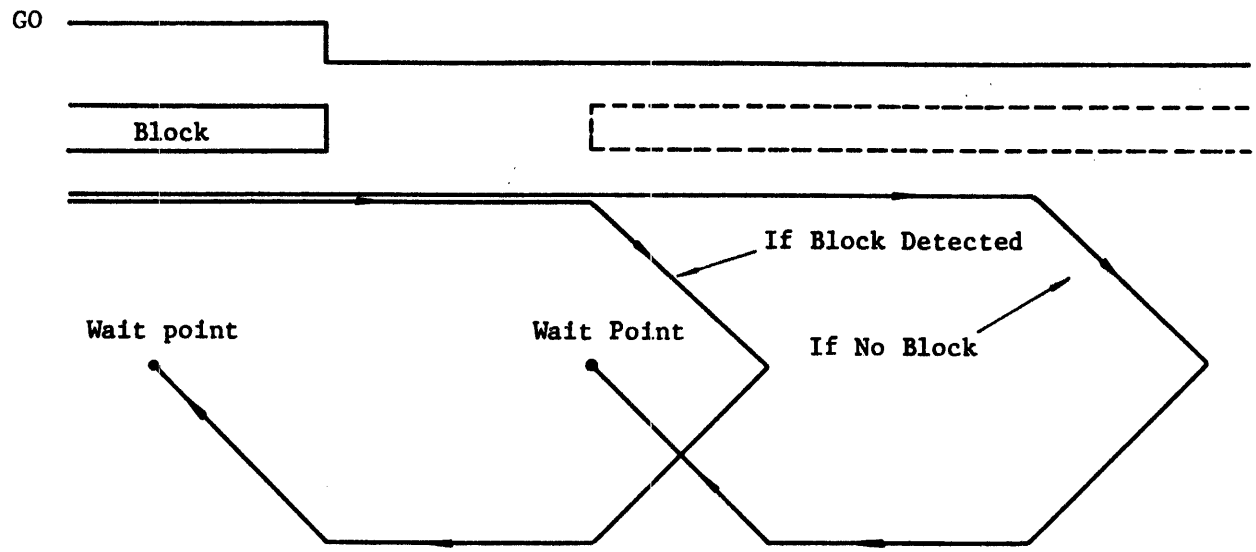


Figure 5.3 Reposition cycle (Read operation)

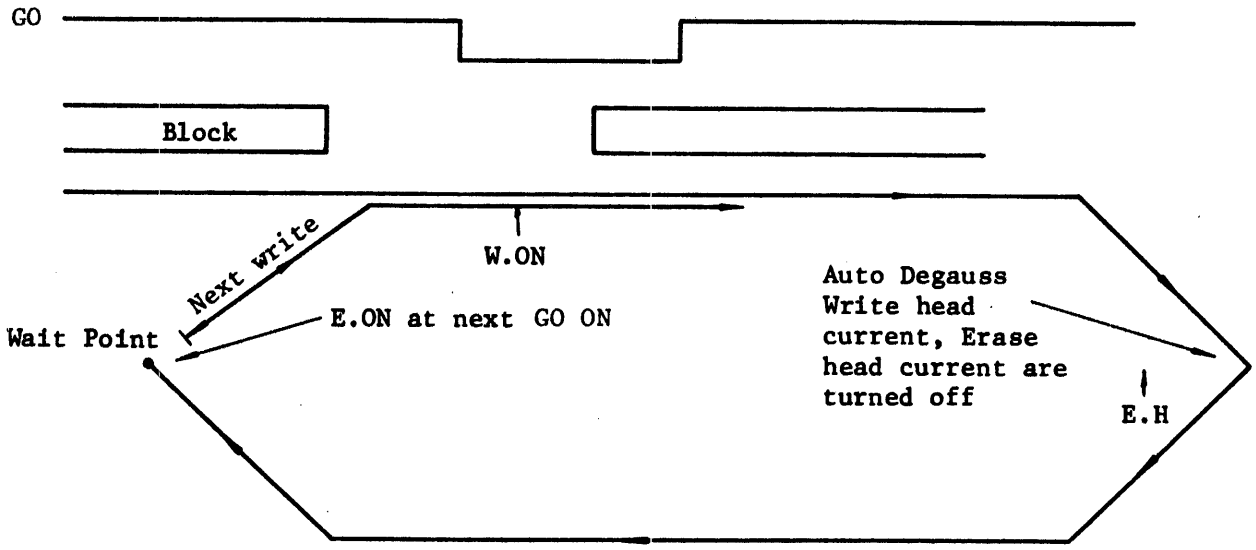


Figure 5.4 Reposition cycle (Write operation)

5.8.3 Changing status in high speed mode

In the high Speed Mode, the tape istopped and a response to a change of status request is sent to the FMT. Then the operations shown in Figure 5.5 and 5.7 are executed when the GO Tag is set.

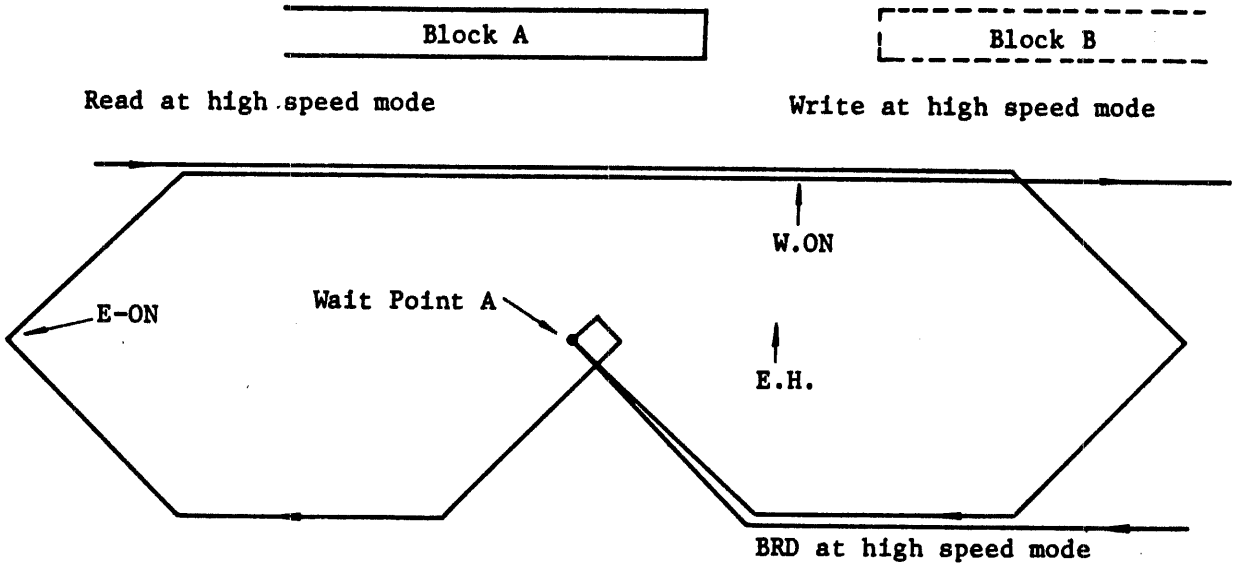


Figure 5.5 Upon changing from read to write status

(1) The operation shown in Figure 5.4 is executed if a Write type command is issued to an MTU which has just processed a READ type command. For example, if set-write-status is specified to the MTU after reading block A, the MTU runs for 6 inches after an FMT GO flag is reset. If a block is detected within this length, the MTU decelerates and returns to wait point A. Response is sent to the FMT (for Set Write Status) from this point. Now, forward hitch is executed when the Go Tag is set. Then the tape is run backwards so that the erase head covers the entire block B(to be erased). After this, the tape is run forward with erase current ON. Write current is off to this point. Write current is turned ON after the READ head passes over the above block A.

(2) If a Read backward type command is issured to an MTU after processing a Write type command, Auto deause is executed after running for a specific length, the tape is run back to the wait point, and a normal backward operation is executed. Therefore, additional rease as in a normal operation is not required.

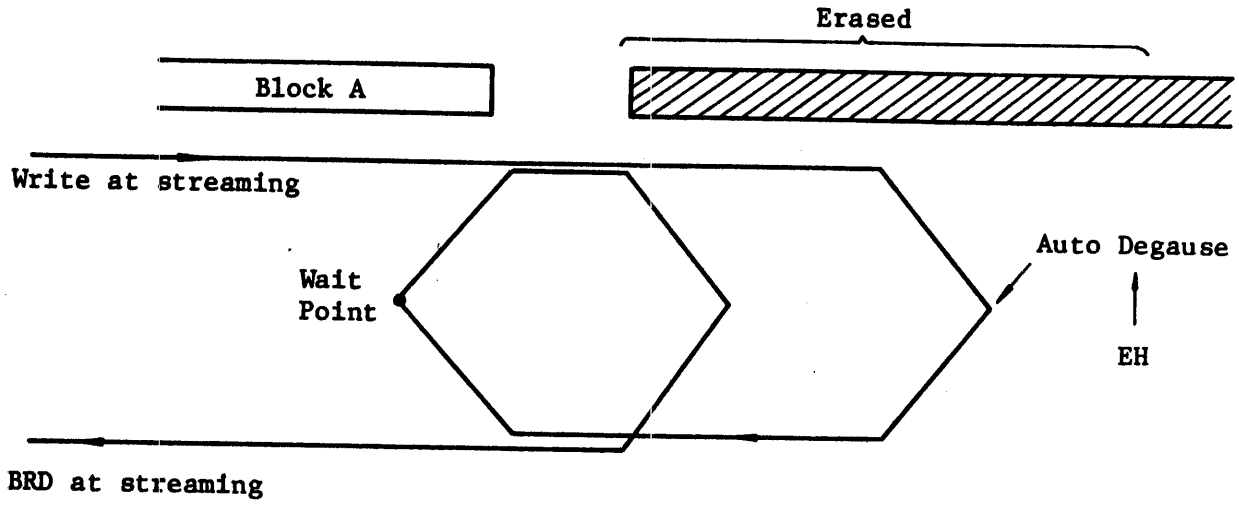


Figure 5.6 Backward read after write

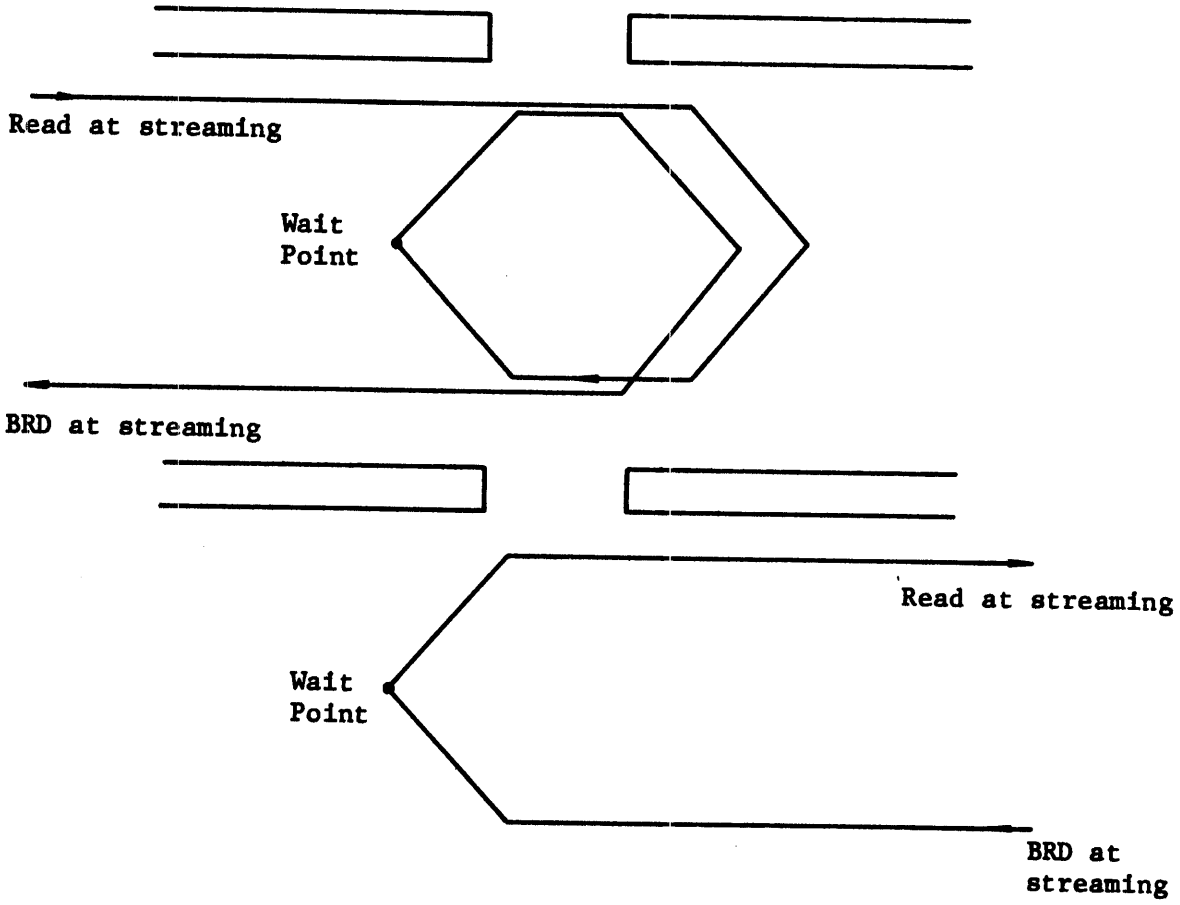


Figure 5.7 Changing from FMD → BWD, BWD → FWD

5.8.4 Command operations in high speed mode

(1) Write Operations

In case of Write type commands, the gap control signal is set at the point of 11 QTPs before normal IBG end in the 6250 rpi mode and at 360 QTPs before normal IBG end in the 1600/800rpi modes. Therefore, WOK should be set after QTPs from the above gap control signal. However, if streaming is not continued, repositioning operation is carried out from the time the GO Tag is set until the Gap Control Signal.

(2) Read Operation

In a normal READ operation, ROK is set at the point of 20 QTPs after the GO Tag is set. Block read operation is started then. However, ROK should be set after the gap control signal. If there is no repositioning cycle, the gap control signal will be set when the READ head is in an intermediate IBG positions.

5.9 MTU Communication Register

Four registers that can be accessed by the FMT are provided in the MTU. These **registers are used** as common memory sevices. Application of these **registers are described in this section.**

The FMT accesses these registers using command-tag operations. The register can be then read in Bus-in registers. Data is entered in half byte units. Register address is entered in the upper four bits while Write data is entered in the lower four bits. This is illustrated in Figure 5.8.

This register is reset (All '0's) when the power supply is turned ON. It remains unchanged even if the reset key is pressed.

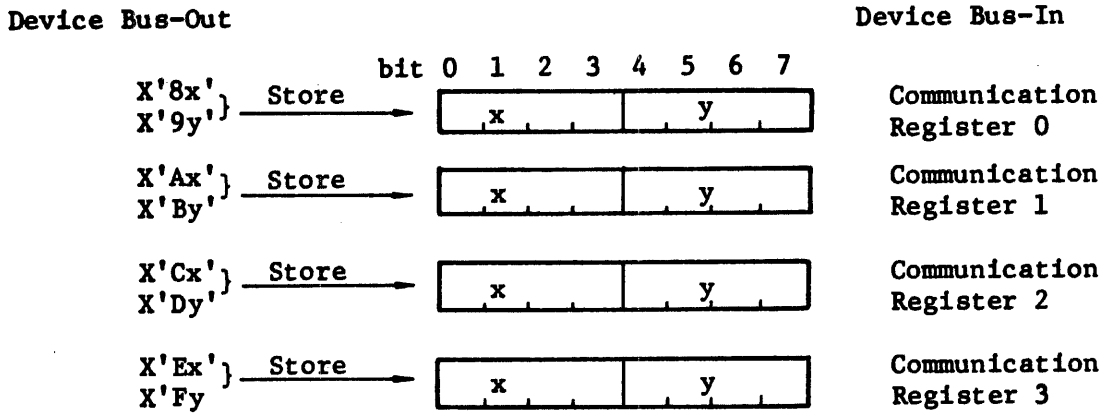


Figure 5.8 Communication register

5.9.1 Register definition

Registers are assigned as in Figure 5.9.

Communication Register	Bit 0	1	2	3	4	5	6	7
Register 0	Write Error Counter							
Register 1	Not used		Retry Counter		Not used			Long IBG
Register 2	VLDCNT	Position Counter (Upper)						
Register 3	Position Counter (Lower)							

VLDCNT: Valid Position Count

Figure 5.9 Register assign

5.9.2 Write Error Counter (WEC)

In the 6250/1600 RPI mode, the counter is advanced by +1 when a drop out error is detected in a write command operation.

Set-error-mark is issued to an MTU at a count of 96 in the 6250 rpi mode and a count of 32 in the 1600/800 rpi modes.

This counter is cleared when BRD, REW and UNL commands are executed. It is reset when starting a BOT operations.

In the 800 RPI mode, this counter is used to count Write errors (VRC, LRC, or CRC).

5.9.3 Retry Counter (RCNT)

This is a two bit counter used for an error retry count during read or read backward commands in high speed mode.

This counter is set to '00' when there are no errors in a Read operation. This counter is advanced by +1 when UCK is generated. A read operation may be executed in high speed mode when the retry counter is at '00' or '01'. However if this counter is at '10' or '11', the FMT issues a reset high speed mode request, and the Read operation is executed in the normal mode. As soon as the read operation is completed, the FMT issues a set high speed mode request. At this stage, the high speed mode is restored.

5.9.4 Long IBG Counter (LIBG)

This counter lengthens the IBG of the volume label and header label. The counter is set to '1' when starting a writer operation from BOT. The counter is decreased to 1 when a write command is completed normally. However, the counter will not underflow from '0'. Unless this long IBG counter is set to '0', the IBG length is longer than the normal IBG by one inch.

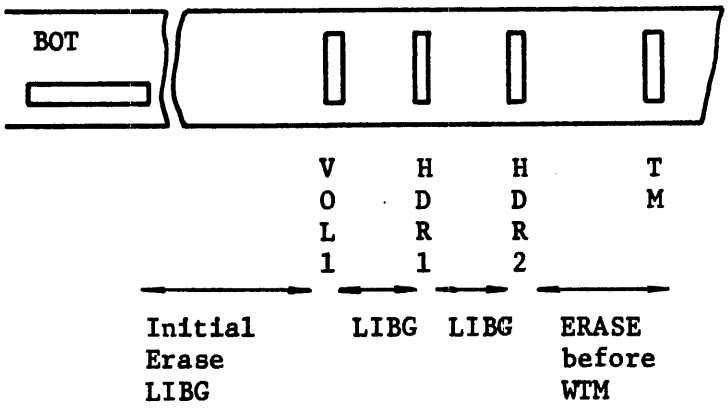


Figure 5.10 Long IBG

Note: One inch tape erase is executed as a initial erase.

5.9.5 Position counter

This counter is used to check if the head has been positioned correctly in Back Space and Space Commands executed for error retry in Read, Read Backward and Write Commands. The positioning is checked by the length through which the tape has run. This checking can improve the reliability for error retry processing. This counter counts the TPs during RD, BRD and WRT commands, the FMT stores them as DCK, OVRN and BUSER. **BUSER.**

The count is started during read commands after detecting HBLK.. The count is continued until the end of the crease check after detecting DBIG. The count is started in the write command when WOK is set and continued until GO Tag is reset.

During SP or BSP (error retry) commands, the counter is started after GAPC is set. The counting is continued until the end of crease checking. At this stage the count is compared with the count from position counter. If the difference between the two (difference in crease length, R/W Head Gap, Add erase, etc.) is greater than ±64 TP, Missing Position error is set (Reject Code 035).

This counter is a 15 bit counter and is capable of counting up to 32 KTP. If the counter over flows, VLDCNT is reset ('0').

VLDCNT is reset after executing RD and BRD commands in the high speed mode. VLDCNT count is reset ('0') if the command to be executed has the same direction as the preceding command. The counter value may not be compared if VLDCNT is '0'.

5.10 Tag Control

The FMT controls the MTU using 3 tag lines (status tag, control tag and GO Tag), nine control data lines (DVB00 to DVB08) and one strobe signal line (TAGVL). The microprogram uses these to specify the required operation.

Various subroutines have been provided for control and check of the selected MTU. These subroutines are used by the command operation routines repeatedly. These subroutines set control data in the DVBO register and generate the required Tag signals. They also scan the MTU to make sure that the required operations are started and completed within the specified time. If an error is detected in the MTU tag control operation, the error data is shown as a Reject Code and the processing is branched to the command operation terminate routine.

Tag Control details are given in Table 5.5.

If the required operations are completed, the register files containing the MTU status are updated.

Table 5.5 Tag control

Function	Manupilation			Response Confirmation	Time out	Sense Byte in case of Errors
	DVBO	STSTAG	CTLTAG			
Set Write Status	10	1	0	ERS=FWD=WRS=1 BWD=LWR=0	500 ms	STRJ
Set Erase Status	80	1	0	ERS=FWD=1 BWD=LWR=0	"	"
Set Forward Read	40	1	0	FWD=1 ERS=BWD=WRS=LWR=0	"	"
Set Backward Read	20	1	0	BWD=1 ERS=FWD=WRS=LWR=0	"	"
Set LWR Status	01	1	0	LWR=1	13.6 ms	"
Reset LWR Status	00	1	0	LWR=0	"	"
Set GCR Status	04	1	0	1600=0	"	"
Set PE Status	02	1	0	1600=1, SAGC=0	"	"
Set NRZ Status	04	1	0	1600=0	"	"
Set LWR2 Status	08	1	1	LWR2=1	13.6 ms	CMRJ
Reset LWR2 Status	09	1	1	LWR=0	"	"
Set low slice level	0A	1	1	LWSL=1	"	"
Reset low slice level	0B	1	1	LWSL=0	"	"
Set High Speed	02	1	1	STRMD=1	1,513 ms	"
Reset High Speed	03	1	1	STRMD=0	"	"
Set Space file	04	1	1	RDY=0	"	"
Set Backspace file	05	1	1	RDY=0	"	"
Set Rewind	02	0	1	REW=1, RDY=0	500 ms	CTRJ
Set DSE	04	0	1	DSE=1, RDY=0	"	"
Set unload	01	0	1	UNL=1, RDY=0	"	"
Set error mark	08	0	1	EMK=1	"	"
Reset TU	08	1	0	TUC=0, WT=0	10 µs (100 µs)	STRJ

5.11 Offline Service Routine

The Field Tester can be used to manually execute various commands. This routine allows for repeating commands, automatic retry on detection of a particular end status, stopping of processing and scanning to enable serial execution of commands in the MTU. The offline service cycle is started when the Field Tester ONL/OFL switch is set to OFL and the SSS switch is toggled. At this stage, a trap is set at address '100' in the microprogram. The control is then transferred to the trap decode routine. The trap decoding routine starts offline service if no other traps are found.

As shown in Fig. 5.11, when a command operation is completed and the end status is generated, this status is checked by branching to the offline service routine prior to going into idle status. The next command operation is started in accordance with the specified control function (command code changing, MTU address increment, Go Down Time, etc.), or the system goes into idle status upon completion of the service cycle.

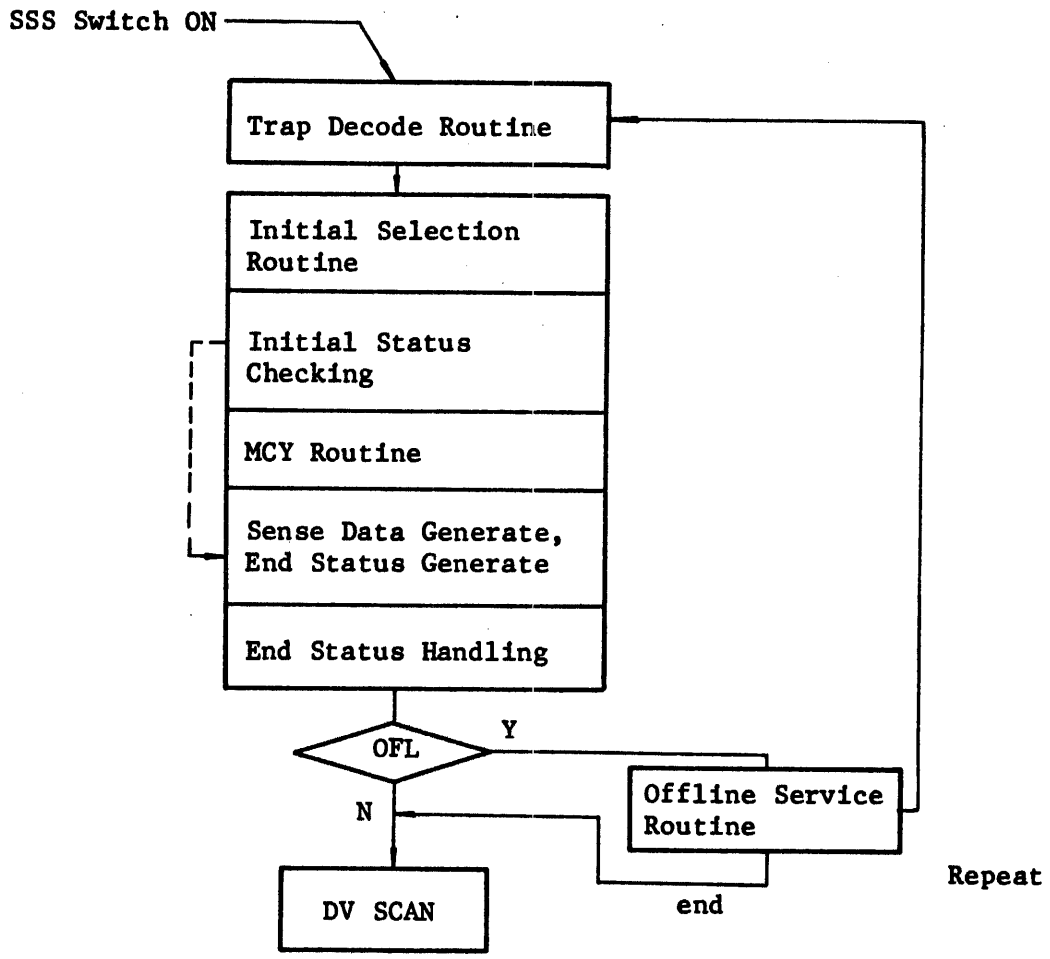


Figure 5.11 Offline service cycle

Table 5.6 Offline Service Function Specification Register

Register Name	SDIA0	SDIA1	SDIA2	SDIA3	OFLCNT	OFLCMT	OFLDVA	BCT
Address	38	39	3A	3B	3C	3D	3E	3F
bit 0	DMW/DMR	LWR TUIF			STP.UCK		SBC	
1	MARG	INV	.MASK track	GDT	RPS.UCK			BYTE Count
2	IPOST/XFR		.Marginal Code	lower	STP.UEX	CMD Code	(BPSCY)	
3	GDT				REW.UEX	& Density	(REVCY)	
4	UORE/MARA		.GDT Upper		REV.UEX	Select	(OFSCY)	
5	LWR R/W	MASKP			RPS		OFDVA0	
6	MASK				REPEAT		OFDVA1	
7	TFMT				TUSCAN		OFDVA2	

The offline service function is specified by storing the required data in the registers shown in Table 5.6

(1) SDIA0 to SDIA3

SDIA0 to SIDA3 are the same as the 4 byte diagnostic flag specified in the Set-diagnostic command.

When the FMT is in an offline status, the specified diagnostic operation may be carried out by executing the command operation (without chaining) by SSIA command. The SDIA data once set, is not be altered until the FMT is set to online status.

(2) Tape Unit Scan

When the OFLCNT register TUSCAN bit is set to '1', the OFLDVA register OFLDVA)_@ bits are advanced by +1. If the repeat bit has also been set '1', commands are issued serially to all MTUs.

(3) REPEAT

When OFLCNT register is set to '1' and the REPEAT bit is reset to '0', a command is executed every time the SSS switch is pressed.

Unless this bit reset ('0'), (while REPEAT bit is 1), the command execution activated by the SSS switch is repeated continuously.

(4) Reposition

The following offline repositioning operation is performed when the OFLCNT register RPS bit is set.

The commands and addresses entered in OFLCMD and OFLDVA 0-2 remain unchanged even after the offline repositioning operation.

Table 5.7 Offline reposition

Commands set in OFLCMD register	Offline Reposition Operation
x6 (Write) 86 6250 46 800 06 1600	Back space command is executed after a Write command. However if IDBRST (ID Burst check) and Reject are set, Rewind Command will be executed instead of the Back Space Command. And then, ERS command is executed.
04 (Read)	Back Space Command follows the Read Command.
05 (Backward Read)	Space Command follows the Backward Read Command.
Other commands	No operation.

(5) UEX Function

The following operation is executed when the UEX bit in the DSB register is set after command operation by using combinations of STP.UEX, REW.UEX, REV. UEX in the OFLCN register.

UEX bit is set in following case; EOT is detected in forward operation. Tape Mark is detected during RD, BRD, SP or BSP commands.

Table 5.8 UEX functions

<table>
<tr><th>STP
.UEX</th><th>REW
.UEX</th><th>REV
.UEX</th><th>UEX Function Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Processing is looped within the offline service routine from the time UEX bit turned ON till STP.UEX bit is reset (0) or SINH is specified.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No operation. (UEX bit is not checked.)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>When UEX bit is included in DSB register, the OFLCMD register command codes are replaced by Reverse Commands as follows:
<table>
<tr><th>Old OFLCMD</th><th>→</th><th>New OFLCMD</th></tr>
<tr><td>WT(06)</td><td>→</td><td>BRD(05)</td></tr>
<tr><td>RD(04)</td><td>→</td><td>BRD(05)</td></tr>
<tr><td>BRD(05)</td><td>→</td><td>RD(04)</td></tr>
<tr><td>SP(0B)</td><td>→</td><td>BSP(09)</td></tr>
<tr><td>BSP(09)</td><td>→</td><td>SP(0B)</td></tr>
<tr><td>ERS(0D)</td><td>→</td><td>BRD(05)</td></tr>
<tr><td>WTM(0C)</td><td>→</td><td>BRD(05)</td></tr>
<tr><td>DSE(1D)</td><td>→</td><td>BRD(05)</td></tr>
<tr><td>NOP(00)</td><td>→</td><td>BRD(05)</td></tr>
<tr><td>Others</td><td>→</td><td>Not changed</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Rewind Command is issued when UEX bit is included in the DSB register after command execution.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Rewinds MTU by issuing a rewind command when UEX bit is included in DSB register. Then, MTUs are reversed from Normal Speed to High Speed or from High Speed mode to Normal Speed.</td></tr>
</table>

(6) UCK Function

In UCK bit is included in the DBS register, the operations shown in the following Table 5.13 are performed. The operations are specified be combinations if the STP.UCK, RPS.UCK bits. ERRF lamp is turned ON when the UCK bit is set.

UCK bit is set in following cases; DCK is asserted.
Reject is asserted.
Overrun is asserted.
BUSER is asserted.

Table 5.9 UCK function

STP .UCK	RPS .UCK	UCK Function Description
0	0	UCK bit is not checked.
0	1	The repositioning operation described in (4) is executed when the UCK bit is set. Any errors in the repositioning operations are ignored.
1	0	When UCK bit is included in DSB register, Processing is looped within the offline service routine until the STP.UCK bit is reset or SINH is specified.
1	1	The repositioning operation in (4) is executed when the UCK bit is set. Any new errors (UCK) during repositioning operation cause μP loop in the offline service routine till STP.UCK bit is reset '0' or SINH is specified.

(7) SINH (Start Inhibit)

When the SINH bit on the Field Tester is ON, commands issued by the SSS swith are inhibited.

A loop created by STP.UCK or STP.UEX bits may be released by setting the SINH bit. If SINH is turned OFF again, commands will be issued again (in case of REPEAT).

Commands may be temporarily inhibited if SINH bit is set (ON when REPEAT has been specified. This facilitates temporary stopping or starting of commands in the manual mode (without resetting REPEAT bit).

CHAPTER 6 FIELD TESTER

6.1 Field Tester

The field tester is made up of eleven switches and twelve luminuous dioses, and does not feature a power supply. It is connected to the FMT for maintenance or checking purposes. A fifty signal line flat cable is used to connect the FMT. Operations carried out by the Field Tester are as follows:

(1) **Display status of signal lines and registers.**

(2) **Rewrites Microprogram Address Counter.**

(3) **Rewrite of data to registers.**

(4) **Address Compare and Stop** MP.

(5) **Address Compare and Branch** MP.

(6) **Address Compare and Display (register data).**

(7) **Address Compare and Write (to register).**

(8) **Microprogram stop, step and run.**

(9) **CS Scan.**

(10) **Starting offline Service Routine, specifying and execution of commands. (Refer to section 5.11.)**

Related hardware is deccribed in subsection 4.4.4. Related software is described in section 5.17.

CHAPTER 7 DIAGNOSTICS

The FMT is provided with microprogram routines and hardware required for diagnostics.

The FMT microprograms perform the following diagnostic operations.

7.1 Diagnostic Routine

(1) Diagnosis upon turning ON the Power Supply

The power-on diagnostic routine tests the FMT hardware when the power supply is turned ON.

The purpose of this diagnostic operation is to detect and notify the system of hardware errors. As soon as the power supply is turned ON, the self test routine (described in section 5.2) is executed to verify the micro processor. If no errors are detected, the Power-On Diagnose routine is executed. (Refer 5.3 (3).)

(2) Processor Self Test

If the microprogram starts from address '000' after the power supply is turned ON, the processor self test is executed. This test is also started by system reset, selective reset, Field Tester ONL/OFL switch transition, and CE reset by the operator from the Field Tester. Details on the tests are given in section 5.2.

(3) Reset Routine

If no errors are detected in the processor self test, the specified reset routine is executed. When LSR is reset by the reset routine, the operation is checked to make sure that the LSR is cleared.

(4) FMT Resident Diagnostics

In the FMT microprogram, there are many diagnostic routines which test both the FMT and MTUs. The diagnostic routines can be initiated by the Field Tester in the offline mode (offline diagnostics) and via the Controller using the Set Diagnostic Command (Test MTS operation). Both the offline diagnostics and Test MTS operation can be initiated using the Field Tester. Refer to section 7.4 for details.

7.2 Diagnostic Error Termination

The errors detected in the diagnostic tests described in section 7.1 are treated as follows:

(1) If an error is detected in the FMT ON-LINE mode, the system goes into a wait status until the next initial selection request is received (INS bit='1').

At this stage, the error codes have been stored in the SB22 and SB23 registers (FRU code). When the next selection request is received. Reject code 302 is sent otu to notify an error to the Controller.

(2) FMT in the offline status

The FMT microprogram operation is the same as in (1). As the ERRF bit on the Field TEster is turned ON in an offline status, the error may be detected visually. As the cause of error is set in Registers SB22, SB23 in the form of error codes, details can be obtained by using the register display function. Error status may be reset by operation similar to online mode (this is done by executing a command or by resetting the system (e.g., CE reset).

7.3 Diagnostic Operation Using the Field Tester

7.3.1 Command trial

To verify various functions of the FMT, execute FMT commands using the Field Tester. The offline service routine is described in detail in section 5.17. For details on Field Tester Operation procedures, refer to the Maintenance Manusl.

When a command is executed form the Field Tester, the results of processing may be displayed by lamp L10 (ERRF lamp). Set Field Tester to Interface Display Mode. The offline service routine sets the ERRF bit when the UCK is included in the DSB register. Errors details are set in SB0-SB23 sense byte stack area and may be displayed by using the register display function. The ERRF lamp will be reset when a new END staus is generated (ERRF lamp indicates the results of the immediately preceeding the command).

The UCK reposition function provided with OFL service routines may be useful to check the DCK.

7.3.2 Issuing TEST MTS

Tests on the basic FMT hardware as well as tests on the Read/Write data bus to the MTU may be executed if necessery. These tests are performed by executing the diagnostic command 'test FMT' function from the Field Tester.

As explained in section 5.10, the diagnostic flag byte may be specified anytime in the offline mode. Therefore, the SDIA command with FMT bit (SDIAO register bit 7) caouses comprehensive diagnostic operations. The test routine number should be indicated in the SDIA register, and the test MTU address should be specified in the OFLDVA register.

Result of those diagnostic operations are indicated in the Y2 and Y3 registers as error codes. If some error has been detected, a Reject Code is generated.

All MTUs may be tested serially by the TUSCAN function.

7.3.3 Issuing Offline Diagnostics

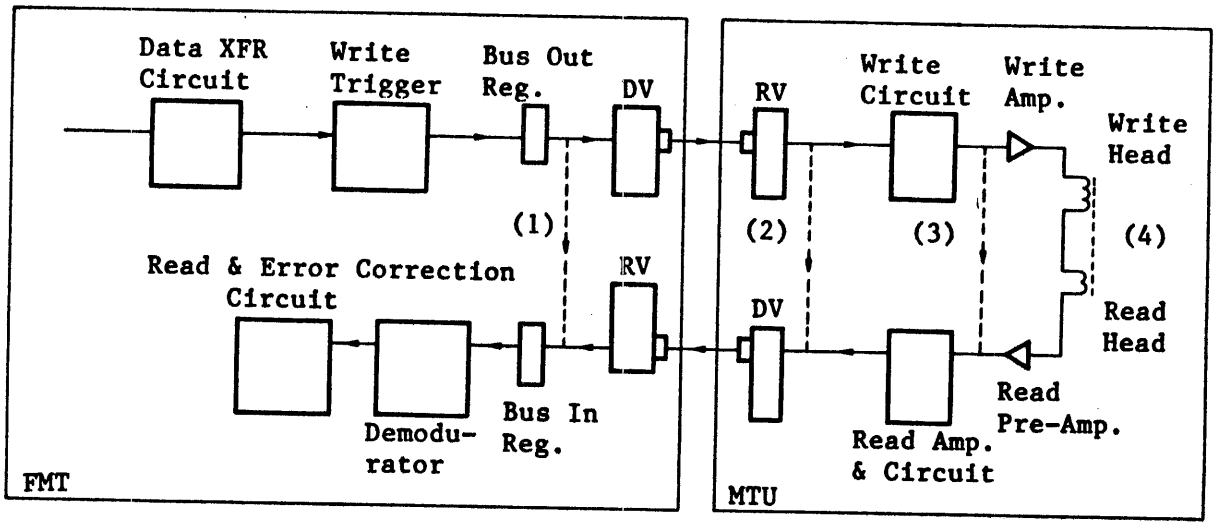
The same operation can be performed as described subsection 7.3.2 by the following operation. After setting routine number to the SDIA1 register, set switches 0 to 7 to hex A8, and then toggle the CNT switch.

If there are same errors in the "ERRF" bit will be set, and the error code will be indicated in the register a Y2 and Y3.

7.4 Offline Diagnostics and TMTS Operation

CONTENTS OF FMT RESIDENT DIAGNOSTICS

Diagnostic routines chek-out the FMT hardeware therefore and examine the MT subsystem and Tape Drive a through FMT MTU interface. Each routine extend its test territory one by one the test program can therefore limit doubtful subassemblies. Following is an example of verification of the read and write data path.



There are four levels of write operations are:

(1) LWR operation within FMT.
In this operation, FMT Read/Write circuits are checked.

(2) LWR TU IF within MTU RV/DV.
In this operation, FMT DV/RV, IF cable and MTU RV/DV are checked.

(3) LWR R/W operation within the MTU analoge R/W curcuit.
In this operation, the MTU R/W PCA is checked.

(4) Normal Write Operation.
In this operation, R/W Head and R/W Amplifiers are checked.

Details of diagnostic routines and error codes are described in Maintenance Manual. Main diagnostic routines are as follows:

Example of Diagnostics Routine

1. FMT MICRO PROCESSOR SELF DIAG

To check all micro processor function.
e.g. Unconditional Branch, Conditional Branch, Test Bit Branch, Register operation, and ALU operation.

2. Local Storage Register Test (FMT)

To check 64 byte RAM.
All Os/all 1s are set, and read/compare Test Data Pattern are set and compared.

3. External Register Test (FMT)

To check 46 byte hareware registers.
e.g. Initial Value check, set and reset each bit.

4. TIMER TEST

To check formatter hardware timer function.
e.g. Clock count mode, TP count mode.

5. Device IF Register Test

To check DV IF PCA function
e.g. Loop from DVBO reg to DVBI reg.
Device Bus MPX.

6. Host Interface Test

To check CNT IF PCA function
e.g. IF register check
Data Transfer, operation check in Offline mode.

7. MTU Selection Logic Test

To check the MTU selection logic in the Distribution PCA.

8. LSI SCAN Test

To check old LSI flip-flops (841 FFs).
e.g. Scan in/out, all 1 data, all 0 data.

9. Time Sensor Test

To check Data Pulse and Time Sensor Logic.
e.g. Time sense function check by micro program, time sensor decoder check.

10. LWR FMT

To check data path in FMT.
e.g. Check R/W circuits of the FMT in the Write status and Read status.

11. LWR TU IF

To check the MTU logic PCA and FMT/MTU interface circuits including the DV/RV and the interface cable.

12. LWR R/W

To check the MTU MTU R/W PCA.

13. Error Correction Logic Test

To check the FMT WRT PCA function.
e.g. Error correction in 1 or 2 Track masked condition.

14. Format Control and Check Logic Test

To check FMT WRT PCA (512186U) function.
e.g. Slip check circuit, Early Begin counter check, etc. by FMT LWR.

15. MTU IF Logic Test

To check the FMT/MTU IF logic function.
e.g. Inspection of Control Tag/Status Tag/Command Tag operation.

16. Reel Servo Test

To check the Reel Motors and capacitive sensor.
e.g. To check that the tape loop does not to enter warning area of columns by performing a Simple FWD or BWD turn, over-load operation.

17. Capstan Test

To check Capstan Motor, Tach and capstan servo.
e.g. Shoe shine test ... check slip & Hitch.
Start/Stop Transient Test.

18. Tape Speed Check

To check tape speed stability and examine speed check circuit of the FMT, and verify tape path, especially air bearings.
e.g. Tach Pulse interval count, speed OK counter check.

19. Erase Effect Test

To check Erase Head installation.
e.g. Write all 1s in high and low density, and back space the . The **erase it only by an erase head and read the area in low slice level.**

20. Read/Write Test

To check the total read/write funtion.
e.g. *Slice margin, SAGC function at various position.
***Set SAGC Count** to $F and check GSD function.

21. Read Level Check

To check the Head using the read amplitude level measured by various slice levels.

22. IBG Length Check

To check the Gap Control Signal and IBG contol circuit.
e.g. *Examination of IBG length by Tach count.
***Examination of capstan by slip length and velocity retry times.**

23. Feed Through Test

To check head feed through signal level.
e.g. Checking read signal in low slice level immediately after writing Block.

24. Cross Talk Test

To check cross talk between each track of head.
e.g. Writing alternate all 1s data and masked data for each track and check **masked Track read level.**

25. Various Density Test

To check the amplitude sensor.
e.g. Write or LWR R/W 9042/3014, 3200/1600 FCI and check read signal.

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