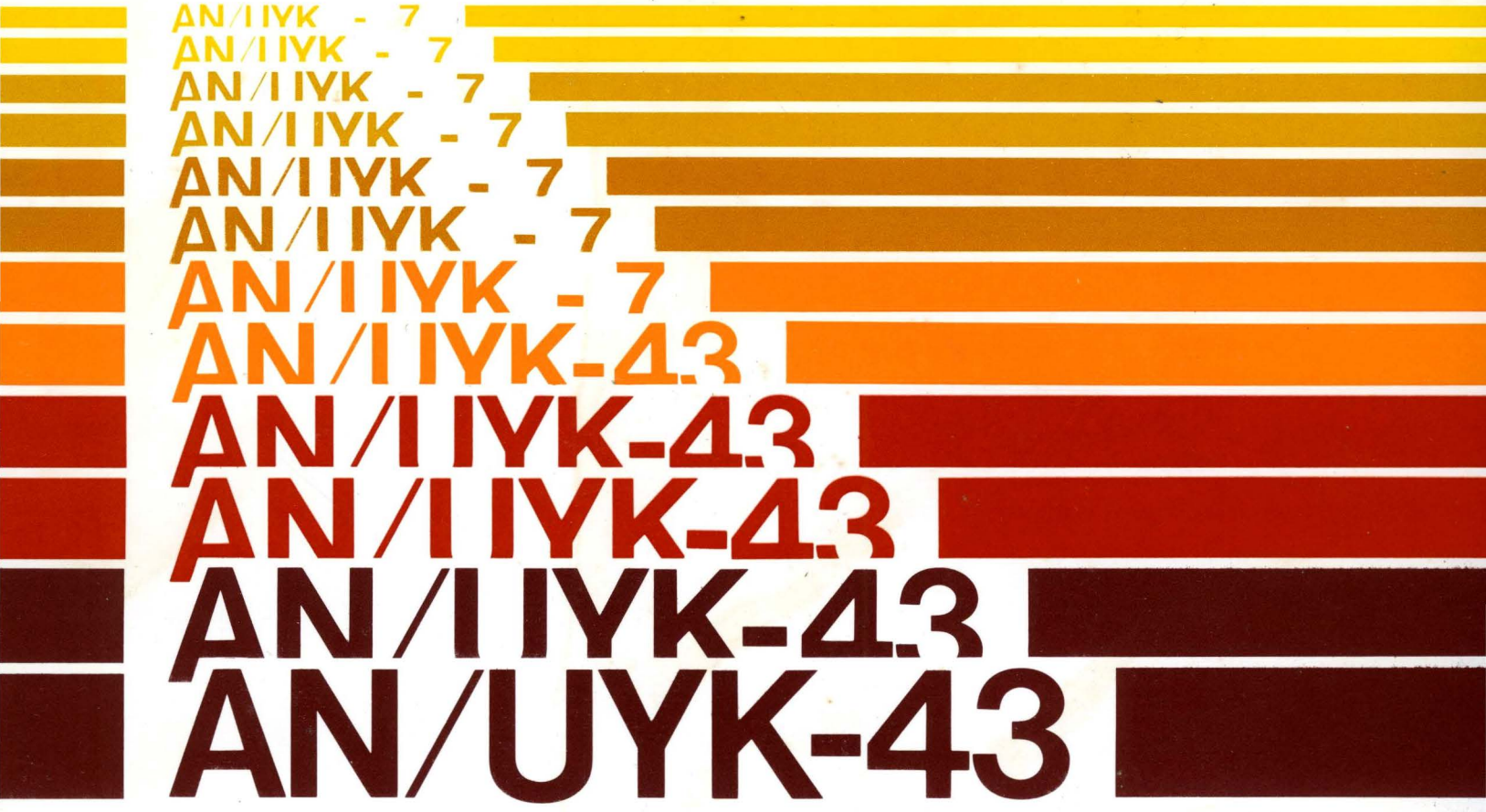
IBM

AN/UYK-43 Full Scale Engineering Development (FSED)

Preliminary Design Review (PDR)
27 April 1981 – 01 May 1981

Book 1



AN/UYK-43

PRELIMINARY DESIGN REVIEW

27 APRIL 1981

Topic	Time	Team	Place	Person Responsible
Introduction	11:00 – 11:15	All	308-310	Wood
Schedule Summary	11:15 – 11:30	All	308-310	O'Gara
Lunch	11:30 – 12:30	–	308-310	
Requirements/Compliance Summary	12:30 – 1:30	All	308-310	Bergeman
Mechanical Packaging Overview	1:30 – 2:00	All	308-310	Yogodzinski
Architecture Overview	2:00 – 2:30	All	308-310	Bergeman
Man Machine Interface	2:30 – 3:30	All	308-310	Mastranadi
Software Development Overview	3:30 – 4:30	All	308-310	Collart

IBM

AN/UYK-43

PRELIMINARY DESIGN REVIEW

28 APRIL 1981 (AM)

Topic	Time	Team	Place	Person Responsible
Mechanical Design	8:00 – 11:30	Hardware	308-310	Yogodzinski
ISA Extensions Navy (Discussions)	8:00 – 8:30	Software	324	Bergeman
ISA Extensions IBM (Discussions)	8:30 – 9:30	Software	324	Bergeman
SDEX/Common Program	9:30 – 10:30	Software	324	Barker
NDRO Programs	10:30 – 11:30	Software	324	Bergeman
Fault Tolerant Design Philosophy	11:30 – 12:30	All	308-310	Bergeman
Lunch	12:30 – 1:00	—	308-310	—

AN/UYK-43

PRELIMINARY DESIGN REVIEW

28 APRIL 1981 (PM)

Topic	Time	Team	Place	Person Responsible
Thermal Design	1:00 – 3:00	Hardware	308-310	Donegan
Worst Case Analysis	3:00 – 4:00	Hardware	308-310	Latvala
FTRM	1:00 – 3:00	System	Exec 2	Barker
Operational Test Program	3:00 – 3:30	Systems	Exec 2	Barker
Emulation Validation Program	3:30 – 4:30	Systems	Exec 2	Dapp
Tactical Computer Program	4:30 – 5:00	Software	Exec 2	Intrieri

AN/UYK-43

PRELIMINARY DESIGN REVIEW

29 APRIL 1981 (AM)

Topic	Time	Team	Place	Person Responsible
CPU Design	8:00 – 11:00	Hardware	308-310	Smith
Hardware Review	9:00 – 12:00	Special	318	Turecek/DeSantis
Memory System	11:00 – 12:00	Hardware	308-310	Smith
Software Programs Relationship	8:00 – 10:30	Software	324	Barker
Diagnostics	10:30 – 12:00	Systems	324	Barker/Dapp
AN/UYK-43 Parts Control	9:00 – 11:00	Special	320	Dickinson
Lunch	12:00 – 1:00	–	308-310	

AN/UYK-43

PRELIMINARY DESIGN REVIEW

29 APRIL 1981 (PM)

Topic	Time	Team	Place	Person Responsible
EMC/EMP	1:00 – 4:00	Special	320	Kearney
IOC Design	1:00 – 3:00	Hardware	308-310	House
IOA Design	3:00 – 5:00	Hardware	308-310	House
Bench Mark Generation Program	1:00 – 2:00	Software	318	Intrieri
Microcode Development Support Software	2:00 – 4:00	Software	318	Barnes
Software Development Plan	4:00 – 4:30	Software	318	Collart
Special Tasks	4:30 – 5:00	Software	318	Kozlowski

IBM

AN/UYK-43

PRELIMINARY DESIGN REVIEW

30 APRIL 1981 (AM)

Topic	Time	Team	Place	Person Responsible
Power System	8:00 – 10:00	Hardware	308-310	Schwarz
Technology Infusion	8:30 – 9:00	Special	322	Annis
Performance Monitor, Program Debug Aids	8:00 – 9:30	Systems	324	Smith/House
Emulation Micro Programs	9:30 – 11:00	Software	324	House/Smith
Computer Interconnection System Design	10:00 – 11:30	Hardware	308-310	Bergeman
Reliability/Maintainability	9:30 – 12:00	Special	322	Bobrowski
AN/UYK-43 Project Library	11:30 – 12:00	Systems	308-310	DeSantis
Lunch	12:00 – 1:00	—	308-310	–

AN/UYK-43

PRELIMINARY DESIGN REVIEW

30 APRIL 1981 (PM)

Topic	Time	Team	Place	Person Responsible
AN/UYK-43 Software Development Facility	1:00 – 2:00	All	308-310	Kemerer
Plant Lab Tour	2:00 – 3:00	All	308-310	Wood
Test Plan	3:00 – 3:30	All	308-310	Mastranadi
System Team Status	3:30 – 4:15			
Hardware Team Summary	4:15 – 5:00		308-310	Latuala

AN/UYK-43

PRELIMINARY DESIGN REVIEW

01 MAY 1981

Topic	Time	Team	Place	Person Responsible
Hardware Schedule Status	8:00 – 8:30	–	308-310	DeSantis
Software Team Status	8:30 – 9:00	–	308-310	Collart
Special Team Summaries				
– EMC/EMP	9:00 – 9:30	–	308-310	Kearney
– Technology Infusion	9:30 – 10:00	–	308-310	Annis
– R&M	10:00 – 11:00	–	308-310	Bobrowski
– Parts Control	11:00 – 11:30	–	308-310	Dickinson
Lunch	11:30 – 12:00	–	308-310	–

SCHEDULE

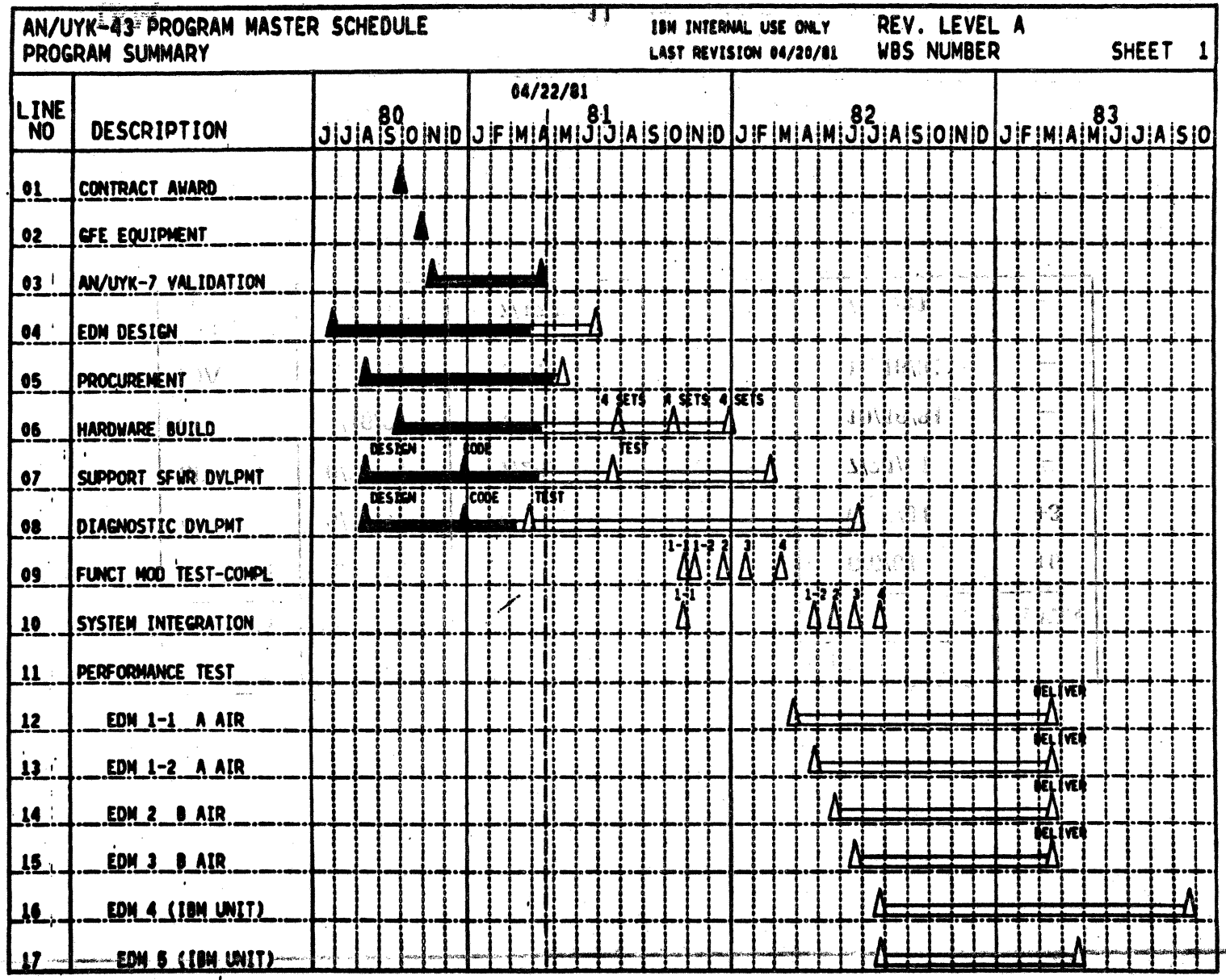
SUMMARY

AN/UYK-43 PROGRAM MASTER SCHEDULE
PROGRAM SUMMARY

IBM INTERNAL USE ONLY
LAST REVISION 04/20/81

REV. LEVEL A
WBS NUMBER

SHEET 1



FUNCTIONAL MODULE TEST SUMMARY

Module	Plan		SDR Outlook		Δ Wks
	Start BLD	Avail. for FMT	Start BLD	Avail. for FMT	
DCP/CCL	3/26/81	4/23/81	5/6/81	6/8/81	+6
IOC	5/1/81	6/4/81	5/22/81	6/24/81	+3
CPU	6/22/81	7/24/81	6/22/81	7/24/81	—
CIS	9/16/81	10/16/81	9/16/81	10/16/81	—
IOA	9/16/81	10/16/81	9/16/81	10/16/81	—
MEM/ BUS	6/12/81	7/12/81	6/12/81	7/12/81	—

SCHEDULE CONTAINMENT PLAN AT SDR

- All LRUS within Functional Modules have been prioritized to insure that proper emphasis is placed on that page required first.
- DCP/CCL – a breadboard driver page has been built by engineering to insure start of Functional Module Test on schedule.
- IOC – multi wire test Backpanel is in process and will be available to start Functional Module Test on Schedule.
- IOA and CIS Functional Module Test is currently projected approximately 9 weeks early through the use of a Multiwire Test Backpanel.

SCHEDULE CONTAINMENT PLAN AT PDR

- All LRUS within Functional Modules have been prioritized to insure that proper emphasis is placed on that page required first.
- DCP/CCL – a breadboard driver page has been built by engineering to insure start of Functional Module Test (FMT) on schedule.
- CPU/IOC – Test fixtures have been built to start initial page test without backpanel.
- IOA–Functional Module Test is currently projected approximately 8 weeks early through the use of a Multiwire Test Backpanel.
- CIS–FMT is being rescheduled and will be made available to meet system integration requirements.
- MEM/BUSS – Test fixtures have been built to start initial page test without backpanel.

FUNCTIONAL MODULE TEST SUMMARY

Module	Plan		PDR Outlook		Δ Wks
	Start BLD	Avail. for FMT	Start BLD	Avail. for FMT	
DCP/CCL	3/26/81	4/23/81	3/20/81	4/24/81	—
IOC	5/1/81	6/4/81	6/5/81	7/3/81	+4
CPU	6/22/81	7/24/81	5/29/81	6/26/81	-4
CIS	9/16/81	10/16/81	11/6/81	12/4/81	+6
IOA	9/16/81	10/16/81	7/24/81	8/21/81	-8
MEM/ BUS	6/12/81	7/12/81	6/26/81	7/24/81	+2

REQUIREMENTS/COMPLIANCE

SUMMARY

REQUIREMENTS/COMPLIANCE SUMMARY

- Performance
- Mission Requirements
- Purchase Description Miscellaneous
- MIL-Standards

IBM

5065-1

PERFORMANCE COMPLIANCE

Parameter	Purchase description requirements	Design projections
CPU		
CPU throughput		
Core alone	1.5 x AN/UYK-7	1.9 x AN/UYK-7
Core w/SCM	—	3.1 x
SCM	3.0 x	3.1 x
CACHE	4.5 x	4.7 x
CIS	1.0 x	1.2 x
CPU IET	⩽ AN/UYK-7	⩽ AN/UYK-7
Interrupt response	⩽ AN/UYK-7	TBD
Memory contention	Contention resolution does not limit performance	Contention resolution overlapped with storage access
I/O		
Aggregate throughput	3 m words/sec	4 m words/sec
IOC IET	⩽ AN/UYK-7	⩽ AN/UYK-7 Instruction execution overlapped with data transfer
Channel throughput	Max allowed by interface specifications	Max
Type J throughput	500 K words/sec	500 K words/sec

PERFORMANCE DATA

MAJOR FUNCTION CODE	AN/UYK-7(V) EXECUTION TIME	WEIGHT FACTOR %	AN/UYK-7(V) WEIGHTED TIME	AN/UYK-43 EXECUTION TIME	AN/UYK-43 WEIGHTED TIME
01	1.5000	.3488	.5232	.8125	.2834
02*	2.7900	1.9930	5.5605	.9286	1.8507
03*	2.5000	.3587	.8969	1.9375	.6951
05*	3.5500	1.9930	7.0752	1.5500	3.0892
06	9.8750	.9965	9.8406	2.8438	2.8338
07	2.4400	.3587	.8753	2.1016	.7539
10	1.5000	21.2058	31.8087	.8125	17.2297
11	1.5000	.3587	.5381	.8125	.2915
12	1.5000	.3587	.5381	.8125	.2915
13	1.5000	.9965	1.4948	.8125	.8097
14	1.5000	.9965	1.4948	.8125	.8097
16	1.5000	.3587	.5381	.8125	.2915
17	1.5000	.3587	.5381	.8125	.2915
20	2.0000	2.9895	5.9791	.8125	2.4290
21	2.0000	.3587	.7175	.8125	.2915
22	2.0000	.3587	.7175	.8125	.2915
23*	1.5000	3.9860	5.9791	.8125	3.2387
24*	1.5000	13.9512	20.9268	.8125	11.3353
25*	1.5000	.3587	.5381	.8125	.2915
26*	1.5000	.3587	.5381	.8125	.2915
27*	1.5000	.3587	.5381	.8125	.2915
32*	2.5000	.9965	2.4913	.8125	.8097
33*	2.5000	1.9930	4.9826	.8125	1.6193
34*	2.5000	.3587	.8969	1.9375	.6951
35*	2.5000	.3587	.8969	1.9375	.6951
36*	2.5000	.3587	.8969	1.9375	.6951
37*	2.5000	.3587	.8969	1.9375	.6951
40	7.5000	1.9930	14.9477	.8125	1.6193
41	14.5000	.3587	5.2018	5.0000	1.7937
42	1.5000	2.9895	4.4843	.8125	2.4290
43	2.0000	.3587	.7175	.8125	.2915
44	1.5000	5.9791	8.9686	.8125	4.8580
45	1.5000	.3587	.5381	.8125	.2915
46	1.5000	.3587	.5381	.8125	.2915
47	1.5000	.3587	.5381	.8125	.2915
50	2.0000	.3587	.7175	1.3125	.4709
51	1.5000	1.9930	2.9895	1.3125	2.6158
52	1.6500	3.9860	6.5770	1.3125	5.2317
53*	1.8750	14.9477	28.0269	1.3125	19.6188
54	1.5000	.0000	.0000	.8125	.0000
55	1.5000	.0000	.0000	.8125	.0000
56*	1.5000	.9965	1.4948	.8125	.8097
57*	1.5000	.0000	.0000	.8125	.0000
60*	1.7500	.9965	1.7439	.8125	.8097
61	1.7500	.9965	1.7439	.8125	.8097
62	1.7500	.9965	1.7439	.8125	.8097
63	1.7500	.3587	.6278	.8750	.3139
64	1.7500	.3587	.6278	.8125	.2915
65	1.7500	.3587	.6278	.8125	.2915
66	1.7500	.3587	.6278	.8125	.2915
67	1.7500	.9965	1.7439	.8750	.8719
70	1.6750	.3587	.6009	.9219	.3307
71	1.0000	.9965	.9965	.8125	.8097
74+	5.6800	.3587	2.0377	2.4844	.8913
77	2.5830	.0000	.0000	1.8750	.0000

BASED ON THE PRECEEDING TABLE, THE PERFORMANCE IS 996.7660 KIPS
WHICH IS 1.9694 TIMES THE PERFORMANCE OF THE AN/UYK-7. 4/20/81

INSTRUCTION COUNT METHOD BENCHMARK TYPE CC, CORE MEMORY.
* CONTAINS STORE OPERATIONS
+ CONTAINS SQUARE ROOT

PERFORMANCE DATA (Continued)

MAJOR FUNCTION CODE	AN/UYK-7(V) EXECUTION TIME	WEIGHT FACTOR %	AN/UYK-7(V) WEIGHTED TIME	AN/UYK-43 EXECUTION TIME	AN/UYK-43 WEIGHTED TIME
01	1.5000	.3488	.5232	1.5000	.5232
02*	2.7900	1.9930	5.5605	1.5179	3.0251
03*	2.5000	.3587	.8969	2.5000	.8969
05*	3.5500	1.9930	7.0752	2.5000	4.9826
06	9.8750	.9965	9.8406	2.8750	2.8650
07	2.4400	.3587	.8753	2.3594	.8464
10	1.5000	21.2058	31.8087	1.5000	31.8087
11	1.5000	.3587	.5381	1.5000	.5381
12	1.5000	.3587	.5381	1.5000	.5381
13	1.5000	.9965	1.4948	1.5000	1.4948
14	1.5000	.9965	1.4948	1.5000	1.4948
16	1.5000	.3587	.5381	1.5000	.5381
17	1.5000	.3587	.5381	1.5000	.5381
20	2.0000	2.9895	5.9791	1.5000	4.4843
21	2.0000	.3587	.7175	1.5000	.5381
22	2.0000	.3587	.7175	1.5000	.5381
23*	1.5000	3.9860	5.9791	1.7500	6.9756
24*	1.5000	13.9512	20.9268	1.7500	24.4145
25*	1.5000	.3587	.5381	1.7500	.6278
26*	1.5000	.3587	.5381	1.7500	.6278
27*	1.5000	.3587	.5381	1.7500	.6278
32*	2.5000	.9965	2.4913	1.7500	1.7439
33*	2.5000	1.9930	4.9826	1.7500	3.4878
34*	2.5000	.3587	.8969	1.7500	.6278
35*	2.5000	.3587	.8969	1.7500	.6278
36*	2.5000	.3587	.8969	1.7500	.6278
37*	2.5000	.3587	.8969	1.7500	.6278
40	7.5000	1.9930	14.9477	1.5000	2.9895
41	14.5000	.3587	5.2018	5.0000	1.7937
42	1.5000	2.9895	4.4843	1.5000	4.4843
43	2.0000	.3587	.7175	1.5000	.5381
44	1.5000	5.9791	8.9686	1.5000	8.9686
45	1.5000	.3587	.5381	1.5000	.5381
46	1.5000	.3587	.5381	1.5000	.5381
47	1.5000	.3587	.5381	1.5000	.5381
50	2.0000	.3587	.7175	1.5000	.5381
51	1.5000	1.9930	2.9895	1.5000	2.9895
52	1.6500	3.9860	6.5770	1.5000	5.9791
53*	1.8750	14.9477	28.0269	1.5469	23.1222
54	1.5000	.0000	.0000	1.5000	.0000
55	1.5000	.0000	.0000	1.5000	.0000
56*	1.5000	.9965	1.4948	1.5000	1.4948
57*	1.5000	.0000	.0000	1.5000	.0000
60*	1.7500	.9965	1.7439	1.5000	1.4948
61	1.7500	.9965	1.7439	1.5000	1.4948
62	1.7500	.9965	1.7439	1.5000	1.4948
63	1.7500	.3587	.6278	1.5000	.5381
64	1.7500	.3587	.6278	1.5000	.5381
65	1.7500	.3587	.6278	1.5000	.5381
66	1.7500	.3587	.6278	1.5000	.5381
67	1.7500	.9965	1.7439	1.5000	1.4948
70	1.6750	.3587	.6009	1.5000	.5381
71	1.0000	.9965	.9965	1.5000	1.4948
74+	5.6800	.3587	2.0377	3.0000	1.0762
77	2.5830	.0000	.0000	2.2083	.0000

BASED ON THE PRECEEDING TABLE , THE PERFORMANCE IS 615.6887 KIPS
WHICH IS 1.2165 TIMES THE PERFORMANCE OF THE AN/UYK-7. 4/20/81

INSTRUCTION COUNT METHOD BENCHMARK TYPE IS, SCM WITH REFRESH PENALTY.
* CONTAINS STORE OPERATIONS OVER CIS INTERFACE.
\+ CONTAINS SQUARE ROOT

PERFORMANCE DATA (Continued)

MAJOR FUNCTION CODE	AN/UYK-7(V) EXECUTION TIME	WEIGHT FACTOR %	AN/UYK-7(V) WEIGHTED TIME	AN/UYK-43 EXECUTION TIME	AN/UYK-43 WEIGHTED TIME
01	1.5000	.3488	.5232	.3750	.1308
02*	2.7900	1.9930	5.5605	.7286	1.4521
03*	2.5000	.3587	.8969	.8094	.2904
05*	3.5500	1.9930	7.0752	.8500	1.6941
06	9.8750	.9965	9.8406	2.8438	2.8338
07	2.4400	.3587	.8753	2.0000	.7175
10	1.5000	21.2058	31.8087	.3750	7.9522
11	1.5000	.3587	.5381	.5000	.1794
12	1.5000	.3587	.5381	.3750	.1345
13	1.5000	.9965	1.4948	.3750	.3737
14	1.5000	.9965	1.4948	.3750	.3737
16	1.5000	.3587	.5381	.3750	.1345
17	1.5000	.3587	.5381	.5000	.1794
20	2.0000	2.9895	5.9791	.3750	1.1211
21	2.0000	.3587	.7175	.3750	.1345
22	2.0000	.3587	.7175	.3750	.1345
23*	1.5000	3.9860	5.9791	.7500	2.9895
24*	1.5000	13.9512	20.9268	.7500	10.4634
25*	1.5000	.3587	.5381	.7500	.2691
26*	1.5000	.3587	.5381	.7500	.2691
27*	1.5000	.3587	.5381	.7500	.2691
32*	2.5000	.9965	2.4913	.7500	.7474
33*	2.5000	1.9930	4.9826	.7500	1.4948
34*	2.5000	.3587	.8969	.8000	.2870
35*	2.5000	.3587	.8969	.8000	.2870
36*	2.5000	.3587	.8969	.8000	.2870
37*	2.5000	.3587	.8969	.8000	.2870
40	7.5000	1.9930	14.9477	.6250	1.2456
41	14.5000	.3587	5.2018	5.0000	1.7937
42	1.5000	2.9895	4.4843	.5000	1.4948
43	2.0000	.3587	.7175	.5000	.1794
44	1.5000	5.9791	8.9686	.3750	2.2422
45	1.5000	.3587	.5381	.5000	.1794
46	1.5000	.3587	.5381	.3750	.1345
47	1.5000	.3587	.5381	.5000	.1794
50	2.0000	.3587	.7175	.7500	.2691
51	1.5000	1.9930	2.9895	.7500	1.4948
52	1.6500	3.9860	6.5770	.7500	2.9895
53*	1.8750	14.9477	28.0269	.7500	11.2108
54	1.5000	.0000	.0000	.3750	.0000
55	1.5000	.0000	.0000	.3750	.0000
56*	1.5000	.9965	1.4948	.5000	.4983
57*	1.5000	.0000	.0000	.5000	.0000
60*	1.7500	.9965	1.7439	.3750	.3737
61	1.7500	.9965	1.7439	.3750	.3737
62	1.7500	.9965	1.7439	.3750	.3737
63	1.7500	.3587	.6278	.8750	.3139
64	1.7500	.3587	.6278	.3750	.1345
65	1.7500	.3587	.6278	.6250	.2242
66	1.7500	.3587	.6278	.3750	.1345
67	1.7500	.9965	1.7439	.8750	.8719
70	1.6750	.3587	.6009	.5938	.2130
71	1.0000	.9965	.9965	.3750	.3737
74+	5.6800	.3587	2.0377	2.2344	.8016
77	2.5830	.0000	.0000	1.8750	.0000

BASED ON THE PRECEEDING TABLE, THE PERFORMANCE IS 1572.6710 KIPS
WHICH IS 3.1073 TIMES THE PERFORMANCE OF THE AN/UYK-7. 4/20/81

INSTRUCTION COUNT METHOD BENCHMARK TYPE IC, MONO FRONTED CORE MEMORY.
* CONTAINS STORE OPERATIONS
+ CONTAINS SQUARE ROOT

PERFORMANCE DATA (Continued)

MAJOR FUNCTION CODE	AN/UYK-7(V) EXECUTION TIME	WEIGHT FACTOR %	AN/UYK-7(V) WEIGHTED TIME	AN/UYK-43 EXECUTION TIME	AN/UYK-43 WEIGHTED TIME
01	1.5000	.4553	.6830	.2969	.1352
02*	2.7900	1.5387	4.2929	.5536	.8518
03*	2.5000	.4103	1.0258	.6875	.2821
05*	3.5500	2.1058	7.4755	.7000	1.4740
06	9.8750	1.3010	12.8473	2.8438	3.6997
07	2.4400	.4684	1.1428	1.9844	.9296
10	1.5000	27.6851	41.5276	.2500	6.9213
11	1.5000	.4684	.7025	.5000	.2342
12	1.5000	.4684	.7025	.2500	.1171
13	1.5000	1.3010	1.9515	.2500	.3252
14	1.5000	1.3010	1.9515	.2500	.3252
16	1.5000	.4684	.7025	.2500	.1171
17	1.5000	.4684	.7025	.5000	.2342
20	2.0000	3.9030	7.8059	.2500	.9757
21	2.0000	.4684	.9367	.2500	.1171
22	2.0000	.4684	.9367	.2500	.1171
23*	1.5000	.4837	.7256	.3750	.1814
24*	1.5000	5.9254	8.8880	.3750	2.2220
25*	1.5000	.0039	.0059	.3750	.0015
26*	1.5000	.0039	.0059	.3750	.0015
27*	1.5000	.0039	.0059	.6250	.0024
32*	2.5000	.0302	.0756	.7500	.0227
33*	2.5000	.1209	.3023	.7500	.0907
34*	2.5000	.0039	.0098	.6250	.0024
35*	2.5000	.0039	.0098	.6250	.0024
36*	2.5000	.0039	.0098	.6250	.0024
37*	2.5000	.0039	.0098	.6250	.0024
40	7.5000	2.6020	19.5149	.6250	1.6262
41	14.5000	.4684	6.7912	5.0000	2.3418
42	1.5000	3.9030	5.8545	.5000	1.9515
43	2.0000	.4684	.9367	.5000	.2342
44	1.5000	7.8059	11.7089	.2500	1.9515
45	1.5000	.4684	.7025	.5000	.2342
46	1.5000	.4684	.7025	.3750	.1756
47	1.5000	.4684	.7025	.5000	.2342
50	2.0000	.4684	.9367	.5000	.2342
51	1.5000	2.6020	3.9030	.3750	.9757
52	1.6500	5.2040	8.5865	.4688	2.4394
53*	1.8750	17.1312	32.1210	.4063	6.9596
54	1.5000	.0000	.0000	.3750	.0000
55	1.5000	.0000	.0000	.3750	.0000
56*	1.5000	.0302	.0453	.5000	.0151
57*	1.5000	.0000	.0000	.5000	.0000
60*	1.7500	.0302	.0529	.3750	.0113
61	1.7500	1.3010	2.2767	.3750	.4879
62	1.7500	1.3010	2.2767	.2500	.3252
63	1.7500	.4684	.8196	.8750	.4098
64	1.7500	.4684	.8196	.2500	.1171
65	1.7500	.4684	.8196	.6250	.2927
66	1.7500	.4684	.8196	.2500	.1171
67	1.7500	1.3010	2.2767	.8750	1.1384
70	1.6750	.4684	.7845	.5625	.2635
71	1.0000	1.3010	1.3010	.3750	.4879
74+	5.6800	.4684	2.6603	2.2344	1.0465
77	2.5830	.0000	.0000	1.8750	.0000

BASED ON THE PRECEEDING TABLE , THE PERFORMANCE IS 2301.0314 KIPS
WHICH IS 4.6676 TIMES THE PERFORMANCE OF THE AN/UYK-7. 4/20/81

INSTRUCTION COUNT METHOD BENCHMARK TYPE 11, CACHE MEMORY.
* CONTAINS STORE OPERATIONS REDUCED TO 8 PERCENT FOR UYK-7 AND UYK-43.
+ CONTAINS SQUARE ROOT

PERFORMANCE DATA (Continued)

MAJOR FUNCTION CODE	AN/UYK-7(V) EXECUTION TIME	WEIGHT FACTOR %	AN/UYK-7(V) WEIGHTED TIME	AN/UYK-43 EXECUTION TIME	AN/UYK-43 WEIGHTED TIME
01	1.5000	.3488	.5232	.3750	.1308
02*	2.7900	1.9930	5.5605	.7286	1.4521
03*	2.5000	.3587	.8969	.8094	.2904
05*	3.5500	1.9930	7.0752	.8500	1.6941
06	9.8750	.9965	9.8406	2.8438	2.8338
07	2.4400	.3587	.8753	2.0000	.7175
10	1.5000	21.2058	31.8087	.3750	7.9522
11	1.5000	.3587	.5381	.5000	.1794
12	1.5000	.3587	.5381	.3750	.1345
13	1.5000	.9965	1.4948	.3750	.3737
14	1.5000	.9965	1.4948	.3750	.3737
16	1.5000	.3587	.5381	.3750	.1345
17	1.5000	.3587	.5381	.5000	.1794
20	2.0000	2.9895	5.9791	.3750	1.1211
21	2.0000	.3587	.7175	.3750	.1345
22	2.0000	.3587	.7175	.3750	.1345
23*	1.5000	3.9860	5.9791	.7500	2.9895
24*	1.5000	13.9512	20.9268	.7500	10.4634
25*	1.5000	.3587	.5381	.7500	.2691
26*	1.5000	.3587	.5381	.7500	.2691
27*	1.5000	.3587	.5381	.7500	.2691
32*	2.5000	.9965	2.4913	.7500	.7474
33*	2.5000	1.9930	4.9826	.7500	1.4948
34*	2.5000	.3587	.8969	.8000	.2870
35*	2.5000	.3587	.8969	.8000	.2870
36*	2.5000	.3587	.8969	.8000	.2870
37*	2.5000	.3587	.8969	.8000	.2870
40	7.5000	1.9930	14.9477	.6250	1.2456
41	14.5000	.3587	5.2018	5.0000	1.7937
42	1.5000	2.9895	4.4843	.5000	1.4948
43	2.0000	.3587	.7175	.5000	.1794
44	1.5000	5.9791	8.9686	.3750	2.2422
45	1.5000	.3587	.5381	.5000	.1794
46	1.5000	.3587	.5381	.3750	.1345
47	1.5000	.3587	.5381	.5000	.1794
50	2.0000	.3587	.7175	.7500	.2691
51	1.5000	1.9930	2.9895	.7500	1.4948
52	1.6500	3.9860	6.5770	.7500	2.9895
53*	1.8750	14.9477	28.0269	.7500	11.2108
54	1.5000	.0000	.0000	.3750	.0000
55	1.5000	.0000	.0000	.3750	.0000
56*	1.5000	.9965	1.4948	.5000	.4983
57*	1.5000	.0000	.0000	.5000	.0000
60*	1.7500	.9965	1.7439	.3750	.3737
61	1.7500	.9965	1.7439	.3750	.3737
62	1.7500	.9965	1.7439	.3750	.3737
63	1.7500	.3587	.6278	.8750	.3139
64	1.7500	.3587	.6278	.3750	.1345
65	1.7500	.3587	.6278	.6250	.2242
66	1.7500	.3587	.6278	.3750	.1345
67	1.7500	.9965	1.7439	.8750	.8719
70	1.6750	.3587	.6009	.5938	.2130
71	1.0000	.9965	.9965	.3750	.3737
74+	5.6800	.3587	2.0377	2.2344	.8016
77	2.5830	.0000	.0000	1.8750	.0000

BASED ON THE PRECEEDING TABLE, THE PERFORMANCE IS 1572.6710 KIPS
WHICH IS 3.1073 TIMES THE PERFORMANCE OF THE AN/UYK-7. 4/20/81

INSTRUCTION COUNT METHOD BENCHMARK TYPE I, SCM WITH REFRESH PENALTY.
* CONTAINS STORE OPERATIONS
+ CONTAINS SQUARE ROOT

PERFORMANCE DATA (Continued)

61		LD TSK CMR WTH I=0A	4A	1	1.75	.3750	3	.3750	.3750	1.5000	.8125
61		LD INT CMR WTH I=1A	4A	1	1.75	.3750	3	.3750	.3750	1.5000	.8125
62		SHIFT LEFT CIRC	4B	10	1.75	.2500	2	.3750	.3750	1.5000	.8125
63		DOUBLE SHIFT L CIRC	4B	10	1.75	.8750	7	.8750	.8750	1.5000	.8750
64		SHIFT RT FILL 0	4B	10	1.75	.2500	2	.3750	.3750	1.5000	.8125
65		DOUBLE SH RT FILL 0	4B	10	1.75	.6250	5	.6250	.6250	1.5000	.8125
66		SHIFT RT FILL SIGN	4B	10	1.75	.2500	2	.3750	.3750	1.5000	.8125
67		DOUBLE SH RT FILL S	4B	10	1.75	.8750	7	.8750	.8750	1.5000	.8750
70	0	SCALE FACTOR	4A	2+10	2.25	.3750	3	.3750	.3750	1.5000	.8125
70	1	DOUBLE SCALE FACTOR	4A	2+10	2.25	1.2500	10	1.2500	1.2500	1.5000	1.2500
70	2	COMPLEMENT A	4A	11	1.1	.2500	2	.3750	.3750	1.5000	.8125
70	3	DOUBLE COMPLEMENT A	4A	11	1.1	.3750	3	.3750	.3750	1.5000	.8125
70	5	CIS REQ ID (DIO)	4A	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
71	0	INCLUSIVE OR A	4A	11	1.0	.3750	3	.3750	.3750	1.5000	.8125
71	1	ADD (SUM)	4A	2	1.0	.3750	3	.3750	.3750	1.5000	.8125
71	2	ADD NEGATIVE	4A	2	1.0	.3750	3	.3750	.3750	1.5000	.8125
71	3	EXCLUSIVE OR A	4A	11	1.0	.3750	3	.3750	.3750	1.5000	.8125
71	4	CPU MON CLK CONTROL	4A	Z	N	1.0000	8	1.0000	1.0000	1.5000	1.0000
71	5	AND A	4A	11	1.0	.3750	3	.3750	.3750	1.5000	.8125
71	6	IOC MON CLK CTR I=0L	4A	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
71	6	IOC RTC CONTROL I=1	4A	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
74	0	MULTIPLY (REG)	4A	8	7.75	.7500	6	.7500	.7500	1.5000	.8125
74	1	DIVIDE (REG)	4A	9	15.0	5.0000	40	5.0000	5.0000	5.0000	5.0000
74	2	SQUARE ROOT (REG)	4A	V	15.0	10.0000	80	10.0000	10.0000	10.0000	10.0000
74	3	LOAD BA WITH BB	4A	1	1.75	.3750	3	.3750	.3750	1.5000	.8125
74	4	COMPARE A	4A	3	1.1	.5000	4	.5000	.5000	1.5000	.8125
74	5	COMP A WITHIN LIMITS	4A	3	1.75	.5000	4	.5000	.5000	1.5000	.8125
74	6	COMP A WITH MASK	4A	3	1.1	.3750	3	.3750	.3750	1.5000	.8125
74	7	COMPARE BB WITH BA	4A	3	2.0	.3750	3	.3750	.3750	1.5000	.8125
76	0	CLEAR BIT N F4=0	4S	*1+11	N	.5000	4	.5000	.5000	1.5000	.8125
76	1	SET BIT N F4=1	4S	*1+11	N	.5000	4	.5000	.5000	1.5000	.8125
76	2	TEST BIT N F4=2	4S	*1+11	N	.5000	4	.5000	.5000	1.5000	.8125
76	3	TEST, SET BIT N F4=3	4S	*1+11	N	.6250	5	.6250	.6250	1.5000	.8125
77	0	STORE I/O MON CLK	4A	X	3.0	3.6250	29	3.6250	3.6250	3.6250	3.6250
77	1	STORE REAL TIME CLK	4A	X	3.5	3.6250	29	3.6250	3.6250	3.6250	3.6250
77	2	ST/DIS MON CLK I=0	4A	Z	N	1.0000	8	1.0000	1.0000	1.5000	1.0000
77	2	CONFIDENCE TEST I=1	4A	NA	N		N	N	N	N	N
77	3	IOC CLEAR CLK I=1	4A	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
77	4	PREVENT CLS 3 INTER	4A	Z	2.25	1.0000	8	1.0000	1.0000	1.5000	1.0000
77	5	ALLOW CLASS 3 INTER	4A	Z	2.25	1.0000	8	1.0000	1.0000	1.5000	1.0000
77	6	STOP PROCESSOR I=0	4A	Z	2.25	1.0000	8	1.0000	1.0000	1.5000	1.0000
77	6	WAIT FOR INTER I=1	4A	Z	2.25	1.0000	8	1.0000	1.0000	1.5000	1.0000
77	7	P HIST ENABLE I=0	4A	Z	N	1.0000	8	1.0000	1.0000	1.5000	1.0000
77	7	P HIST DISABLE I=1	4A	Z	N	1.0000	8	1.0000	1.0000	1.5000	1.0000

PERFORMANCE DATA (Continued)

06	7	FP DIV WITH ROUND	2	7	17.0	5.5000	44	5.5000	5.5000	5.5000	5.5000
07	00	ENT EXC STATE A=0	2	1+12	2.1	.6250	5	.6250	.6250	1.5000	.8125
07	10	INTERPROC INT A=1	2	W		2.8750	23	2.8750	2.8750	2.8750	2.8750
07	1	ALLOW EXT INT	2	W	2.0	2.9750	23	2.8750	2.8750	2.8750	2.8750
07	2	PREVENT EXT INT	2	W	2.0	2.8750	23	2.8750	2.8750	2.8750	2.8750
07	3	LOAD ENAB MON CLK	2	W	3.0	2.9750	23	2.8750	2.8750	2.8750	2.8750
07	4	INITIATE I/O	2	W	3.5	2.8750	23	2.8750	2.8750	2.8750	2.8750
07	5	INTERRUPT RETURN	2	12+1	3.0	.6250	5	.6250	.6250	1.5000	.8125
07	6	REPEAT	2	13	1.5	.2500	2	.3750	.3750	1.5000	.8125
07	7	CHANNEL CLEAR I=0	2	W		2.8750	23	2.8750	2.8750	2.8750	2.8750
07	7	P HIST FILE RD I=1	2	Z		1.0000	8	1.0000	1.0000	1.5000	1.0000
10		LOAD A	1	1	1.5	.2500	2	.3750	.3750	1.5000	.8125
11		LOAD A AND INDEX B	1	1+13	1.5	.5000	4	.5000	.5000	1.5000	.8125
12		LOAD DIFF (Y-A)	1	2	1.5	.2500	2	.3750	.3750	1.5000	.8125
13		ADD NEG A	1	2	1.5	.2500	2	.3750	.3750	1.5000	.8125
14		ADD A	1	2	1.5	.2500	2	.3750	.3750	1.5000	.8125
15		LOAD SUM (Y+A)	1	2	1.5	.2500	2	.3750	.3750	1.5000	.8125
16		LOAD NEGATIVE	1	1	1.5	.2500	2	.3750	.3750	1.5000	.8125
17		LOAD MAGNITUDE	1	1	1.5	.5000	4	.5000	.5000	1.5000	.8125
20		LOAD B	1	1	2.0	.2500	2	.3750	.3750	1.5000	.8125
21		ADD B	1	2	2.0	.2500	2	.3750	.3750	1.5000	.8125
22		ADD NEGATIVE B	1	2	2.0	.2500	2	.3750	.3750	1.5000	.8125
23		STORE B	1	1*	1.5	.3750	3	.7500	.7500	1.7500	.8125
24		STORE A	1	1*	1.5	.3750	3	.7500	.7500	1.7500	.8125
25		STORE A, INDEX B	1	*1+13	1.5	.3750	3	.7500	.7500	1.7500	.8125
26		STORE COMPLEMENT	1	1*	1.5	.3750	3	.7500	.7500	1.7500	.8125
27		STORE MAGNITUDE	1	1*	1.5	.6250	5	.7500	.7500	1.7500	.8125
30	OK	REP IF +, DEC A=0	1	1+2		.6250	5	.7500	.7500	1.7500	.8125
31		BP CONTROL (DIO)	1	L		2.6250	21	2.6250	2.6250	2.6250	2.6250
32		CLEAR BIT	1	*1+11	2.5	.7500	6	.7500	.7500	1.7500	.8125
33	AK	SET BIT A=0-33	1	*1+11	2.5	.7500	6	.7500	.7500	1.7500	.8125
33	AK	TST + SET BIT A=4-77	1	1+11		1.0000	6+2	1.0000	1.0000	1.7500	1.0000
34		REPLACE ADD	1	*1+2	2.5	.6250	3+2	.8000	.8000	1.7500	1.9375
35		REPLACE INCREMENT	1	*1+2	2.5	.6250	3+2	.8000	.8000	1.7500	1.9375
36		REPLACE ADD NEG	1	*1+2	2.5	.6250	3+2	.8000	.8000	1.7500	1.9375
37		REPLACE DECREMENT	1	*1+2	2.5	.6250	3+2	.8000	.8000	1.7500	1.9375
40		MULTIPLY A	1	8	7.5	.6250	5	.6250	.6250	1.5000	.8125
41		DIVIDE A	1	9	14.5	5.0000	40	5.0000	5.0000	5.0000	5.0000
42		COMPARE BIT TO 0	1	3	1.5	.5000	4	.5000	.5000	1.5000	.8125
43		COMPARE INDEX INCR	1	3+13	2.0	.5000	4	.5000	.5000	1.5000	.8125
44		COMPARE	1	3	1.5	.2500	2	.3750	.3750	1.5000	.8125
45		COMP WITHIN LIMITS	1	3	1.5	.5000	4	.5000	.5000	1.5000	.8125
46		COMP WITH MASK	1	3+11	1.5	.3750	3	.3750	.3750	1.5000	.8125
47		COMPARE GATED	1	3+2	1.5	.5000	4	.5000	.5000	1.5000	.8125
50	0	JUMP EVEN PARITY	3	4	2.0	.5000	4	.7500	.7500	1.5000	1.3125
50	1	JUMP ODD PARITY	3	4	2.0	.5000	4	.7500	.7500	1.5000	1.3125
50	2	DOUBLE JMP A EQ 0	3	4	2.0	.5000	4	.7500	.7500	1.5000	1.3125
50	3	DOUBLE JMP A NE 0	3	4	2.0	.5000	4	.7500	.7500	1.5000	1.3125
51	0	JUMP A POSITIVE	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
51	1	JUMP A NEGATIVE	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
51	2	JUMP A ZERO	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
51	3	JUMP A NOT ZERO	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
52	0	LOAD B AND JUMP	3	1+12	1.5	.5000	4	.7500	.7500	1.5000	1.3125
52	1	JUMP B NOT ZERO	3	13+4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
52	2	JUMP SY+B	3	12	1.8	.5000	4	.7500	.7500	1.5000	1.3125
52	3	JUMP LOWER	3	12	1.8	.5000	4	.7500	.7500	1.5000	1.3125
53	00	JUMP NO OVFL UNCOND	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	10	JUMP OVERFLOW	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	60	PERF MON MEMORY A=6	3	Z		1.0000	8	1.0000	1.0000	1.5000	1.3125
53	70	PERF MON REGS A=7	3	Z		1.0000	8	1.0000	1.0000	1.5000	1.3125
53	01	JUMP NOT EQUAL	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	11	JUMP EQUAL	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	21	JUMP GREATER THAN	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	31	JUMP GT OR EQUAL	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	41	JUMP LESS THAN	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	51	JUMP LT OR EQUAL	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	61	JMP NOT WITHIN LIM	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	71	JMP WITHIN LIMITS	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	02	RETURN JUMP A=0	3	12+1*	3.0	.5000	4	.7500	.7500	1.7500	1.3125
53	A2	RET JMP COND A=1-3	3	4+1*	3.0	.5000	4	.7500	.7500	1.7500	1.3125
53	A2	RET JMP ST C A=4-7	3	4+1*	3.75	.5000	4	.7500	.7500	1.7500	1.3125
53	03	MANUAL JUMP A=0	3	12	1.5	.5000	4	.7500	.7500	1.5000	1.3125
53	A3	JMP COND SET A=1-3	3	4	1.5	.3750	3	.7500	.7500	1.5000	1.3125
53	A3	JMP STOP C S A=4-7	3	4	2.25	.3750	3	.7500	.7500	1.5000	1.3125
54		LOAD TASK CMR	1	1	1.5	.3750	3	.3750	.3750	1.5000	.8125
55		LOAD INTR CMR	1	1	1.5	.3750	3	.3750	.3750	1.5000	.8125
56		STORE TASK CMR	1	1*	1.5	.5000	4	.5000	.5000	1.5000	.8125
57		STORE INTR CMR	1	1*	1.5	.5000	4	.5000	.5000	1.5000	.8125
60		ST TSK CMR IN A I=0	4A	1*	1.75	.3750	3	.3750	.3750	1.5000	.8125
60		ST INT CMR IN A I=1	4A	1*	1.75	.3750	3	.3750	.3750	1.5000	.8125

PERFORMANCE DATA (Continued)

EXTENDED INSTRUCTION LIST 04/20/81

FUNCTION CODE		INSTRUCTION NAME	FORMAT	MIX	OLD TIME (USEC)	CACHE (USEC)	CYCLES	TYPE I BENCHMARK DATA SCM TIME (USEC)	MONO-CORE TIME (USEC)	CIS TIME (USEC)	CORE TIME (USEC)
01	0	INCLUSIVE OR	2	11	1.5	.2500	2	.3750	.3750	1.5000	.8125
01	1	SELECTIVE CLEAR	2	11	1.5	.2500	2	.3750	.3750	1.5000	.8125
01	2	MASKED SEL SUBS	2	11	1.5	.3750	3	.3750	.3750	1.5000	.8125
01	3	EXCLUSIVE OR	2	11	1.5	.2500	2	.3750	.3750	1.5000	.8125
01	4	ADD LOGICAL PROD	2	11+?	1.5	.3750	3	.3750	.3750	1.5000	.8125
01	5	LOAD LOGICAL PROD	2	11	1.5	.2500	2	.3750	.3750	1.5000	.8125
01	6	ADD NEG LOGI PROD	2	11+2	1.5	.3750	3	.3750	.3750	1.5000	.8125
01	7	LOAD L PROD NEXT	2	11	1.5	.2500	2	.3750	.3750	1.5000	.8125
02	0	COUNT ONES	2	1+2+3+10	7.5	.7500	6	.7500	.7500	1.5000	.8125
02	2	EXECUTE REMOTE	2	12	1.5	.5000	4	.5000	.5000	1.5000	.8125
02	3	EXECUTE REMOTE L	2	12	1.5	.5000	4	.5000	.5000	1.5000	.8125
02	4	STORE LOGI PROD	2	11+2	2.0	.5000	4	.7500	.7500	1.5000	.8125
02	5	STORE SUM	2	2+1*	2.0	.5000	4	.7500	.7500	1.5000	.8125
02	6	STORE DIFFERENCE	2	2+1*	2.0	.5000	4	.7500	.7500	1.5000	.8125
02	7	DOUBLE STORE A	2	1+1*	3.0	.6250	5	1.1000	1.1000	1.6250	1.6250
03	0	REPL INCLUSIVE OR	2	1+1*	2.5	.6250	3+2	.8000	.8000	2.5000	1.9375
03	1	REPL SELECT CLEAR	2	*1+11	2.5	.6250	3+2	.8000	.8000	2.5000	1.9375
03	2	R MASKED SEL SUBS	2	*1+11	2.5	.8750	5+2	.8750	.8750	2.5000	1.9375
03	3	REPL EXCLUSIVE OR	2	*1+11	2.5	.6250	3+2	.8000	.8000	2.5000	1.9375
03	4	P ADD LOGI PROD	2	*1+11+2	2.5	.7500	4+2	.8000	.8000	2.5000	1.9375
03	5	REPL LOGICAL PROD	2	*1+11	2.5	.6250	3+2	.8000	.8000	2.5000	1.9375
03	6	R ADD NEG L PROD	2	*1+11+2	2.5	.7500	4+2	.8000	.8000	2.5000	1.9375
03	7	TEST AND SET FLAG	2	3+11	2.5	.6250	3+2	.8000	.8000	2.5000	1.9375
04	0	IOC CAR TO A	2	X	N	3.6250	29	3.6250	3.6250	3.6250	3.6250
04	1	IOC CAP REGS TO A	2	X	N	3.6250	29	3.6250	3.6250	3.6250	3.6250
04	2	IOC M P REGS TO A	2	Y	N	3.8750	31	3.8750	3.8750	3.8750	3.8750
04	3	IOC B P REGS TO A	2	Y	N	3.8750	31	3.8750	3.8750	3.8750	3.8750
04	4	ST A IN IOC CAR	2	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
04	5	ST A IN IOC CAP REG	2	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
04	6	ST A IN IOC M P REG	2	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
04	7	ST A IN IOC B P REG	2	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
05	0	DOUBLE LOAD A	2	1+11	3.0	.5000	4	.7500	.7500	2.7500	1.6250
05	1	DOUBLE ADD A	2	2+2	3.0	.6250	5	.7500	.7500	2.7500	1.6250
05	2	DOUBLE ADD NEG A	2	2+?	3.0	.6250	5	.7500	.7500	2.7500	1.6250
05	3	DOUBLE COMPARE	2	3+3	3.0	.5000	4	.7500	.7500	2.7500	1.6250
05	4	LOAD BASE AND MP	2	1+1+1*	5.75	1.2500	10	1.2500	1.2500	1.5000	1.2500
05	5	SET CIS M PROTECT	2	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
05	6 0	FP ADD (DP)	5	5	N	2.5000	20	2.5000	2.5000	2.5000	2.5000
05	6 1	FP SUBTRACT (DP)	5	5	N	2.5000	20	2.5000	2.5000	2.5000	2.5000
05	6 2	FP MULTIPLY (DP)	5	6	N	9.7500	78	9.7500	9.7500	9.7500	9.7500
05	6 3	FP DIVIDE (DP)	5	7	N	22.2500	178	22.2500	22.2500	22.2500	22.2500
05	6 4	FP ADD (SP)	5	5	N	1.5000	12	1.5000	1.5000	1.5000	1.5000
05	6 5	FP SUBTRACT (SP)	5	5	N	1.5000	12	1.5000	1.5000	1.5000	1.5000
05	6 6	FP MULTIPLY (SP)	5	6	N	2.3750	19	2.3750	2.3750	2.3750	2.3750
05	6 7	FP DIVIDE (SP)	5	7	N	4.0000	32	4.0000	4.0000	4.0000	4.0000
05	6 10	FP EXPONENTIAL (SP)	5	P	N	19.6250	157	19.6250	19.6250	19.6250	19.6250
05	6 11	FP NATURAL LOG (SP)	5	P+1+?	N	19.0000	152	19.0000	19.0000	19.0000	19.0000
05	6 12	TRIG VECTOR	5	R	N	8.8750	71	8.8750	8.8750	8.8750	8.8750
05	6 13	TRIG ROTATE	5	R	N	8.8750	71	8.8750	8.8750	8.8750	8.8750
05	6 14	HYPER VECTOR	5	R	N	8.8750	71	8.8750	8.8750	8.8750	8.8750
05	6 15	HYPER ROTATE	5	R	N	8.8750	71	8.8750	8.8750	8.8750	8.8750
05	6 16	FP SINCOS (SP)	5	P	N	10.1250	81	10.1250	10.1250	10.1250	10.1250
05	6 17	FP ARCSIN (SP)	5	Q	N	18.5000	148	18.5000	18.5000	18.5000	18.5000
05	6 20	FP ARCCOS (SP)	5	Q	N	18.5000	148	18.5000	18.5000	18.5000	18.5000
05	6 21	FP ARCTAN (SP)	5	P	N	12.0000	96	12.0000	12.0000	12.0000	12.0000
05	6 22	CONV BAMS TO RADS	5	S	N	3.1250	25	3.1250	3.1250	3.1250	3.1250
05	6 23	CONV RADS TO BAMS	5	S	N	3.1250	25	3.1250	3.1250	3.1250	3.1250
05	6 24	CONV FLOAT TO FIXED	5	1+11	N	.6250	5	.6250	.6250	1.5000	.8125
05	6 25	CONV FIXED TO FLOAT	5	1+1+5	N	.5000	4	.5000	.5000	1.5000	.8125
05	6 26	FLOAT TO FLOAT I=0	5	U	N	2.7500	22	2.7500	2.7500	2.7500	2.7500
05	6 26	FLOAT TO FLOAT I=1	5	1+1*+5+3	N	1.0000	8	1.0000	1.0000	1.5000	1.0000
05	7 00	PUSH STACK	5	1*+2	N	.3750	3	.3750	.3750	1.5000	.8125
05	7 01	POP STACK	5	1+2	N	.3750	3	.3750	.3750	1.5000	.8125
05	7 02	COMPARE STACK	5	3	N	.2500	2	.3750	.3750	1.5000	.8125
05	7 03	INCR STACK POINTER	5	2	N	.2500	2	.3750	.3750	1.5000	.8125
05	7 04	DECR STACK POINTER	5	2	N	.2500	2	.3750	.3750	1.5000	.8125
05	7 10	SET INTCMP TIMEOUT	5	W	N	2.8750	23	2.8750	2.8750	2.8750	2.8750
06	0	FP ADD	2	5	6.25	2.0000	16	2.0000	2.0000	2.0000	2.0000
06	1	FP ADD NEGATIVE	2	5	6.25	2.0000	16	2.0000	2.0000	2.0000	2.0000
06	2	FP MULTIPLY	2	6	10.0	1.2500	10	1.2500	1.2500	1.5000	1.2500
06	3	FP DIVIDE	2	7	17.0	5.3750	43	5.3750	5.3750	5.3750	5.3750
06	4	FP ADD WITH ROUND	2	5	6.25	2.2500	18	2.2500	2.2500	2.2500	2.2500
06	5	FP SUB WITH ROUND	2	5	6.25	2.2500	18	2.2500	2.2500	2.2500	2.2500
06	6	FP MPY WITH ROUND	2	6	10.0	2.1250	17	2.1250	2.1250	2.1250	2.1250

MISSION REQUIREMENT COMPLIANCE

Parameter	Purchase description requirements	Projected design	
		Core	SCM
R (2000 hours) for A encl	0.720	0.807	0.811
B encl	0.720	0.885	0.891
A (0) for A encl	0.90		
B encl	0.90		
MTBF (hours) A encl	6000	9,348	9,517
B encl	6000	16,335	17,329
MTTF (hours) A encl	2400	2,407	2,900
B encl	1050	1,154	1,378
Fault isolation			
To: 3 LRUs (A & B encl)	98%	98%	98%
2 LRUs (A & B encl)	95%	95%	95%
1 LRU (A & B encl)	90%	90%	90%

MAINTENANCE CONCERNS

- Basic Maintenance Action
- IOC/IOA Bus Fault Group

IBM

5065-4

IOC/IOA BUS FAULTS

- Concern: Failure Mechanisms which Disable the Bus and which Cannot be Readily Isolated
  - Stuck bus due to a failed transceiver shorting the bus to ground
  - Corrupted bus due to a transceiver being erroneously enabled
- Probable Incidence:
  - Each IOA 0.02665 failures per 10^6 hours
  - Each IOC 0.1933 failures per 10^6 hours

SIGNIFICANCE OF IOC/IOA BUS FAULTS

	A Enclosure	B Enclosure
Population	IOC + 24 IOA	2 (IOC + 32 IOA)
Failures/10^6 Hours	0.8329	2 (1.0461)
% of "Box" Failure Rate	0.110%	0.113%
Expected Incidents		
Per Box Per Year	0.005	0.0125
Per Box Per 20 Years	0.1	0.25

ON-LINE IOA REPLACEMENT

- Current Approach Calls for Quiescing the IOC/IOA for Repair
- No Electrical Problems Involved in Pulling/Plugging a Hot IOA
- Quiescing Avoids the Possibility of Bus Perturbations
- Electronic Quiescing of Individual IOA's to Allow Safe On-Line Repair was not Implemented in the EDM's Because:
  - Cost of different drivers and electronic switching was not justified in light of
  - Limited value of on-line I/O repair to system MTBF
  - Observation that a high availability/fault tolerant system provides redundant IOC/IOA's, and that, if IO repair is normal, it is very unlikely that the redundant IOC/IOA would contain a fault and be unable to cover for the IOC/IOA to be quiesced and repaired.

OVERALL PURCHASE DESCRIPTION COMPLIANCE

COMPLY WITH P.D. IN ALL AREAS EXCEPT:

• Weight	P.D.	Project Design
A Encl	500 lbs	569 lbs
B Encl	750 lbs	1071 lbs

• ISA Growth	P.D.	Project Design
(Spare Microstructure	40% Spare ISA Microstore for Maintenance	31% Total* Spare Locations
	20% ISA + Maintenance Microstore for ISA Extensions	

*Does not include 1024 words of read/write diagnostic microstore

IBM

5065-7

MIL-STD DEVIATIONS

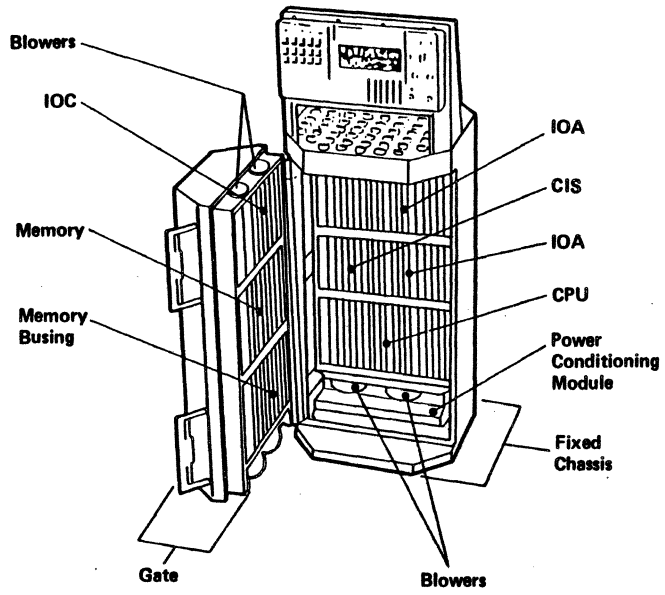
- 64K Dynamic RAM
- MIL-E-16400
  - Line Width
  - Conformal Coat Thickness
  - Non-Standard Parts

IBM

5065-6

MECHANICAL PACKAGING OVERVIEW

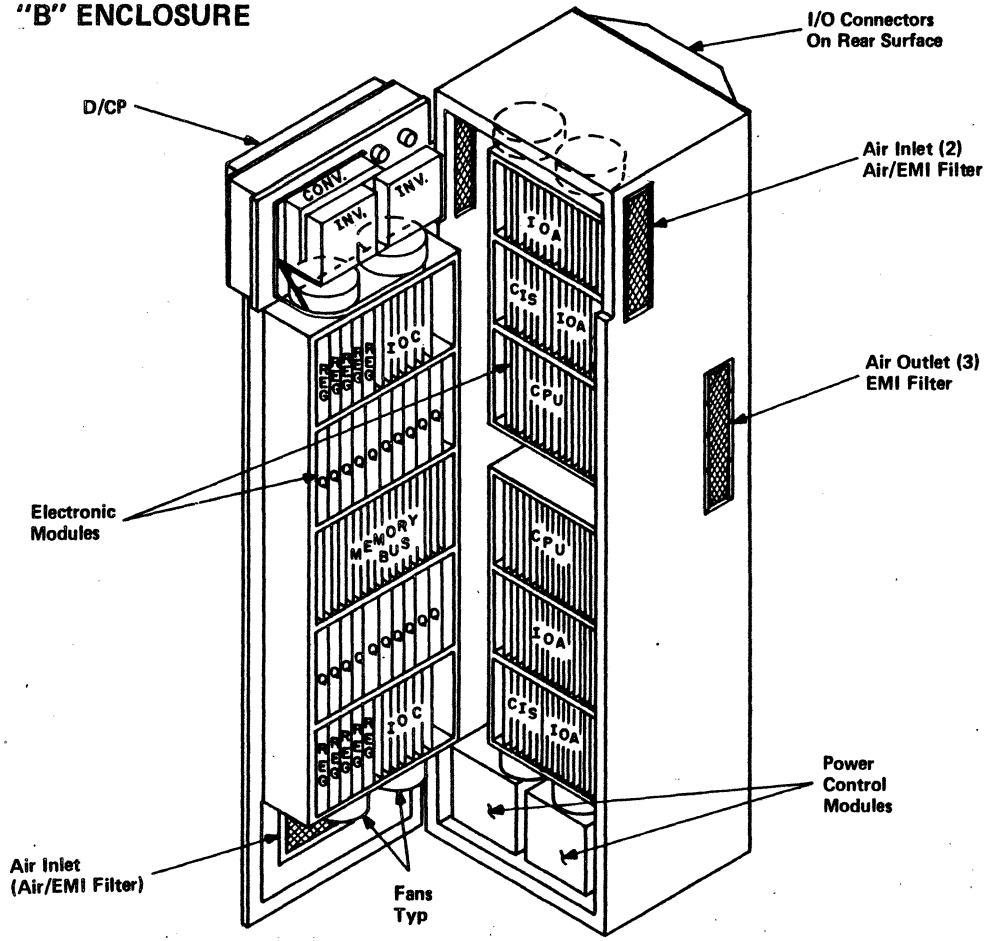
"A" ENCLOSURE



LRU SUMMARY

Logic LRU	70
Memory	10
Power Reg.	12
Fans	4
External Conn (Max)	69

"B" ENCLOSURE



LRU SUMMARY

Logic LRU	141
Memory	20
Power Reg.	21
Fans	10
External Conn (Max)	148

PROGRESS

- Mechanical Design Is Hardened
  - Unit design layouts with exception of ROCU are complete
  - Engineering drawings for the following have been/or are presently being released
    - LRU frames and assemblies
    - Backpanel MIBS, support plates and assemblies
    - Wiring harnesses
    - Power supply regulators and converters
    - D/CP drawing package released
    - A Enclosure – air structure and chassis released
    - B Enclosure – air structure and chassis released

TECHNICAL CONSIDERATIONS

- IBM Owego Standard MCS Technology Used In LRUs Provides Previously Qualified Hardware for AN/UYK-43
- Liquid Cooled Design Utilizes Pure Conduction to Cold Plate. No Fans Required In This Design. Enhances Reliability and Acoustic Requirement.
- Design Has Been Continually Monitored by Personnel from Relevant Support Functions, i.e., Environmental, Maintainability, EMI/EMC, Manufacturing Engineering, Safety, etc.
- Potential Risk Areas Listed Below Have Been Evaluated or Tested:
  - LRUs subjected to previously untested MIL-S-901 shock requirements
  - Display panel subjected to shock and vibe
  - Door latch mechanism – mockup
  - Large size mem/mem bus backpanel processed through standard production line to verify producibility with existing processes
  - Rough mockups of enclosures built to aid routing of wiring harnesses and analyze air flow characteristics
  - Simulated structure fabrication to verify weld technique.
  - Blowers tested to determine airborne and structureborne noise levels

DESIGN VERSUS P.D.

- Design Complies With P.D. To Greatest Extent Possible
- Configurability – Computer family members may be configurable at time of manufacture with a range of Functional modules as specified in P.D.
- Maintainability – All maintainability criteria except front removal of CPU and IOA backpanels has been achieved
- Environmental Requirements – All imposed environmental requirements have been considered with every effort made to meet or exceed those requirements
- Installation – Overall size, mounting criteria, and connector locations have been attained. Shock and vibration tolerant enclosure plus a thermally efficient conductive design drives unit weight over P.D. limits.

PHYSICAL INTERFACE

- Computer Can Be Configured at Time of Manufacture To Accept any Power Source Identified in the P.D.
- All Connectors, IOA Channel/Connector Reconfiguration, and Connector Locations are as Specified in the P.D. Visible Connector Reference Designations on the Enclosure Will Provide Ease of Installation.
- D/CPs Mounted Above the A Enclosure, in the B Enclosure and/or 30 Cable Feet Away from either Enclosure Will Provide the Man/Machine Interface
- A Bulkhead Mountable ROCU up to 150 Cable Feet from the Computer May Be Connected to either Family Member to Monitor and Control any Computer Configuration.
- The D/CP and ROCU Are Visible to and Operable by the Computer Operator when in the Normal Operating Condition Without Removal of Panels or Opening Doors

ARCHITECTURE OVERVIEW

ISA STATUS

- Preliminary ECP Submitted 4/14
- Awaiting Navy Feedback Before Formal Submittal
- ECP, Once Accepted, Will Be Merged with AN/UYK-7 ISA Spec to Become Formal AN/UYK-43 ISA Spec

SIGNIFICANT CLARIFICATIONS

COMPATIBILITY MODE

- ASR Bits 31, 30 modified only by explicit instruction
- Polarity of 31, 30 might be reconsidered
- Transitions between modes, except (43 exec, 43 task) and (43 exec, 7 task) should be done only in very restricted circumstances
- In AN/UYK-7 mode base registers are written as 18 bits with zero fill and read as 18 bits with zero fill

CIS INTERRUPT ROUTING

- IOC interrupts to an initiator are also sent to the CPU whose system ID is paired with the initiator's

NESTED MACHINE CHECKS

- Integrity critical errors which cannot be handled by software will cause the CPU to stop

ULTRA FORMAT

- Additional IOC format is required for opcodes 30-33 & 70

PREVIOUS AGREEMENTS

REGISTER STATE

- At most one bit may be set in present (ASR 19-16) or target (ASR 29-26)
- TBD response to an attempt to set more than one bit

CIS INTERRUPT CONTROL REGISTER

- Deleted

INSTRUCTION- LOAD INDEX & JUMP

- Deleted

AN/UYK-7 IDIOSYNCRACIES (INCLUDING ECP's)

- Irrational privileged instructions are not found in 43
- Floating point in 43 matches AN/UYK-7 ISA (PRE-ECP), also prenormalizes for MPY & DIV (ECP's 2, 5, 7)
- No shift count funny in 43 (ECP 1)
- No SPR 16, ASR 9 funny in 43 (ECP 4)
- No character/indirect funny in 43 (ECP 6)
- TBD whether critical ASR elements should be modifiable through manipulating DSW's

POTENTIAL ISSUES

OPCODE ASSIGNMENTS

BREAKPOINT

- Addresses (& readability)
- AN/UYK-7 compatibility
- Control register format

HYPERBOLICS

- Recommend deletion

STACK INSTRUCTIONS

- Recommend indirection be deleted
- Deserve to be revisited to improve flexibility

P-HISTORY

- Original definition, including interrupt bit
- Read not POP

IOC ADDRESSING

- Format II Y field should be same 18 - bit length as format 1

MAN MACHINE INTERFACE

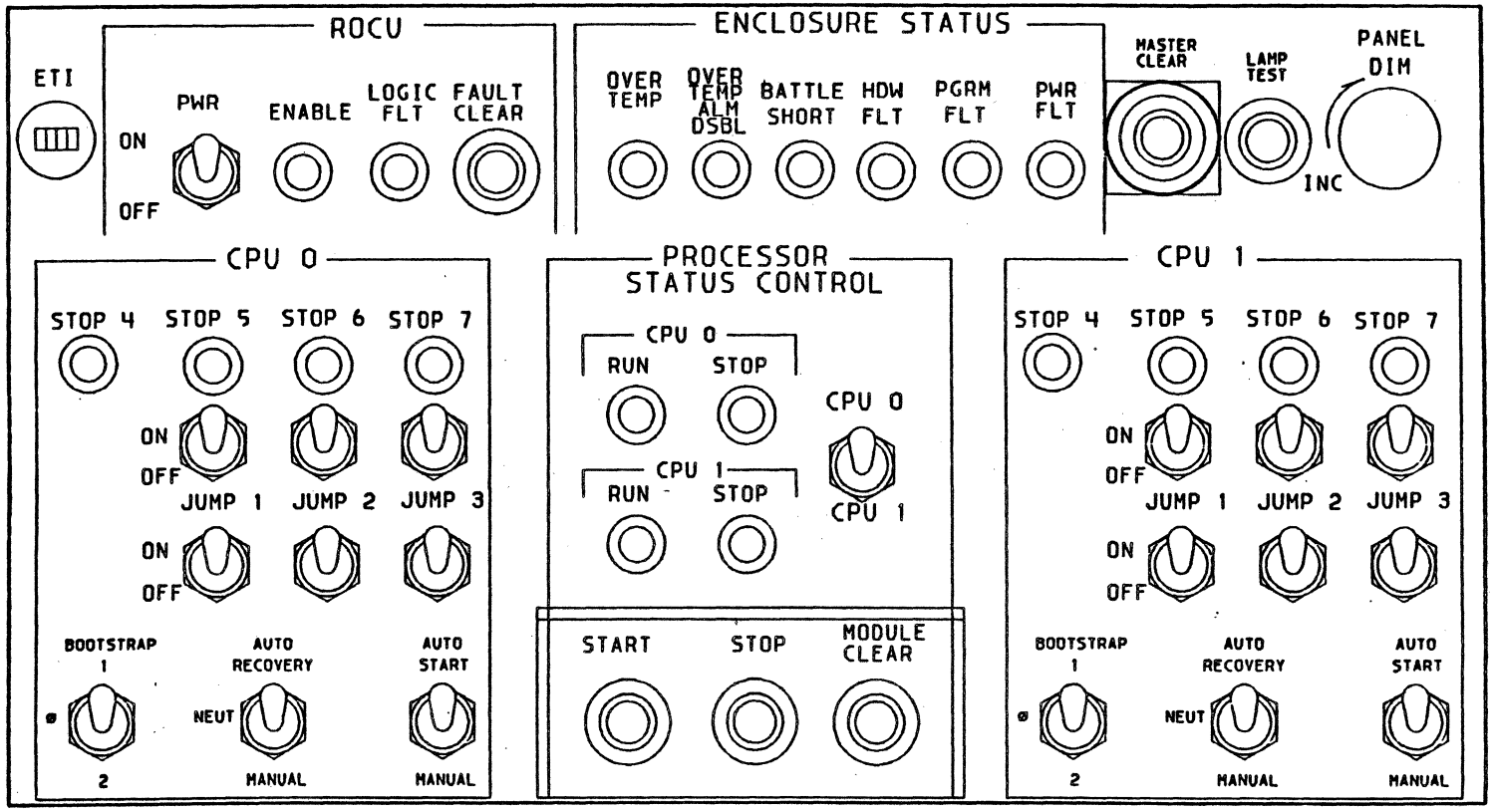
Agenda for PDR

- PDR ROCU
- PDR P/TP
- D/CP & Common Control Logic Status Update
- Respond to SDR Action Item List

REMOTE OPERATOR CONTROL UNIT

ROCU OVERVIEW

Requirements	IBM Design
• ROCU General Description	
– One ROCU as an Ordering Option	Met
– ROCU Must be Accessible to Operator	Met
– Monitors and Controls any Computer Configuration	Met
– Located up to 150 Cable Feet From Computer	Exceeded
– Powered by Computer	Met
• ROCU Functions	
– Implement at Least the Functions of UYK-7 ROCU	Met
– Can Select Which CPU to Control	Met
– Will not Affect Computer Until Enabled by D/CP	Met
• ROCU Performance	
– Continuous Display of: a) Power Status b) Operating Mode c) Fault Status d) Control Status	Met
• ROCU Maintainability	
– Repairable On-line	Met
– No Computer Resources Needed for Diagnosis	Met
– MTTR $\leqslant$ 0.25 Hours	Exceeded
– Maximum Repair Time $\leqslant$ 1 Hour at 95%	Exceeded


ROCU
ETI
PWR
ON
OFF
ENABLE
LOGIC FLT
FAULT CLEAR
ENCLOSURE STATUS
OVER TEMP
OVER TEMP ALM DSBL
BATTLE SHORT
HDW FLT
PGRM FLT
PWR FLT
MASTER CLEAR
LAMP TEST
PANEL DIM
INC
CPU 0
STOP 4
STOP 5
STOP 6
STOP 7
ON
OFF
JUMP 1
JUMP 2
JUMP 3
BOOTSTRAP 1
2
AUTO RECOVERY
NEUT
MANUAL
AUTO START
MANUAL
PROCESSOR STATUS CONTROL
CPU 0
RUN
STOP
CPU 1
RUN
STOP
CPU 0
CPU 1
START
STOP
MODULE CLEAR
CPU 1
STOP 4
STOP 5
STOP 6
STOP 7
ON
OFF
JUMP 1
JUMP 2
JUMP 3
BOOTSTRAP 1
2
AUTO RECOVERY
NEUT
MANUAL
AUTO START
MANUAL

IBM

5065-122

INDICATOR DESCRIPTION

- ROCU Enable Lamp – Indicates a D/CP has Enabled the ROCU
- Hardware Fault Lamp – Indicates an Enclosure Hardware Fault
- Program Fault Lamp – Indicates an Enclosure Program Fault
- Run Lamp – Indicates the Corresponding Processor is in its Run Mode
- Stop Lamp – Indicates the Corresponding Processor has Stopped
- Pwr Flt Lamp – Indicates a Power Fault has been Detected
- Over Temp Lamp – Indicates an Over-Temperature Condition has been Detected
- Battle Short Lamp – Indicates the Over-Temperature Protection Interlocks have been Bypassed
- Alarm Disable Lamp – Indicates the Audible Alarm has been Disabled
- ROCU Logic FLT Lamp – Indicates a Hardware Logic Fault has been Detected Within the ROCU
- Stop Lamps (8) – Indicate Corresponding CPU has Executed the Corresponding Stop Instruction and Stopped

SWITCH FUNCTION DESCRIPTION

- CPU0/CPU1 Switch – Selects Which Processor the ROCU Will Control
- Lamp Test Pushbutton – Lights all Lamps on the ROCU to Their Full Intensity
- ROCU Fault Clear Pushbutton – Clears the Panel Logic Fault Lamp and Re-initializes the ROCU
- Run Pushbutton – Causes the Selected Processor to be Sent a Start Command
- Stop Pushbutton – Causes a Halt Command to be Sent to the Selected Processor
- Master Clear Pushbutton – Causes the CCL to Issue Reset Commands to all Functional Modules
- Module Clear Pushbutton – Causes a Reset Command to be Sent to the Selected Processor
- Stop 5, 6, 7 Switches (Two Sets) – Causes Corresponding Stops to Occur Under Program Control in the Corresponding CPU
- Jump 1, 2, 3 Switches (Two Sets) – Causes Corresponding Jump to Occur in Corresponding CPU Under Program Control.
- Bootstrap 0, 1, 2 Switches (Two) – For Each CPU, Selects NDRO Entrance Address

SWITCH FUNCTION DESCRIPTION (Con't)

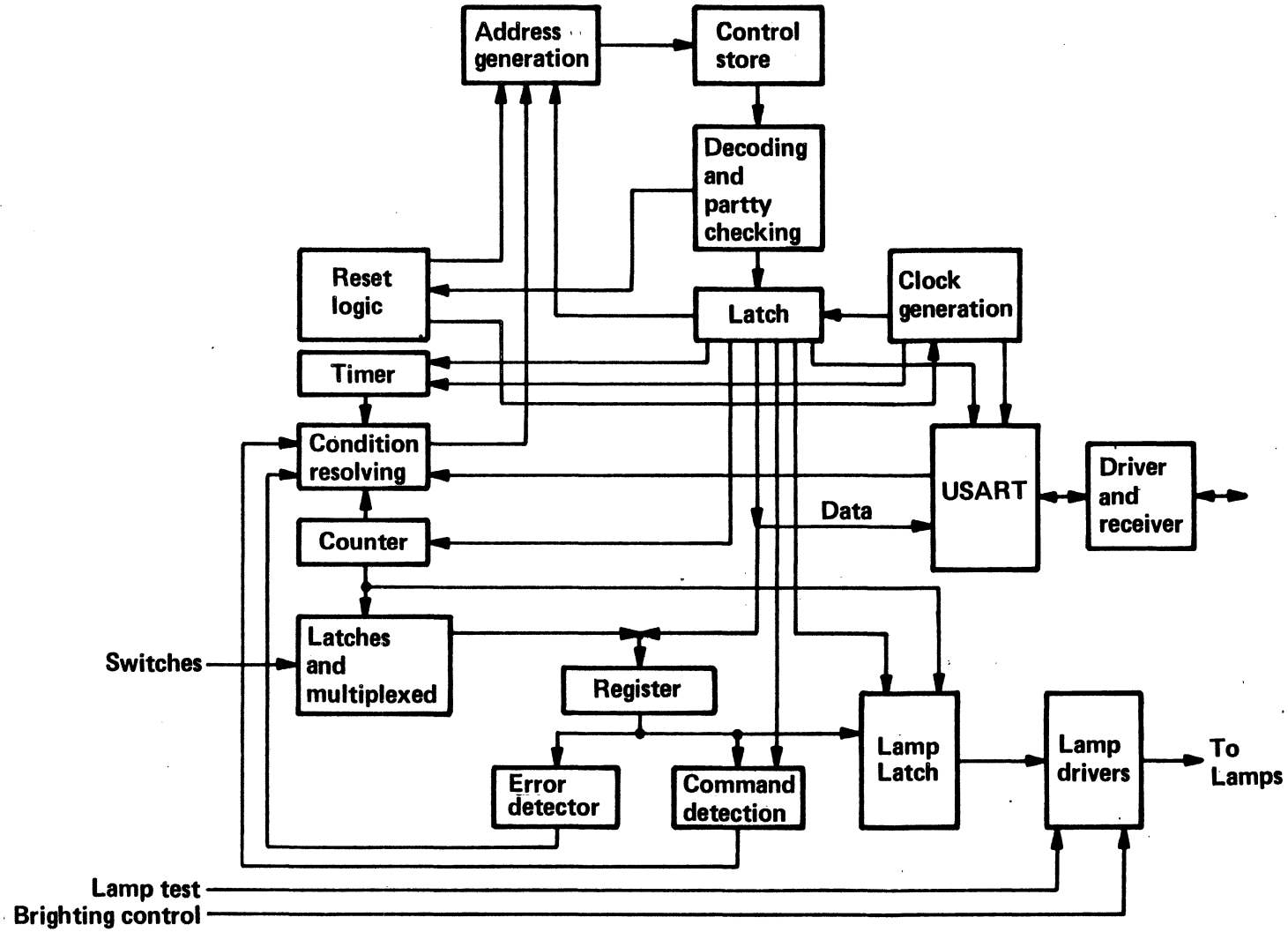
- Auto Recovery/Neutral/Manual Switches (Two) – For Each CPU: – Causes NDRO Automatic Entry or NDRO Access when Start is Depressed in Manual Mode or Class II Fault Interrupt Entrance when in Neutral Position
- Auto Start/Manual – Switches (Two) – For Each CPU: – Allows Automatic Start of Computer or in Manual Delays Start of Computer Until Start Pushbutton is Depressed
- Panel Dimming – Varies Intensity of Lighted Indicators

ROCU PACKAGING

- 9 Inch Page
- Total IC Components: 84
  - 67 LSTTL IC's
  - 5 High Power Lamp Drivers
  - 4 PROMS (32 x 8 Bits Each)
  - 2 Fairchild Fast IC's
  - 1 Universal Synchronous/Asynchronous Receiver Transmitter
  - 1 Oscillator I.C.
  - 1 Timer I.C.
- 32 Discrete Components
- 16 Decoupling Capacitors for +5 Volts
- 2 Decoupling Capacitors for -5 Volts

		Typical	Maximum
• Input Power	=	14.60 Watts	20.44 Watts
Logic	=	8.72 Watts	8.72 Watts
Lamps	=	1.80 Watts	6.00 Watts
Regulator	=	4.08 Watts	5.72 Watts

ROCU LOGIC


Address generation
Control store
Decoding and partty checking
Reset logic
Latch
Clock generation
Timer
Condition resolving
USART
Driver and receiver
Data
Counter
Latches and multiplexed
Switches
Register
Lamp Latch
Lamp drivers
To Lamps
Error detector
Command detection
Lamp test
Brighting control

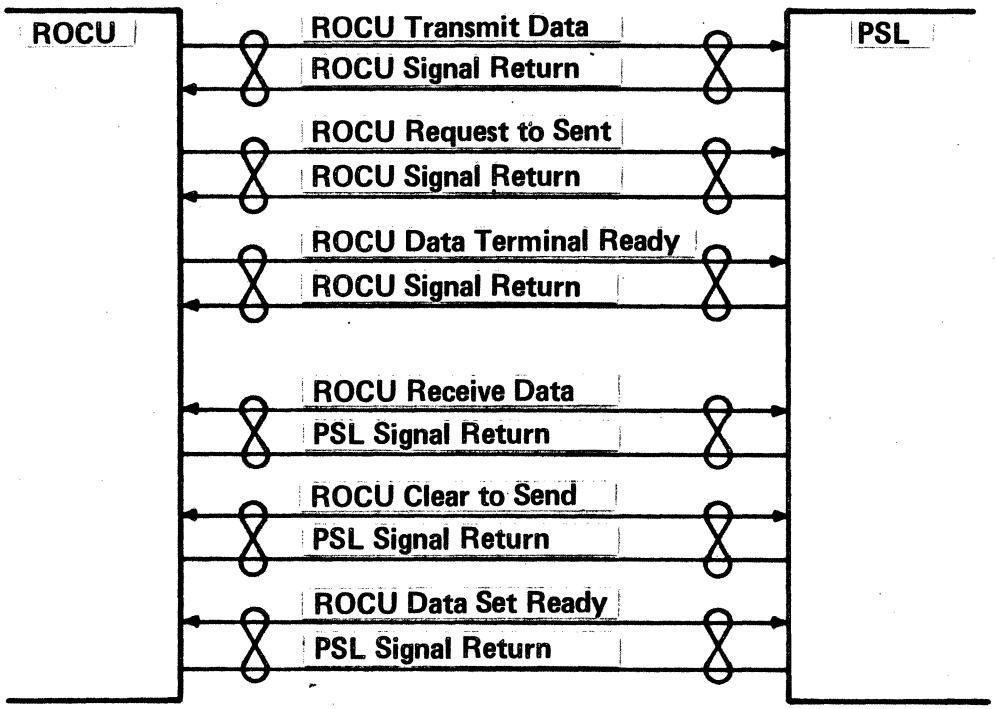
ROCU BUILT-IN-TEST

- Parity Check on Control Store
- Internal Data Wrap Test
- CCL Controlled Wrap Test
- Detected Error Indicated on Panel
- Operator Initiated Retry
- ROCU Operation is Stopped Following a Detected Error
- Parity, Framing and Overrun Errors Detected on RS449 Interface

ROCU-PSL INTERFACE

- EIA RS449
- Compatible with EIA RS232
- Unbalanced Voltage – EIA RS423
- Serial Data
- Data Rate 9600 BAUD
- Checking of Parity and Framing and Overrun Errors
- Capable of Driving up to 200 ft. of Cable
- Three Recognized Commands
  - Status Command – Start of Status Message
  - Switch Request – Request of Switch Data from ROCU
  - Wrap Test – Start of Data Wrap to ROCU
- Detected Errors Cause Remainder of Transmission to be Ignored

ROCU-PSL INTERFACE SIGNALS

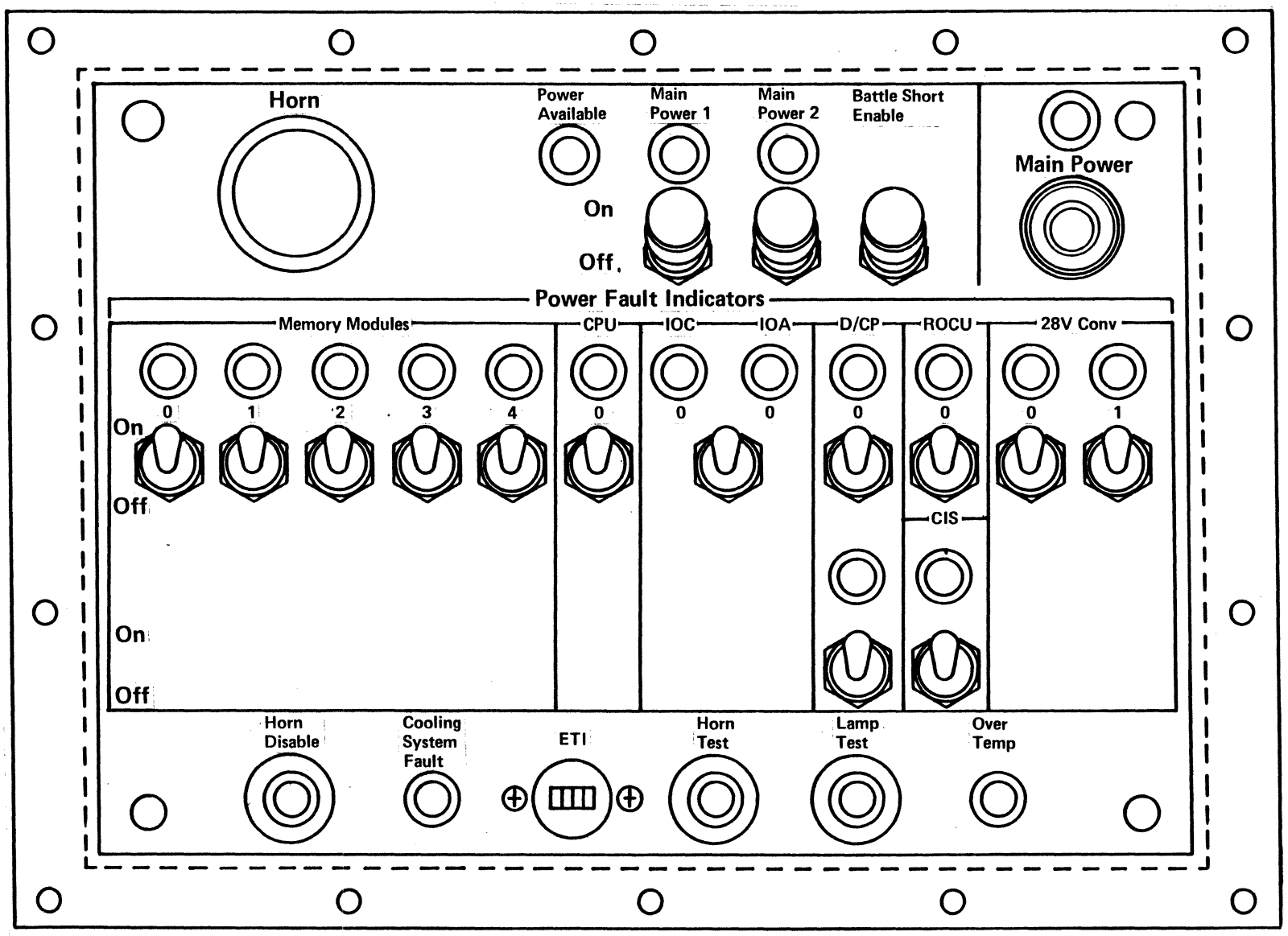


FUNCTIONAL COMPARISON

UYK-7 Functions	IBM UYK-43 ROCU Functions
Power Fault Indicator	Provided
Program Fault Indicator	Provided
Hardware Fault Indicator	Provided
Program Stops Indicators	Provided
Processor Running Indicator	Provided
Unit On Line Indicator	Provided
Indicator Test	Provided
Program Stops Controls	Provided
Program Jump Controls	Provided
Unit On Line Control	Provided
Bootstrap 1, 0, 2 Control	Provided
Auto Recovery/Manual Control	Provided
Stop Control	Provided
Start Control	Provided
Master Clear Control	Provided
Over Temp Indicator	Provided
Power On Indicator	Provided
	Battle Short Activated Indicator
	Panel Logic Fault Indicator
	Overtemp Alarm Disabled Indicator
	Panel Dim Control
	CPU Select Control
	Auto Start/Manual Control
	Module Clear Control
	ROCU Error Clear Control

PTP OVERVIEW

P/TP Requirements	IBM Design
• P/TP General Description	
– Implements all Power and Temperature Functions of the AN/UYK-7 Operator Panel	Met
• P/TP Functions	
– Continuous Display of:	
- Power Status	Met
- Temperature Status	Met
– Battle Short Switch	Met
– Audible Alarm	Met
– Audible Alarm Disable	Met


Horn
Power Available
Main Power 1
Main Power 2
Battle Short Enable
On
Off
Main Power
Power Fault Indicators
Memory Modules
CPU
IOC
IOA
D/CP
ROCU
28V Conv
0
1
2
3
4
0
0
0
0
0
0
1
On
Off
CIS
On
Off
Horn Disable
Cooling System Fault
ETI
Horn Test
Lamp Test
Over Temp

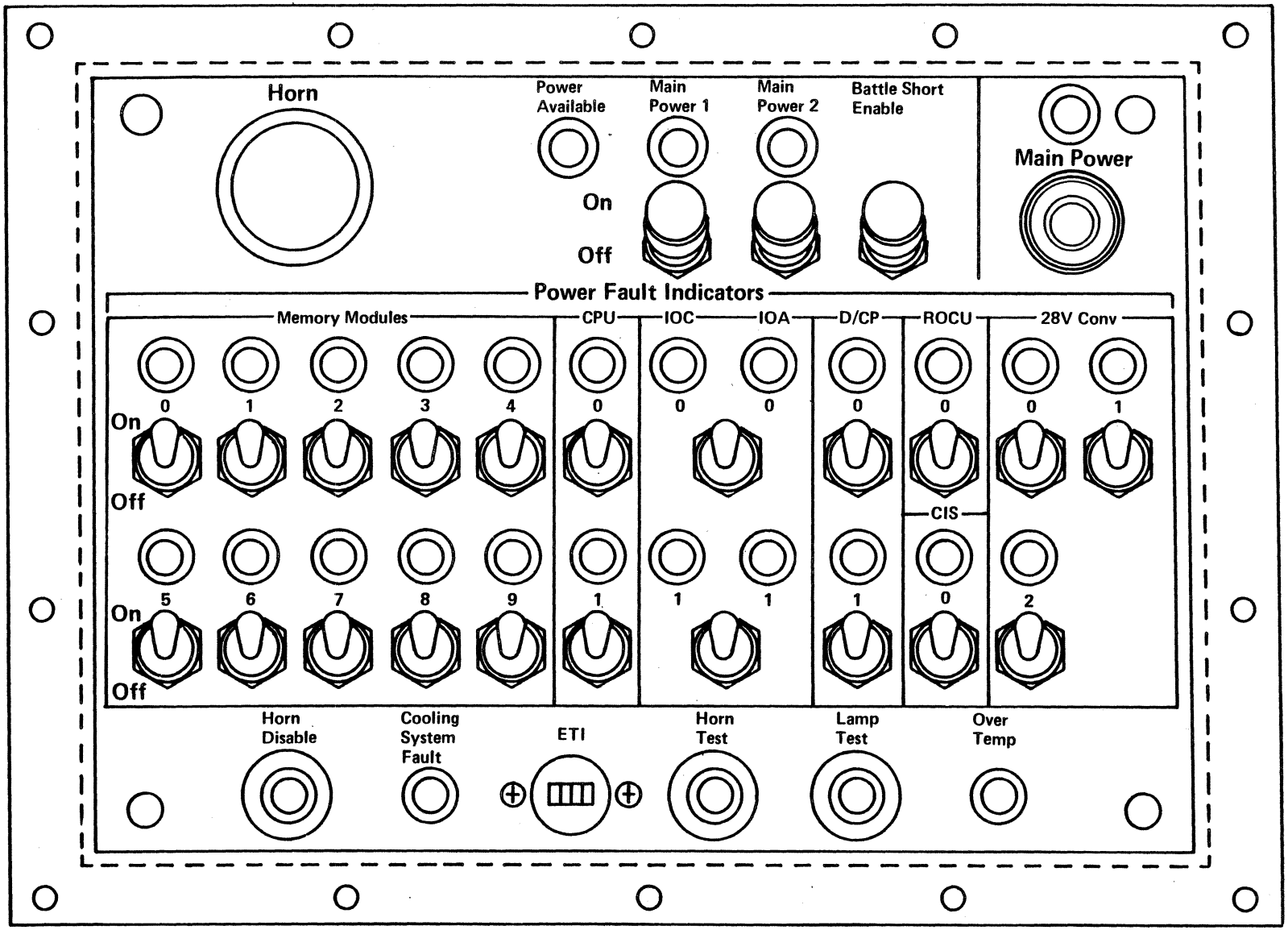

Horn
Power Available
Main Power 1
Main Power 2
Battle Short Enable
On
Off
Main Power
Power Fault Indicators
Memory Modules
CPU
IOC
IOA
D/CP
ROCU
28V Conv
0
1
2
3
4
0
0
0
0
0
0
1
On
Off
CIS
5
6
7
8
9
1
1
1
1
0
2
On
Off
Horn Disable
Cooling System Fault
ETI
Horn Test
Lamp Test
Over Temp

TABLE I. P/TP PANEL DEFINITION

- Power Available Indicator – At the time the circuit breakers are activated this indicator lights. It is a green light indicating a go ahead condition.
- Main Power Push Button and Indicator – After the circuit breakers have been activated the main power PB can then be activated. In so doing, the main power indicator will become lighted. It is a white light providing a functional indication.
- D.C. Power Switch(es) and Indicator(s) – This switch(es) is a lever-locked toggle which under normal operating conditions is used by the operator to energize the coil of the contractor which supplies power to the input power conditioners. The indicator(s) is white providing a functional indication.
- Power Module Switches and Fault Indicators – These switches are always kept in their active position up or on. Their purpose is to inhibit the output power only. They do not remove the input power. This is done inside the cabinet prior to removal. The indicator only indicates if there is a serious fault. The indicator is red for power fault or malfunction.
- 28V Converter Switches and Fault Indicators – These switches and indicators operate the same as do the power module switches and indicators.

TABLE I (Continued)

- Horn Disable Switch and Overtemp Indicator – The horn disable switch is used to disable the audible alarm. In conjunction with the horn is an overtemp indicator. When first stage overtemperature occurs, the indicator flashes until the operator disables the horn. The indicator then glows continuously while overtemp persists. At second stage of overtemperature, the indicator glows continuously even after automatic power shut down. The overtemp indicator is red indicating a malfunction or failure condition.

- Battle Short Switch – This switch is a lever-locked toggle that, when enabled, overrides the second stage overtemp power drop out sensors, the D.C. power switches, the interlocks, and turns on the interlock override indicator.

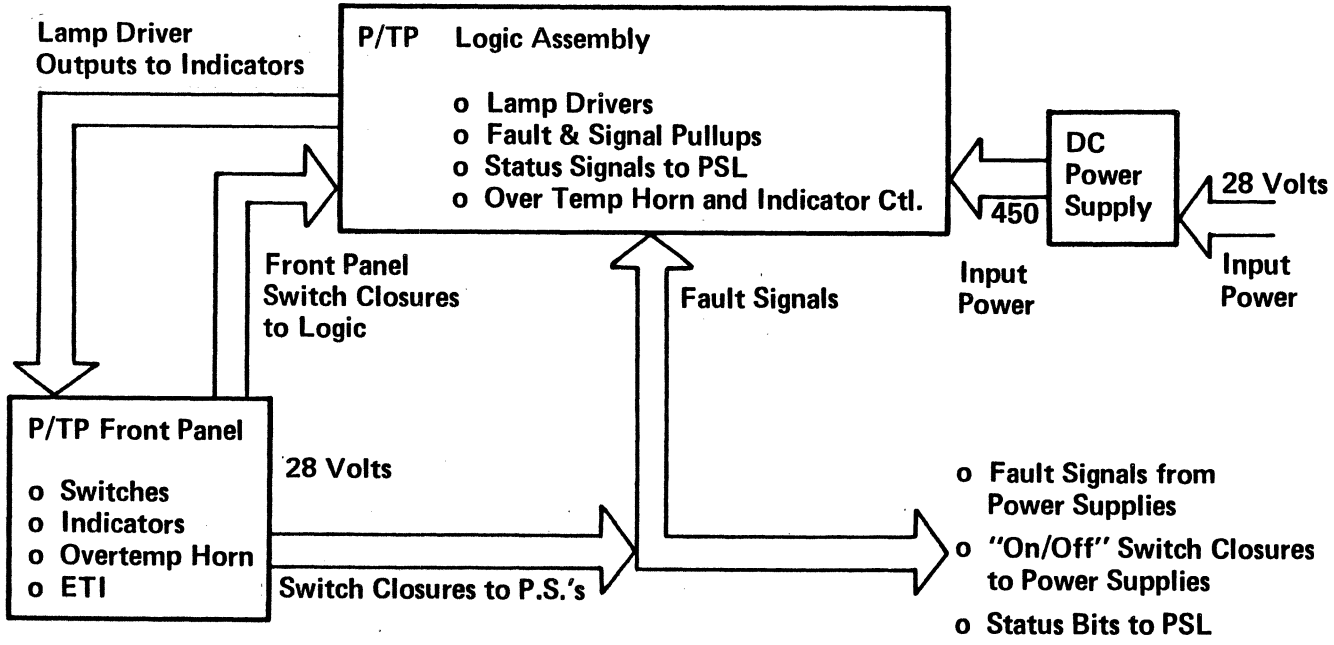
- Horn Test Push Button – Used to check the presence of the horn.

- Lamp Test Push Button – Used to check indicator lamps.

- Cooling System Fault Indicator – Used to report a fault in the cooling system. This is a red indicator indicating a failure condition.

- ETI – Counts enclosure power-on time.

P/TP BLOCK DIAGRAM



IBM

5065-127

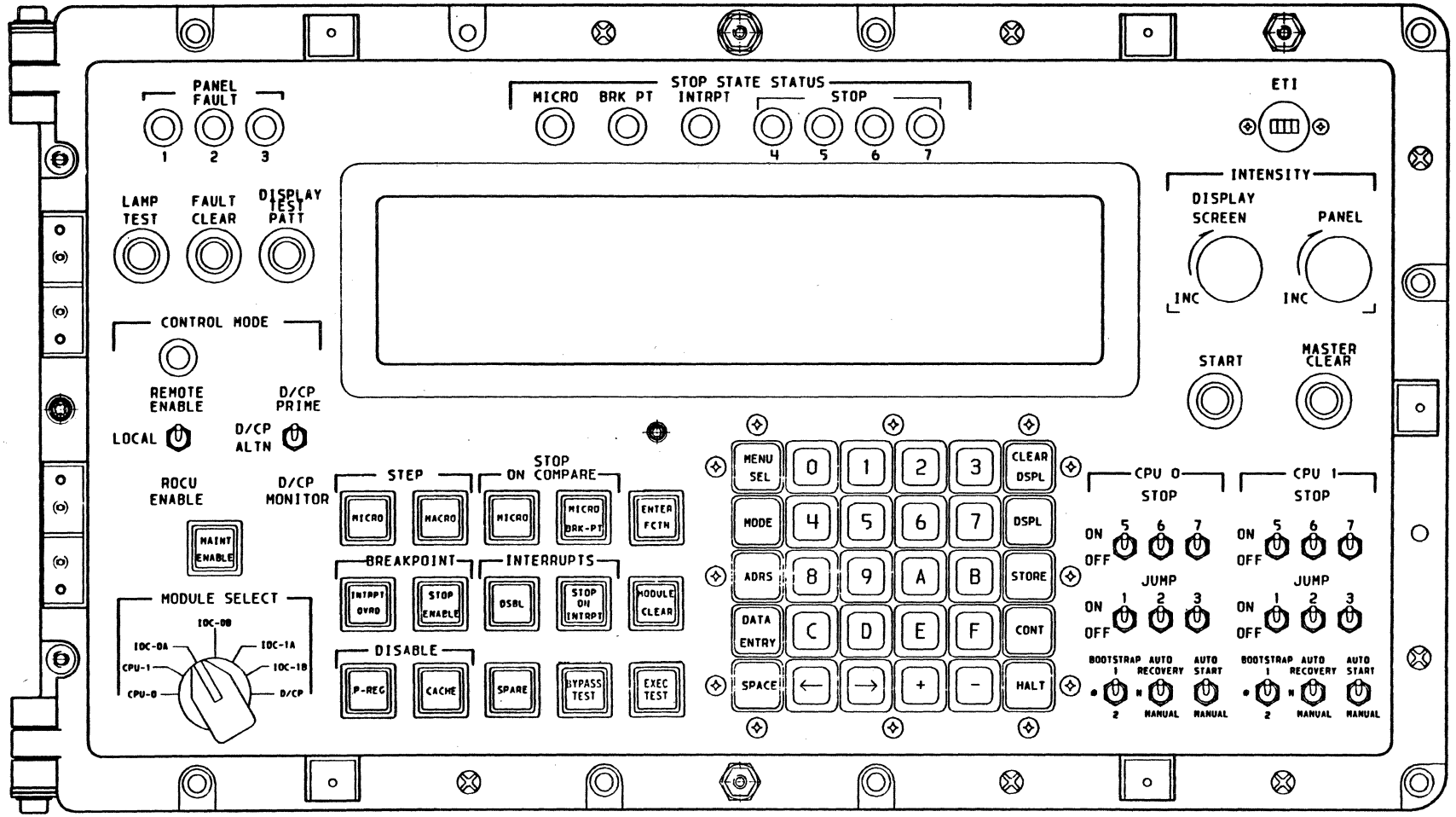
POWER/TEMPERATURE PANEL (P/TP) HARDWARE/POWER CHARACTERISTICS

"A" PANEL			"B" PANEL		
*Common P. C. Board Qty – 1 (2.76" x 8.12")			*Common P. C. Board Qty. – 1 (2.76" x 8.12")		
• 30 Flatpacks • 1 Dip Timer • 26 Idling Resistors • 1 to 5 5V Relay			• 30 Flatpacks • 1 Dip Timer • 26 Idling Resistors • 1 to 5 5V Relay		
Power			Power		
P. C. Board Logic @ 5V		5.48W	P. C. Board Logic @ 5V		5.48W
17 Lamps @ 5V (Lamp Test)		9.90W	26 Lamps @ 5V (Lamp Test)		15.50W
		15.38W			20.98W
2 Lamps @ 28V	2.24W		3 Lamps @ 28V	3.36W	
1 Horn @ 28V	1.68W		1 Horn @ 28V	1.68W	
	3.92W	3.92W		5.04W	5.04W
	Total	19.30W		Total	26.02W

*Note: P. C. Board Assembly is same for both A and B Panels.

D/CP CHANGES SINCE PDR

- Addition of Jump-Stop Toggles as Discretes on D/CP
- IPL Function Pushbutton Deleted
- Enter Function Pushbutton Changed to Lighted Pushbutton Position
- Two New Functions Added to Run Control/Disable Pushbutton Field to Support Enclosure Fault Isolation Procedures:
  - Bypass Test
  - Execute Test
- Switch Protection Provisions Added for "Start" "Masterclear" Pushbuttons and all "Operational Toggles"


PANEL FAULT
1
2
3
STOP STATE STATUS
MICRO
BRK PT
INTRPT
STOP
4
5
6
7
ETI
LAMP TEST
FAULT CLEAR
DISPLAY TEST PATT
INTENSITY
DISPLAY SCREEN
PANEL
INC
INC
CONTROL MODE
REMOTE ENABLE
D/CP PRIME
LOCAL
D/CP ALTN
START
MASTER CLEAR
ROCU ENABLE
D/CP MONITOR
MAINT ENABLE
STEP
MICRO
MACRO
STOP ON COMPARE
MICRO
MICRO BRK-PT
ENTER FCTN
BREAKPOINT
INTRPT QUAD
STOP ENABLE
INTERRUPTS
DSBL
STOP ON INTRPT
MODULE CLEAR
DISABLE
P-REG
CACHE
SPARE
BYPASS TEST
EXEC TEST
MENU SEL
0
1
2
3
CLEAR DSPL
MODE
4
5
6
7
DSPL
ADRS
8
9
A
B
STORE
DATA ENTRY
C
D
E
F
CONT
SPACE
←
→
+
−
HALT
MODULE SELECT
IOC-0B
IOC-0A
IOC-1A
CPU-1
IOC-1B
CPU-0
D/CP
CPU 0
STOP
ON
OFF
5
6
7
JUMP
1
2
3
BOOTSTRAP
AUTO RECOVERY
AUTO START
1
2
MANUAL
MANUAL
CPU 1
STOP
JUMP
BOOTSTRAP
AUTO RECOVERY
AUTO START

OVERVIEW

SIMPLIFIED MAINTENANCE APPROACH

- Based on SDR Discussions IBM has Configured a Simplified Maintenance Procedure
  - Two Functions Added to D/CP Panel
    - Execute Test Pushbutton
    - Bypass Test Pushbutton
- Enclosure Self Test Callup Available at any Time
- Procedure is Interactive
- Expanded Capability Using Mode 600 Function is Still Retained

Execute Test ——— Depressing this Pushbutton Causes 1 of the Following to Occur

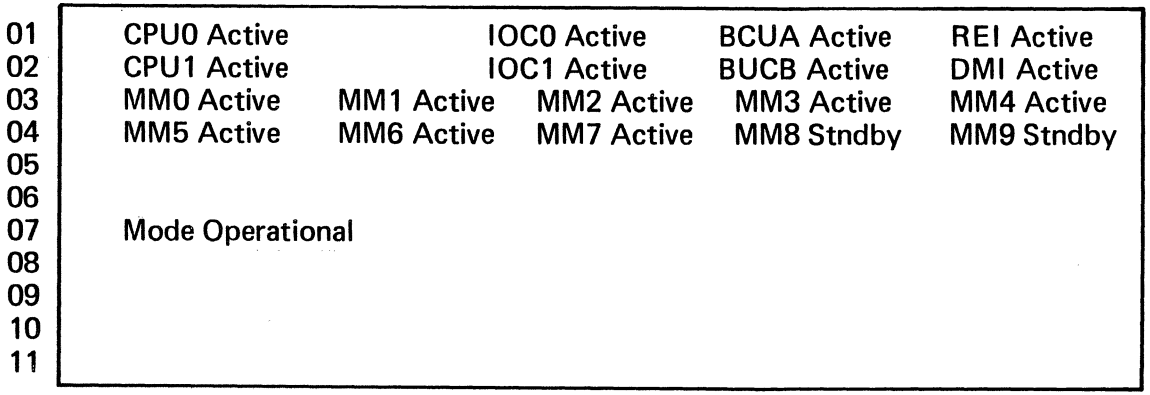
- Directs FTRM to Execute the Fault Isolation Routine Associated with the Identified Failure.
- Will Prompt Operator for an Additional Response if no Failure Currently Exist

Bypass Test ——— Depressing this Pushbutton the Following to Occur

- Causes FTRM to Abort the Test Procedure that is in Process and Places the Related Failed FM at the Bottom of the Failed FM List and Displays the Next Failed Module IF Another Exist

TYPICAL D/CP DISPLAY

- Shows Resource Status
  - Fully operational "B" enclosure
  - No failures



MAINTENANCE PROCEDURE FOR LOGIC FAULT

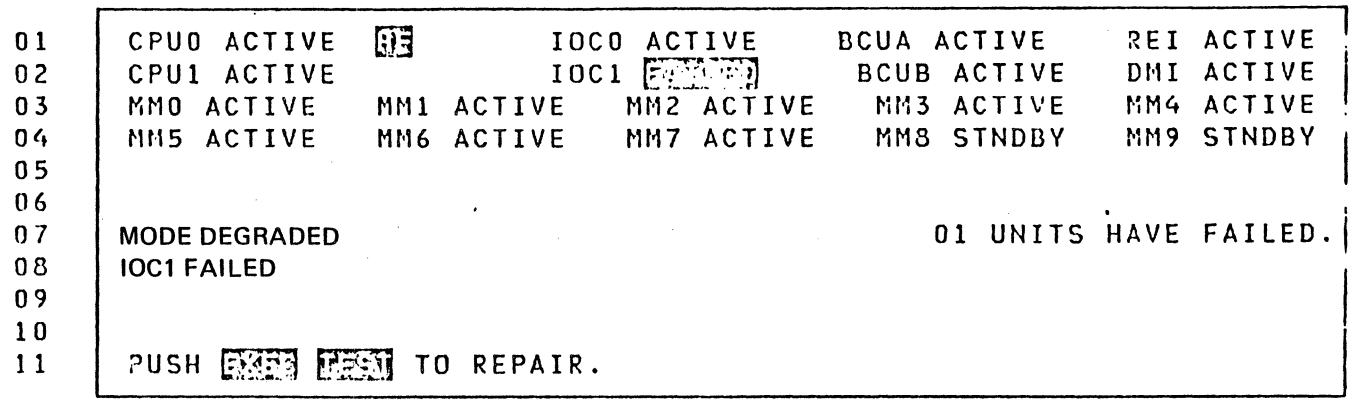
- D/CP Status Indicates FHM Failed
- Depress EXEC TEST on D/CP
- Observe D/CP Display – LRU Callouts
- Power Down FHM – Toggle Switch on P/TP
- Remove Indicated LRU
- Replace with Spare LRU
- Power Up FHM –
- Depress EXEC TEST

AUTOMATED MAINTENANCE PROCEDURE

- D/CP Display When Fault Has Occurred
  - — System has been automatically reconfigured
- Shows Resource Status

A. Example

- — "B" enclosure operational, reduced capability
- — IOC1 failed



AUTOMATED MAINTENANCE PROCEDURE (Continued)

B. The operator depresses the EXEC TEST pushbutton which causes the D/CP to indicate on the display that fault is being diagnosed.

```
      0         1         2         3         4         5         6
      12345678901234567890123456789012345678901234567890123456789012345678901234
   01 CPU0 ACTIVE  HE        IOC0 ACTIVE    BCUA ACTIVE    REI ACTIVE
   02 CPU1 ACTIVE            IOC1 FAILED     BCUB ACTIVE    DMI ACTIVE
   03 MM0 ACTIVE   MM1 ACTIVE   MM2 ACTIVE    MM3 ACTIVE    MM4 ACTIVE
   04 MM5 ACTIVE   MM6 ACTIVE   MM7 ACTIVE    MM8 STNDBY    MM9 STNDBY
   05
   06
   07 MODE DEGRADED                                  01 UNITS HAVE FAILED.
   08
   09                      DIAGNOSING
   10
   11
```

IOC1 Failure Being Diagnosed

AUTOMATED MAINTENANCE PROCEDURE (Continued)

B1. FIRM executes the IOC diagnostics resulting in the fault callout display.

```
      0         1         2         3         4         5         6
      12345678901234567890123456789012345678901234567890123456789012345678901234
   01 CPU0 ACTIVE  HE        IOC0 ACTIVE    BCUA ACTIVE    REI ACTIVE
   02 CPU1 ACTIVE            IOC1 FAILED     BCUB ACTIVE    DMI ACTIVE
   03 MM0 ACTIVE   MM1 ACTIVE   MM2 ACTIVE    MM3 ACTIVE    MM4 ACTIVE
   04 MM5 ACTIVE   MM6 ACTIVE   MM7 ACTIVE    MM8 STNDBY    MM9 STNDBY
   05
   06
   07 MODE DEGRADED                                  01 UNITS HAVE FAILED.
   08 IOC1 FAILED          REPLACE LRUS IN ORDER XXXXXX, XXXXXX, XXXXXX.
   09
   10
   11 PUSH EXEC TEST TO RETEST.
```

Results of Diagnostic Test

AUTOMATED MAINTENANCE PROCEDURE (Continued)

C. The Operator Drops Power on IOC1
(places IOC1 toggle switch on P/TP in "OFF" position)

- Removes 1st LRU on List and Installs Spare LRu
- Restores Power to IOC1 (IOC1 toggle on P/TP to "ON")
- Depresses EXEC TEST Pushbutton on D/CP – FTRM Retests IOC1

```
01  CPU0 ACTIVE  BE        IOC0 ACTIVE    BCUA ACTIVE    REI ACTIVE
02  CPU1 ACTIVE            IOC1 Failed    BCUB ACTIVE    DMI ACTIVE
03  MM0 ACTIVE   MM1 ACTIVE   MM2 ACTIVE   MM3 ACTIVE   MM4 ACTIVE
04  MM5 ACTIVE   MM6 ACTIVE   MM7 ACTIVE   MM8 STNDBY   MM9 STNDBY
05
06
07  BEING DIAGNOSED                                01 UNITS HAVE FAILED.
08
09                       DIAGNOSING
10
11
```

IOC1 Failure Being Diagnosed

AUTOMATED MAINTENANCE PROCEDURE (Continued)

D. System Automatically Reconfigured Since Fault Was Cleared

```
          0         1         2         3         4         5         6
          12345678901234567890123456789012345678901234567890123456789012345678901234
01  CPU0 ACTIVE            IOC0 ACTIVE    BCUA ACTIVE    REI ACTIVE
02  CPU1 ACTIVE            IOC1 ACTIVE    BCUB ACTIVE    DMI ACTIVE
03  MM0 ACTIVE   MM1 ACTIVE   MM2 ACTIVE   MM3 ACTIVE   MM4 ACTIVE
04  MM5 ACTIVE   MM6 ACTIVE   MM7 ACTIVE   MM8          MM9
05
06
07  MODE OPERATIONAL.
08
09
10
11
```

Fully Operational System Display

SDR ACTION ITEM REVIEW FOR MAN MACHINE INTERFACE

ITEM	RESPONSE
8. Bulkhead mounting of D/CP	IBM will supply mounting fixture to accomplish this.
9. Review possible commonality with UYK-44 keyboard.	Not feasible for following reasons: • Does Not Contain Suitable Character Display Capability to Support PD Requirements or Intent nor IBM's technical response. • Would Require Many Additional Operator Actions. • Would Not Meet the Three-Fold Functions Proposed and Designed into the UYK-43 Display/Control Panel.

SDR ACTION ITEM REVIEW FOR MAN-MACHINE INTERFACE – Continued

ITEM	RESPONSE
11. Review implementation of jump/stop switches relative to IPL & Power On Recovery	The design of the D/CP was modified to provide for 3 jump switches and for 3 jump switches for each CPU. This approach fits the IPL/ Recovery technique required in the UYK-7 code transported to the UYK-43.
12. Provide further information on D/CP in following areas: • Main Storage Modification • Disable Interrupts • Labeling (Abbreviations) • I/O Channel Activity	Main Storage Modification – Will provide on-the-fly main storage modifications to be made from the D/CP. Disable Interrupts – Provided as a program debug aid. When enabled, the following CPU external interrupts are not recognized: • IOC 0 Class I & Class III • IOC 1 Class I & Class III • CIS Class I & Class III • BCU A & BCU B

SDR ACTION ITEM REVIEW FOR MAN-MACHINE INTERFACE – Continued

ITEM	RESPONSE
12. Continued	Labeling (Abbreviations) on Plasma Panel – By using the abbreviations in MIL-STD 783B & 12C Line 6 of the plasma panel can accommodate the information to be displayed.

Battle Short Enable	=	BATSHORTENBL	12		
Alarm Disable	=	ALMDSBL	7		
Overtemperature	=	OVERTEMP	8		
Remote Enable	=	REMOTEENBL	10	Mutually	53
ROCU Enable	=	ROCUENBL	8	Exclusive	Characters
Fan Fault	=	FANFAULT	8		
Power Fault	=	PWRFAULT	8		

I/O Channel Activity – Bit information defining channel activity is spread throughout BCW array. IBM has studied a number of ways to gather this information all of which impact the IOC & CCL software.

SOFTWARE DEVELOPMENT OVERVIEW

SOFTWARE DEVELOPMENT OVERVIEW

AGENDA REVIEW

AN/UYK-43 SOFTWARE SUMMARY SCHEDULE

Program	Resp.	Requirements	HL Design	Detail Design	Code	Module Test	Subprgm Test
CPU Emul. Microprogram	M35	03/27/81 04/10/81C	06/01/81	07/31/81	07/31/81	02/26/82	02/26/82
IOC Emul. Microprogram	560	03/27/81 04/10/81C	05/01/81 05/15/81	05/29/81 06/19/81	05/29/81 06/19/81	02/26/82	02/26/82
Microcode Assm. (Int)	M44	11/21/80 01/08/81C	12/05/80C	12/26/80C	12/26/80 01/23/81C	12/26/80 01/30/81C	01/30/81C
(Fin)		06/19/81	06/26/81	07/03/81	07/10/81	07/31/81	07/31/81
Microcode Lked. (Int)	M44	11/21/80 01/08/81C	12/05/80 01/12/80C	12/05/80 01/16/81C	12/05/80 03/27/81C	12/05/80 04/13/81C	04/13/81C
(Fin)		07/03/81	07/10/81	07/17/81	07/24/81	07/31/81	07/31/81
Microcode Sim. (Int)	M44	12/26/80 03/20/81C	01/30/81 03/27/81C	02/13/81 03/27/81C	01/30/81 04/10/81C	04/03/81 05/01/81	05/01/81
(Fin)		06/26/81	07/10/81	07/24/81	08/07/81	08/28/81	08/28/81
BGP	M44	05/01/81 06/15/81	07/10/81 10/09/81	07/17/81 10/16/81	09/25/81 12/18/81	12/11/81 03/26/82	TBD
CPU Diagnostics	M66	03/01/81 04/10/81C	01/30/81 02/13/81C	02/28/81 03/15/81C	04/30/81 08/01/81	05/15/81 08/22/81	06/30/81 10/31/81
Unit/Sys Diagnostics	M97	03/01/80C	06/15/81 02/26/81C	07/30/81 01/15/82	09/15/81 03/01/82	10/15/81 03/01/82	11/30/81 04/15/82
D/CP Software	515	12/01/80 02/27/81C	01/16/81 04/08/81C	02/27/81 05/12/81	04/24/81 05/25/81	05/15/81 06/05/81	06/12/81 07/03/81

AN/UYK-43 SOFTWARE SUMMARY SCHEDULE — Continued

Program	Resp.	Require-ments	HL Design	Detail Design	Code	Module Test	Subprgm Test
Tools (Sim Supp RTNS)	M44	01/23/81 03/20/81C	03/20/81 04/03/81C	04/03/81 04/10/81C	05/01/81	06/26/81 04/30/81	N/A
SDEX SFW Mods	M97	03/01/81C	07/10/81	10/01/81	01/01/82	01/31/82	03/31/82
FTRM	M97	03/01/81 04/10/81C	05/01/81	10/01/81	03/01/82	03/01/82	05/31/82 04/01/82
OTP (M66)	M66	03/01/81 04/10/81C	05/01/81 05/15/81	12/30/81	01/30/82	02/12/82	03/30/82 04/01/82
OTP (M97)	M97	03/01/81 04/10/81C	05/01/81	10/01/81	01/01/82	01/01/82 01/02/82	05/01/82 11/01/81
EVP (M66)	M66	01/31/81 02/13/81C	05/01/81 05/15/81	05/10/81 08/14/81	06/15/81 08/21/81	07/30/81 08/28/81	10/31/81
EVP (M97)	M97	01/01/81 02/13/81C	05/01/81	05/15/81	07/01/81	07/01/81 09/01/81	09/01/81 11/01/81
NDRO	M97	03/01/81C	05/01/81	11/01/81	12/01/81	12/01/81	01/02/82
S/W Development Lab	L68	12/15/80C	01/16/81C	04/17/81C	04/24/81	05/01/81 05/09/81	05/01/81 05/09/81

CPU DIAGNOSTICS SCHEDULE SUMMARY

Function	RESP	Requirements Document (1)	HL Design	Detail Design	Code	Module Test	Subpgm Test
System (1)	DB	N/A	N/A	N/A	N/A	N/A	N/A
E-Unit	PB KK	07/01/80C	12/19/80C	01/30/81 02/20/81C	03/15/81 05/08/81	01/30/81 06/5/81	10/31/81
I-Unit	TW	07/01/80C	12/05/80C	12/15/80 02/27/81C	01/15/81 05/15/81	06/01/81 06/19/81	10/31/81
Sequence	JG	07/01/80C	12/12/80C	01/15/81 03/13/81C	02/15/81 05/11/81	06/30/81 06/26/81	10/31/81
SC-Unit	FN	07/01/80C	11/28/80C	12/30/80 03/15/81C	02/15/81 06/06/81	06/30/81 06/27/81	10/31/81
Perform. Mon.	WS	07/01/80C	01/13/81C	03/02/81C	04/30/81 07/18/81	05/10/81 08/01/81	10/31/81
Pgm. Debug. Aids	FN	07/01/80C	01/30/81 02/06/81C	02/28/81 03/13/81C	03/30/81 08/01/81	05/15/81 08/22/81	10/31/81
NDRO Memory	WS	07/01/80C	02/06/81C	02/28/81 03/02/81C	03/30/81 05/22/81	04/30/81 06/06/81	10/31/81
Multiplier	DG	N/A	02/13/81C	03/06/81 03/13/81C	05/30/81 05/01/81	05/15/81 05/22/81	10/31/81

(1) LOE in support of all other units

UNIT/SYSTEM DIAGNOSTICS SCHEDULE SUMMARY

Function	RESP	Requirements Document (1)	HL Design	Detail Design	Code	Module Test	Subpgm Test
System (1)	JK	N/A	N/A	N/A	N/A	N/A	N/A
Memory	JK	3/01/80C	11/15/80 02/05/81C	12/30/80 03/05/81	06/15/81 10/01/81	07/15/81 11/01/81	08/15/81 03/01/82
IOC	JK	03/01/80C	02/15/81 01/15/81C	05/15/81 02/01/81C	05/15/81 06/01/81	05/30/81 06/15/81	06/30/81 03/01/82
IOA	JK	03/01/80C	12/30/80 02/15/81C	02/28/81 03/27/81	04/30/81 07/15/81	06/15/81 09/01/81	07/30/81 03/01/82
CIS	JK	03/01/80C	02/28/81 02/26/81C	03/30/81 07/15/81	08/15/81 12/01/81	09/10/81 02/08/82	09/30/81 03/01/82
Intra-Unit	JK	03/01/80C	06/15/81 02/26/81C	07/30/81 01/15/82	09/15/81 03/01/82	10/15/81 03/01/82	10/30/81 04/15/82
SASD Supervisor	JK	03/01/80C	01/30/81 02/26/81C	02/28/81 10/15/81	04/15/81 12/01/81	05/15/81 01/01/82	05/30/81 03/01/82

(1) LOE in support of all other units.

D/CP SOFTWARE SCHEDULE SUMMARY

Unit	RESP	Requirements Document	HL Design	Detail Design	Code	Module Test	Subpgm Test
D/CP S/W Subsystem	515	11/03/80C					
Release 1 Diagnostic			01/08/81C	01/15/81C	01/17/81 03/06/81C	03/23/81 04/06/80C	04/17/81 05/08/81
Release 2			01/08/81 02/12/81C	02/13/81 03/18/81C	03/30/81C	04/17/81 05/01/81	05/08/81 05/29/81
Release 3			01/08/81 02/12/81C	02/13/81 04/03/81C	04/10/81 04/24/81	05/08/81 05/25/81	06/12/81 06/19/81
PSL Software Subsystem	515	12/01/80 02/27/81C					
Release 1 Diagnostic			01/15/81C	02/10/81 02/23/81C	03/17/81 04/06/81C	04/07/81 04/24/81	05/15/81 05/22/81
Release 2			03/06/81 04/08/81C	04/03/81 04/28/81	04/24/81 05/08/81	05/08/81 05/15/81	06/05/81 06/12/81
Release 3			01/16/81 04/08/81C	02/27/81 05/12/81	04/24/81 05/25/81	05/15/81 06/05/81	06/12/81 07/03/81
D/CP, PSL Integration			—	—	—	—	—

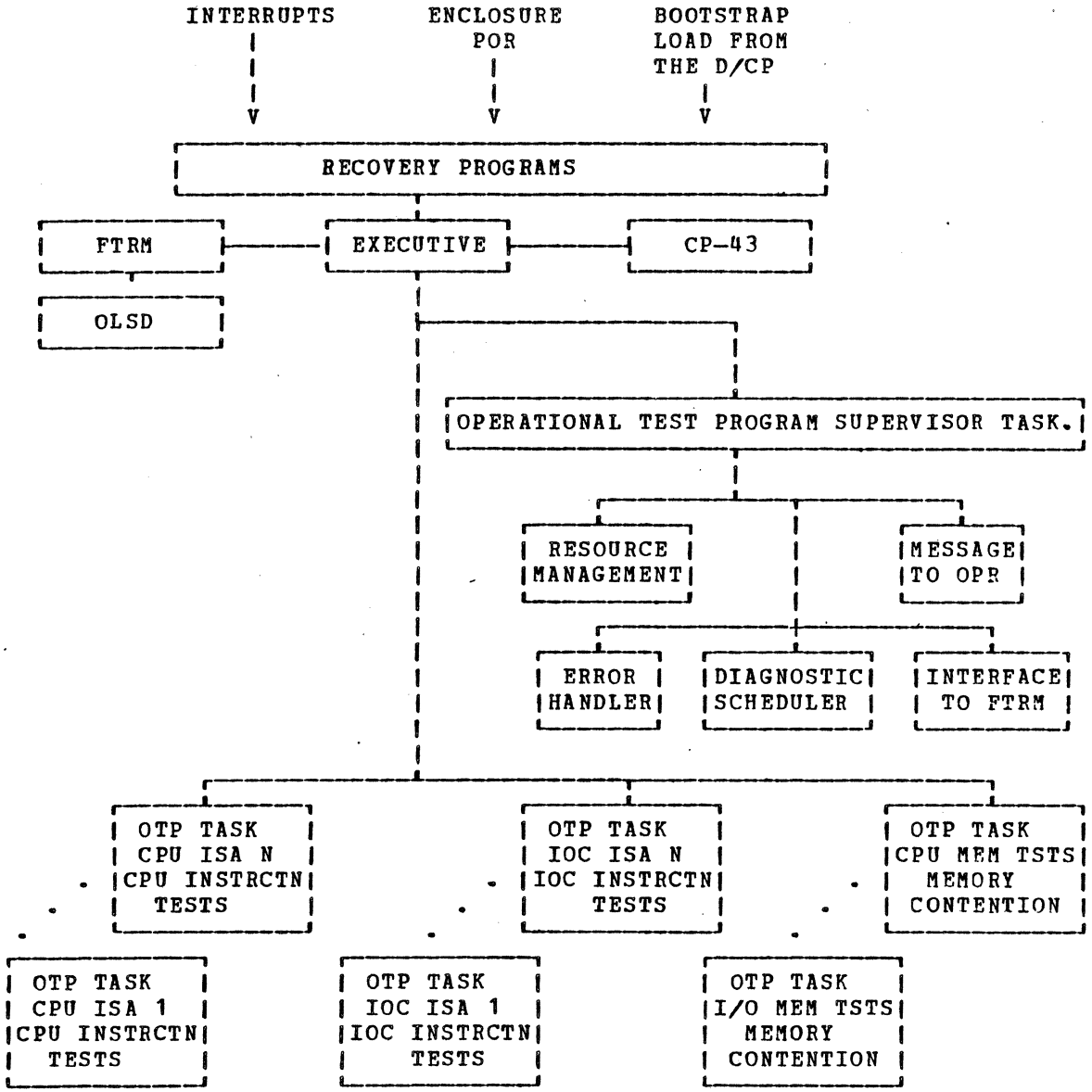
D/CP, CCL SOFTWARE DEVELOPMENT STATUS

Subsystem	Incremental Release	Functional Partition	Status
D/CP	1	Diagnostic selftest	Code and simulation complete
	2	Executive, I/O, interrupt processing Run control pushbutton processing Control mode toggle processing System status display	Code complete Z80 simulation in progress
	3	Operator input/output processing Operator mode processing (CCL Interface)	Code in progress; 50% complete
CCL	1	Diagnostic selftest	Code complete Z80 simulation in progress
	2	Executive, I/O, interrupt processing PSL page control Error detection/reaction	High-level design complete Detailed design in progress
	3	Operator command formatting for bus requests and D/CP responses Bus destination command processing System status message	High-level design complete Detailed design in progress

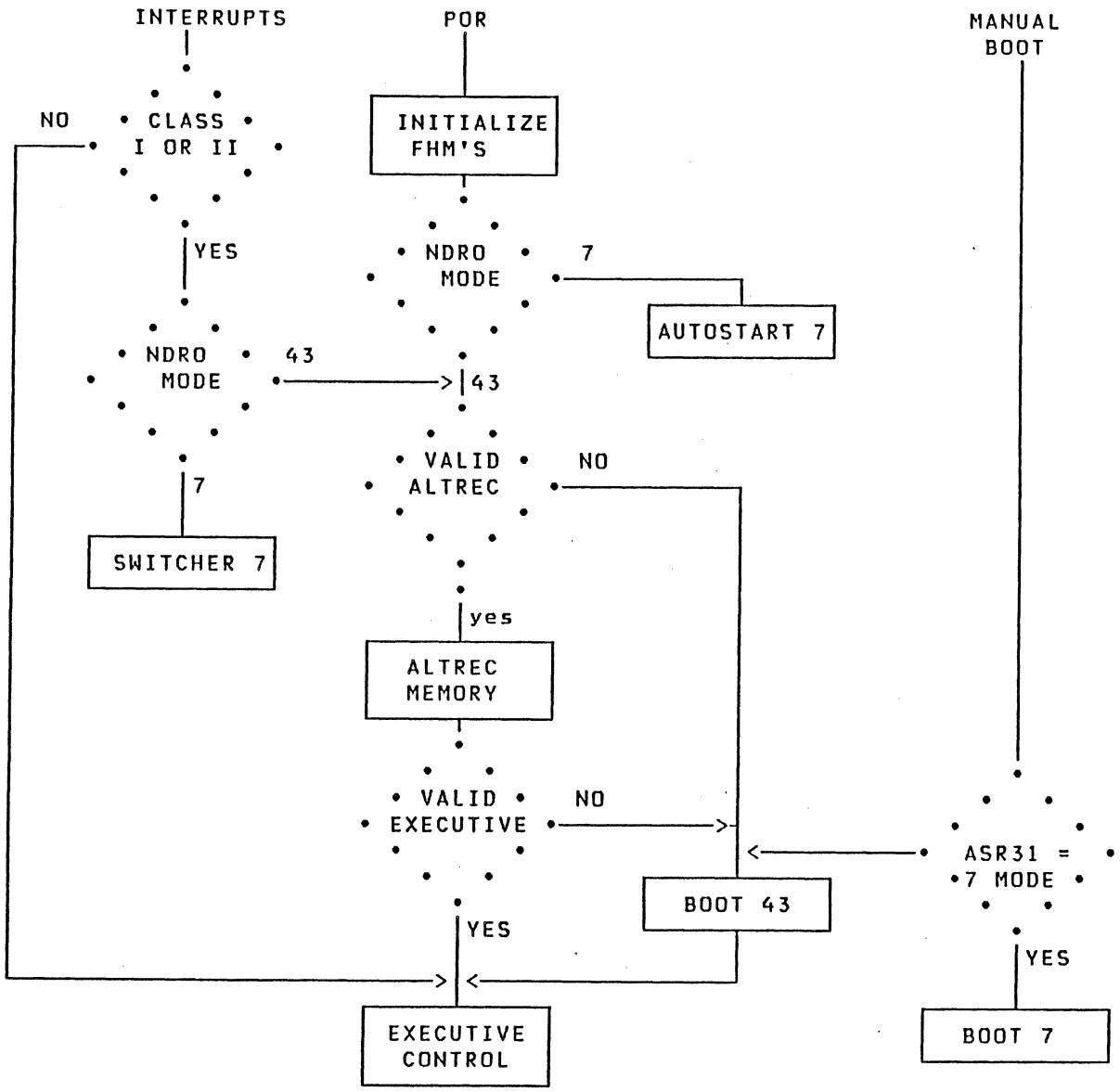
SOFTWARE DEVELOPMENT OVERVIEW

OPERATIONAL SOFTWARE

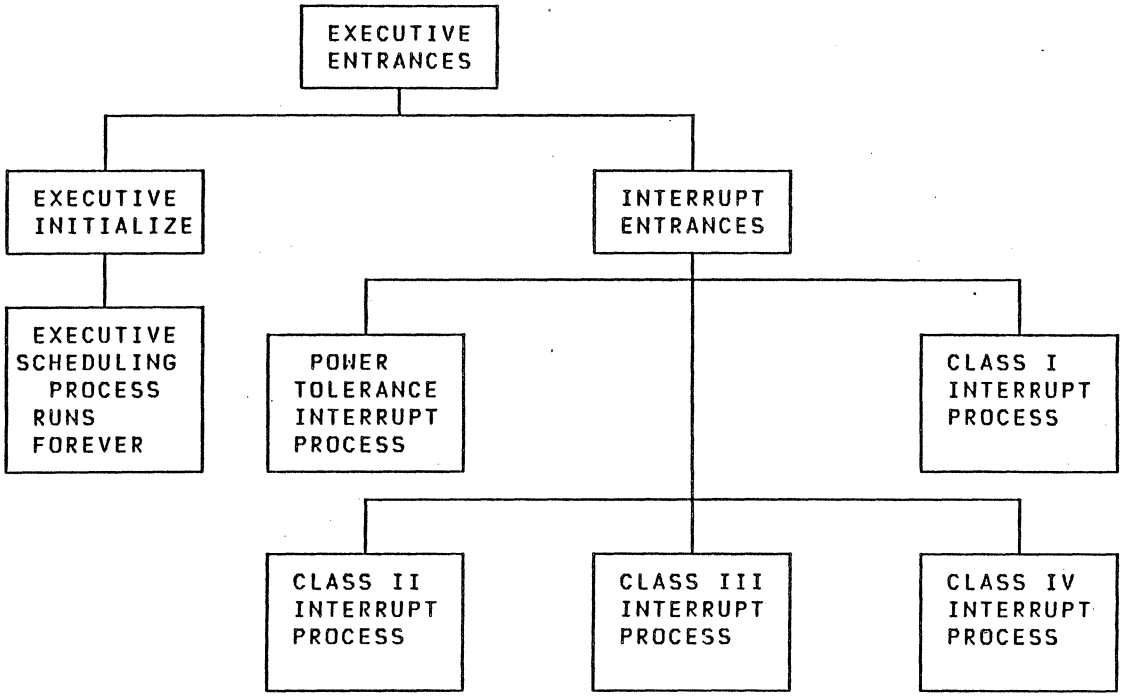
OTP FUNCTIONAL ENVIRONMENT



NDRO RECOVERY PROGRAMS



EXECUTIVE FUNCTIONAL DIAGRAM



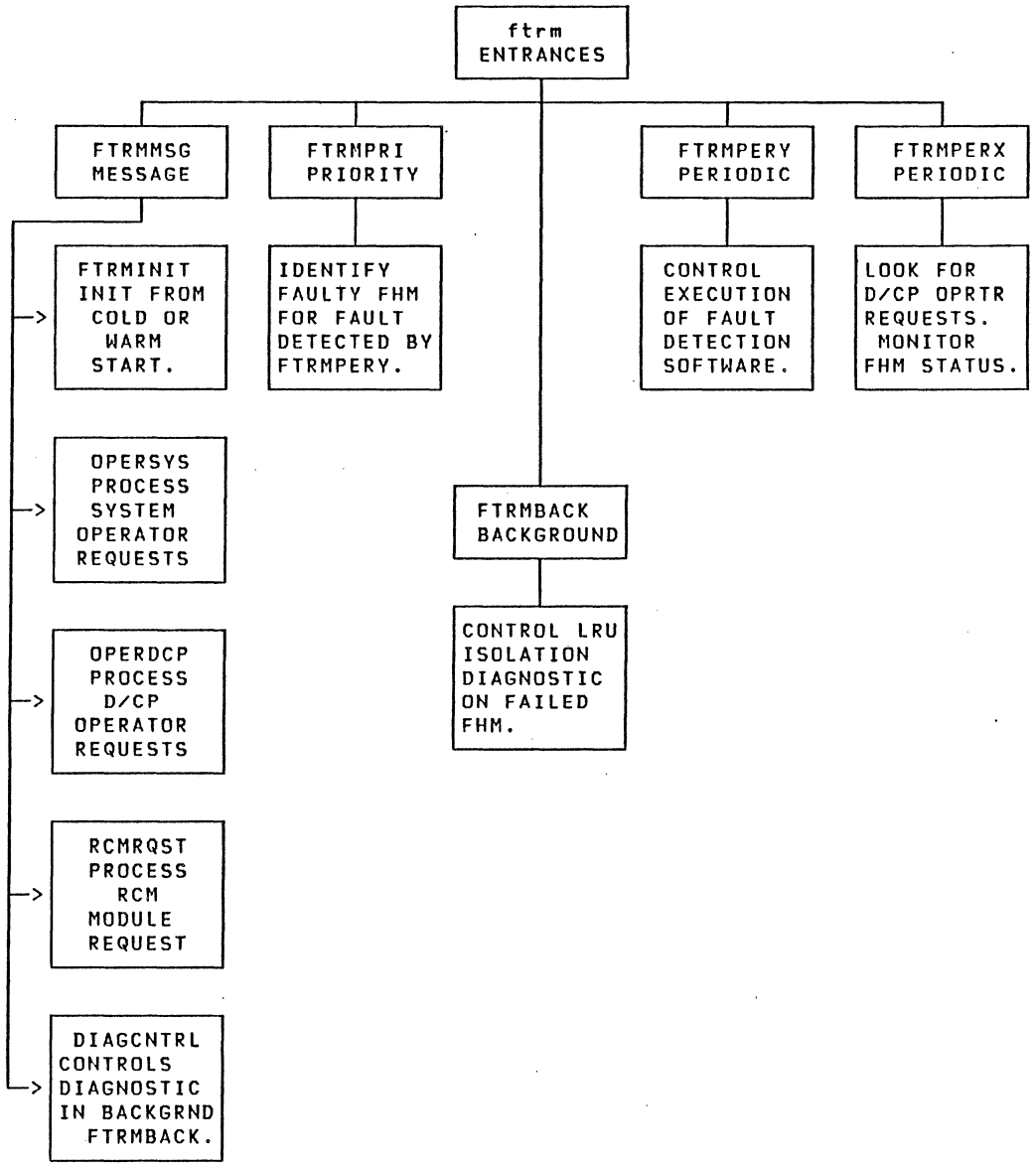
ON ERRORS DETECTED
IN ANY OF THE ABOVE
PROCESSES.

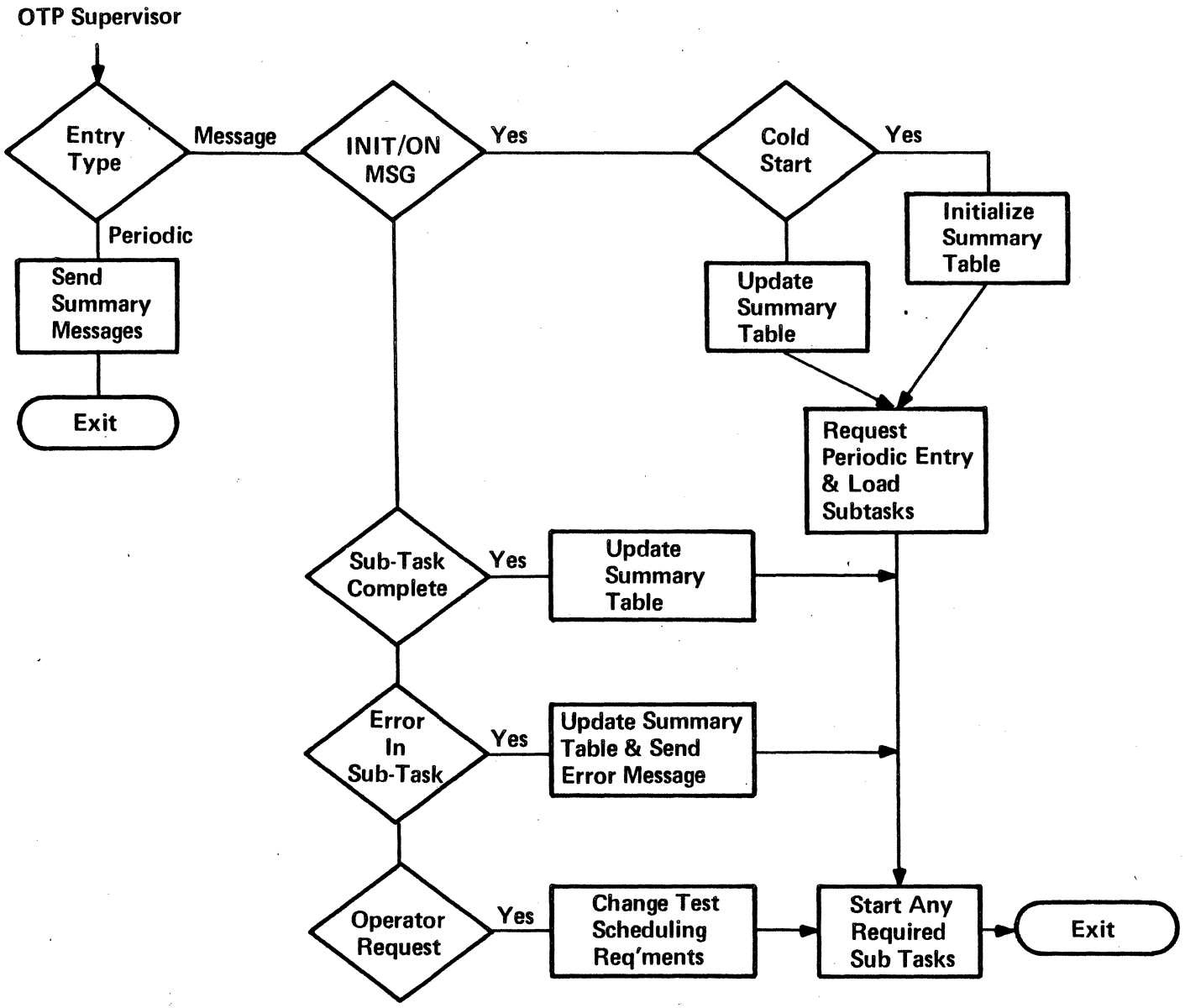
EXECUTIVE ERROR PROCESS

V

AN EXECUTIVE ERROR PACKET
IS SENT TO THE TASK MODULE
RESPONSIBLE FOR ERROR
PROCESSING (FTRM).

FTRM FUNCTIONAL DIAGRAM




OTP Supervisor
Entry Type
Message
INIT/ON MSG
Yes
Cold Start
Yes
Initialize Summary Table
Update Summary Table
Periodic
Send Summary Messages
Exit
Request Periodic Entry & Load Subtasks
Sub-Task Complete
Yes
Update Summary Table
Error In Sub-Task
Yes
Update Summary Table & Send Error Message
Operator Request
Yes
Change Test Scheduling Req'ments
Start Any Required Sub Tasks
Exit

AN/UYK-43 MECHANICAL DESIGN

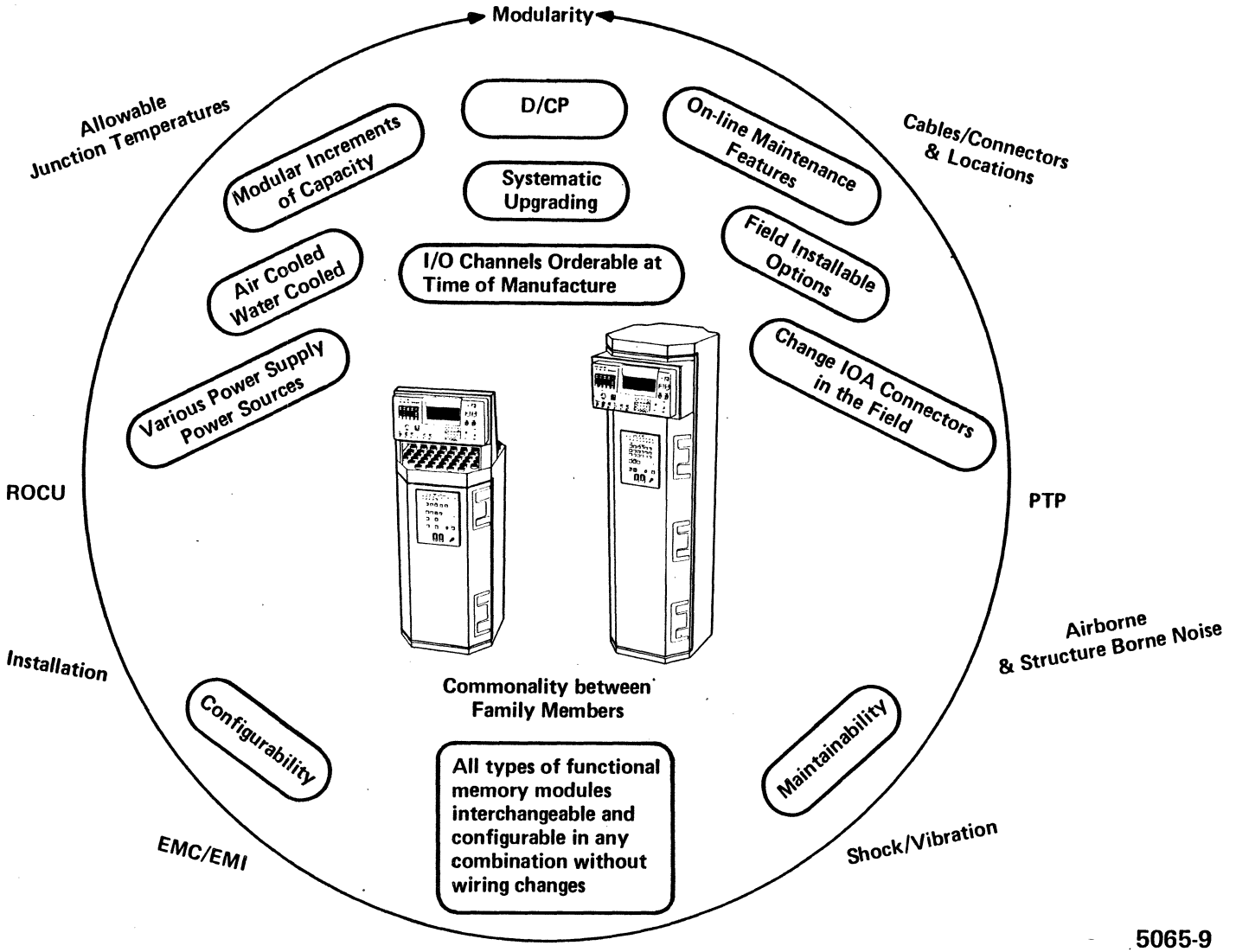
AN/UYK-43 MECHANICAL DESIGN

Mechanical Design – S. G. Yogodzinski
Thermal Analysis – M. Donegan
Structure Analysis – J. Menichello

IBM

5065-8

MAJOR FACTORS IN DEVELOPMENT SPECIFICATION WHICH DICTATED DESIGN



IBM

5065-9

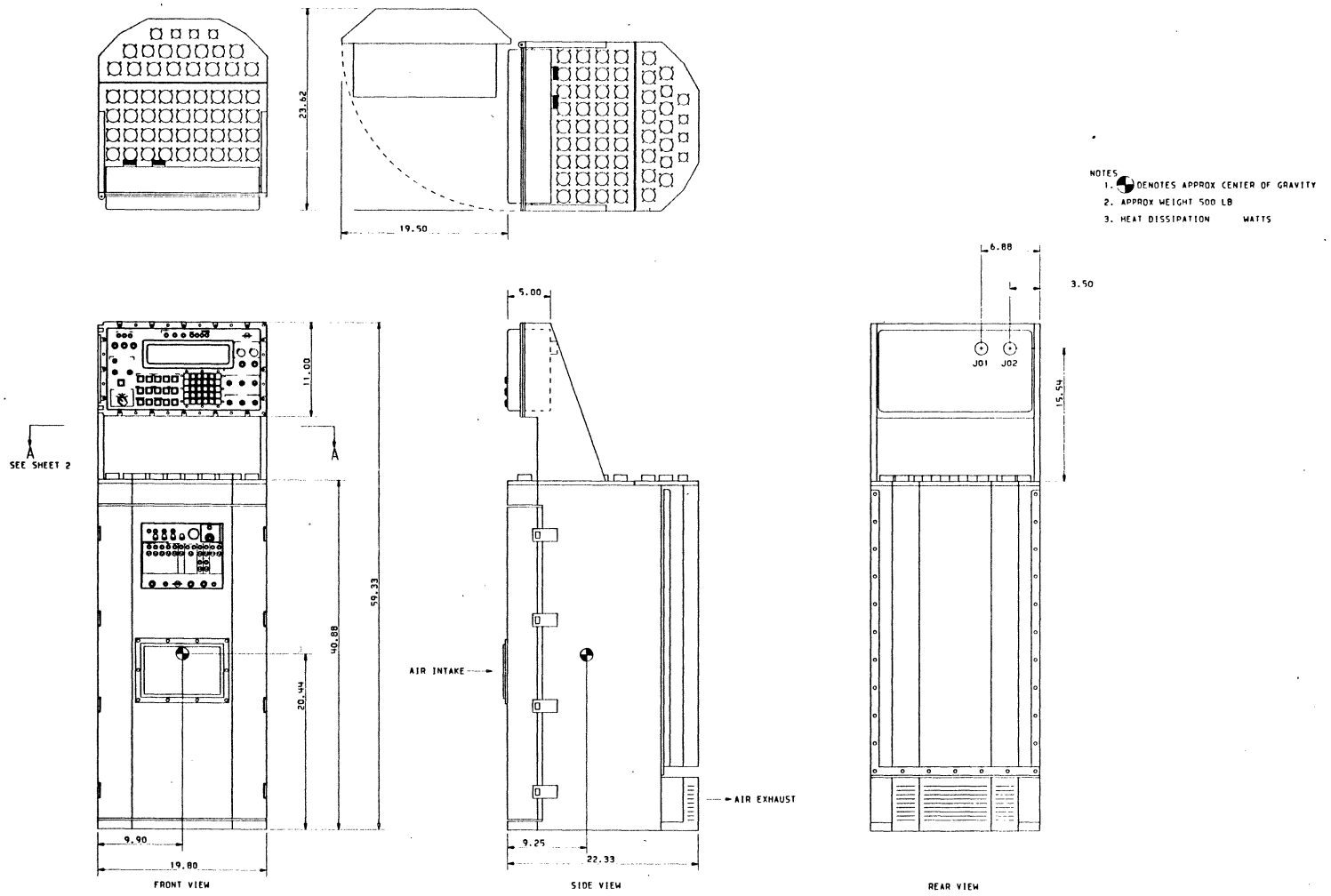
DESIGN PARAMETERS

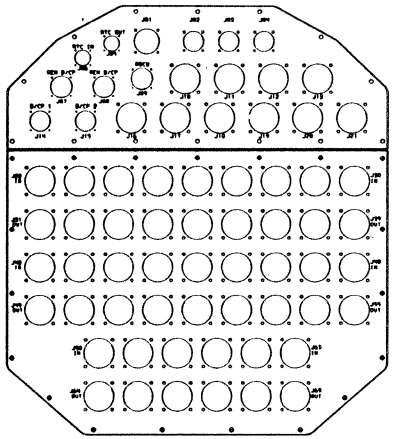
- Installation
- Configurability/Commonality of A/B
- Reliability
- Maintainability
- Shock and Vibration
- Acoustics
- Weight

IBM

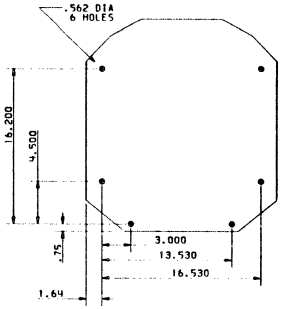
5065-10

A INSTALLATION



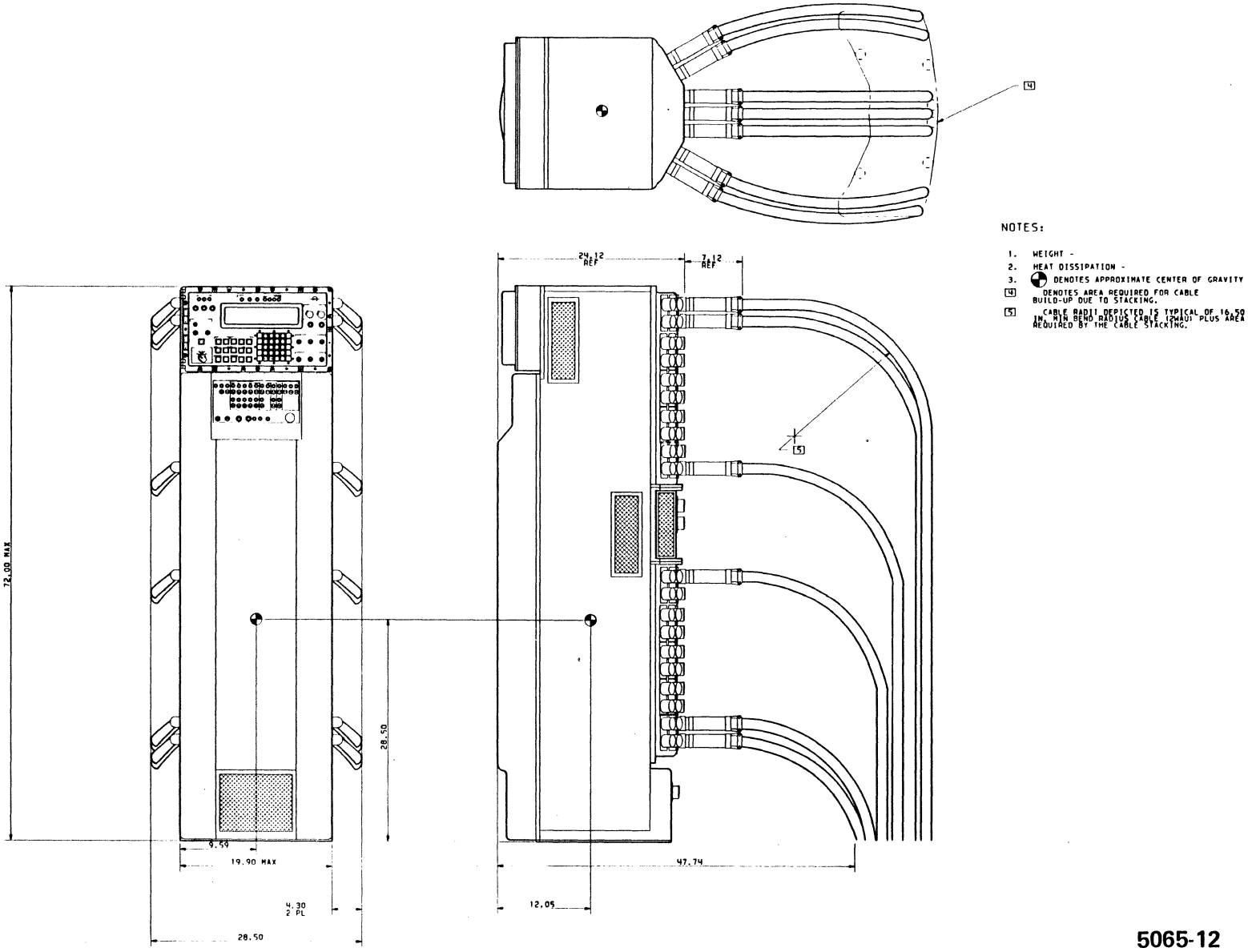


VIEW - A - A
SHEET 1, ZONE D-7
SCALE 1/2



UNIT MOUNTING PATTERN

CONNECTOR REFERENCE DESIGNATION	CONNECTOR PART NUMBER	MATING CONNECTOR PART NUMBER	FUNCTION
A8-J01			INPUT POWER
A8-J02	MS3102R16S-1S	MS3102R16S-1P	D/CP POWER
A8-J03	MS3102R16S-1S	MS3102R16S-1P	REMOTE D/CP POWER
A8-J04	MS3102R16S-1SW	MS3106E16S-1PW	ROCU POWER
A8- J05, J06	HD/12AA1S1	HD/16AA1P1	RTC OUT RTC IN
A8- J10, J11 J12, J13, J16 J17, J18, J19 J20, J21	M28840/12AG1S1	M28840/16AG1P1	CIS SIGNAL
A8- J07, J08	M28840/12AC1P1	M28840/16AC1S1	SIGNAL D/CP REMOTE
A8-J14	M28840/12AE1S1	M28840/16AE1P1	D/CP SIGNAL 1
A8-J09	M28840/12AC1S1	M28840/16AC1P1	ROCU SIGNAL
A8-J15	M28840/12AE1S1	M28840/16AE1P1	D/CP SIGNAL 2
A8-	M81511/01EF01P1	M81511/06EF01S1	SIGNAL-IOA INPUT CHANNELS A,B, C,H
A8-	M81511/01EF01P2	M81511/06EF01S2	SIGNAL-IOA OUTPUT CHANNELS A,B, C,H
A8-	HD/12AA1P1	HD/16AA1S1	SIGNAL-IOA TYPE-F
A8-	36509-2	36506-2	SIGNAL-IOA TYPE-E
A8-	M28840/12AE1P1	M28840/16AE1B1	SIGNAL-IOA TYPE-G
A1-J01	HD/12AE1P1	HD/26CE1B,S1	SIGNAL D/CP
A1-J02	MS3102R16S-1P	MS3106E16S-1S	D/CP POWER

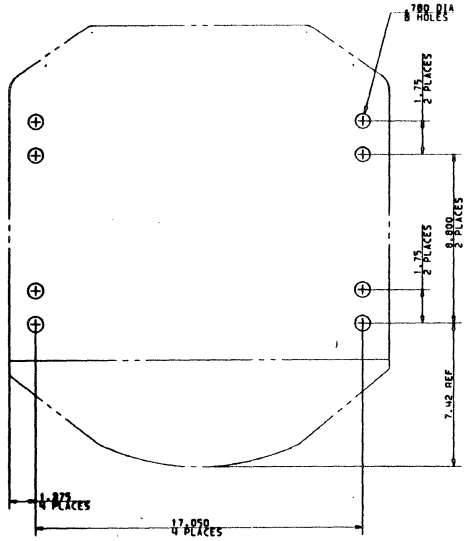


NOTES:

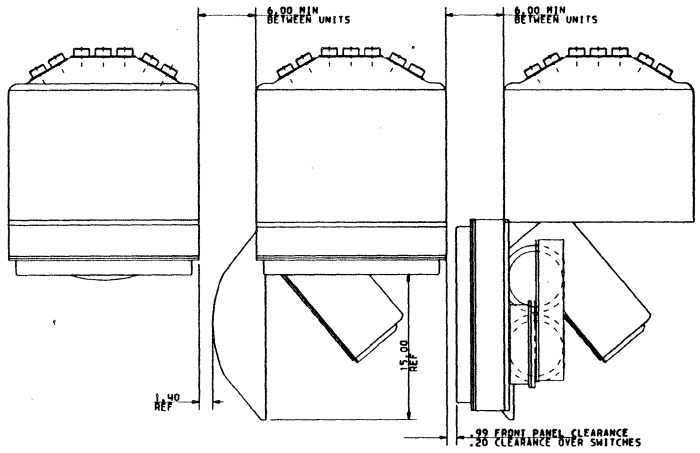
1. WEIGHT -
2. HEAT DISSIPATION -
3. ◔ DENOTES APPROXIMATE CENTER OF GRAVITY
4. [4] DENOTES AREA REQUIRED FOR CABLE BUILD-UP DUE TO STACKING.
5. [5] CABLE RADII DEPICTED IS TYPICAL OF 16.50 IN. MIN BEND RADIUS CABLE (TWAU) PLUS AREA REQUIRED BY THE CABLE STACKING.

IBM

5065-12



INSTALLATION BOLT PATTERN
SCALE=1/2

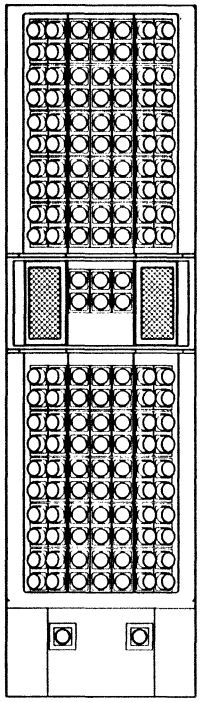


MAIN DOOR SHOWN IN OPEN POSITION AND CHASSIS IN OPEN POSITION

MAIN DOOR AND D/CP SHOWN IN OPEN POSITION

IBM

5065-13



VIEW A-A
SHEET 1 ZONE B-3

CONNECTOR INFORMATION FOR EDM 2

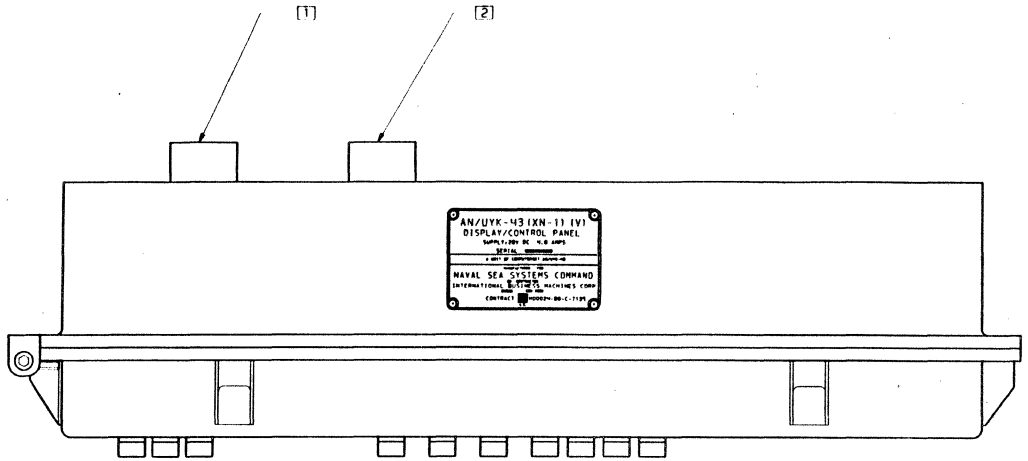
FUNCTION	CONNECTOR PART NUMBER	MATING CONNECTOR	QUANTITY
INPUT POWER (TYPE 4)	MS3102R24-10PW	MS3106E24-10SW	1 (1 SP. ORDER)
INPUT POWER (TYPE 6)	MS3102R20-15P	MS3106E20-15S	1
POWER TO D/CP	MS3102R16S-1S	MS3106E16S-1P	1
POWER TO ROCU	MS3102R16S-1SW	MS3106E16S-1PW	1
SIGNAL-D/CP	M28840/12AE1S1	M28840/16AE1P1	1
SIGNAL-ROCU	M28840/12AC1S1	M28840/16AC1P1	1
SIGNAL-CIS	M28840/12AG1S1	M28840/16AG1P1	10
SIGNAL-IOA (IN) CHANNELS A,B,C,H	M81511/01EF01P1	M81511/06EF01S1	54
SIGNAL-IOA (OUT) CHANNELS A,B,C,H	M81511/01EF01P2	M81511/06EF01S2	54
SIGNAL-IOA CHANNEL F (1553)	M28840/12AA1P1	M28840/16AA1S1	2
SIGNAL-IOA CHANNEL G (RS449)	M28840/12AE1P1	M28840/16AE1S1	4
SIGNAL-IOA CHANNEL E (SERIAL)	M49142/02-0002	M49142/01-0002	8
SIGNAL-REMOTE DEVICE	M28840/12AC1P1	M28840/16AC1S1	2
SIGNAL-REAL TIME CLOCK	M28840/12AA1S1	M28840/16AA1P1	2

CONNECTOR INFORMATION FOR EDM 3

FUNCTION	CONNECTOR PART NUMBER	MATING CONNECTOR	QUANTITY
INPUT POWER (TYPE 2)	MS3102R24-10P	MS3106E24-10S	2 (SP. ORDER)
INPUT POWER (TYPE 6)	MS3102R20-15P	MS3106E20-15S	2
POWER TO D/CP	MS3102R16S-1S	MS3106E16S-1P	1
POWER TO ROCU	MS3102R16S-1SW	MS3106E16S-1PW	1
SIGNAL-D/CP	M28840/12AE1S1	M28840/16AE1P1	1
SIGNAL-ROCU	M28840/12AC1S1	M28840/16AC1P1	1
SIGNAL-CIS	M28840/12AG1S1	M28840/16AG1P1	10
SIGNAL-IOA (IN) CHANNELS A,B,C,H	M28840/12AG1P1	M28840/16AG1S1	50
SIGNAL-IOA (OUT) CHANNELS A,B,C,H	M28840/12AG1P2	M28840/16AG1S2	50
SIGNAL-IOA CHANNEL F (1553)	M28840/12AA1P1	M28840/16AA1S1	4
SIGNAL-IOA CHANNEL G (RS449)	M28840/12AE1P1	M28840/16AE1S1	4
SIGNAL-IOA CHANNEL E (SERIAL)	M49142/02-0002	M49142/01-0002	12
SIGNAL-REMOTE DEVICE	M28840/12AC1P1	M28840/16AC1S1	2
SIGNAL-REAL TIME CLOCK	M28840/12AA1S1	M28840/16AA1P1	2

5065-14

D/CP INSTALLATION



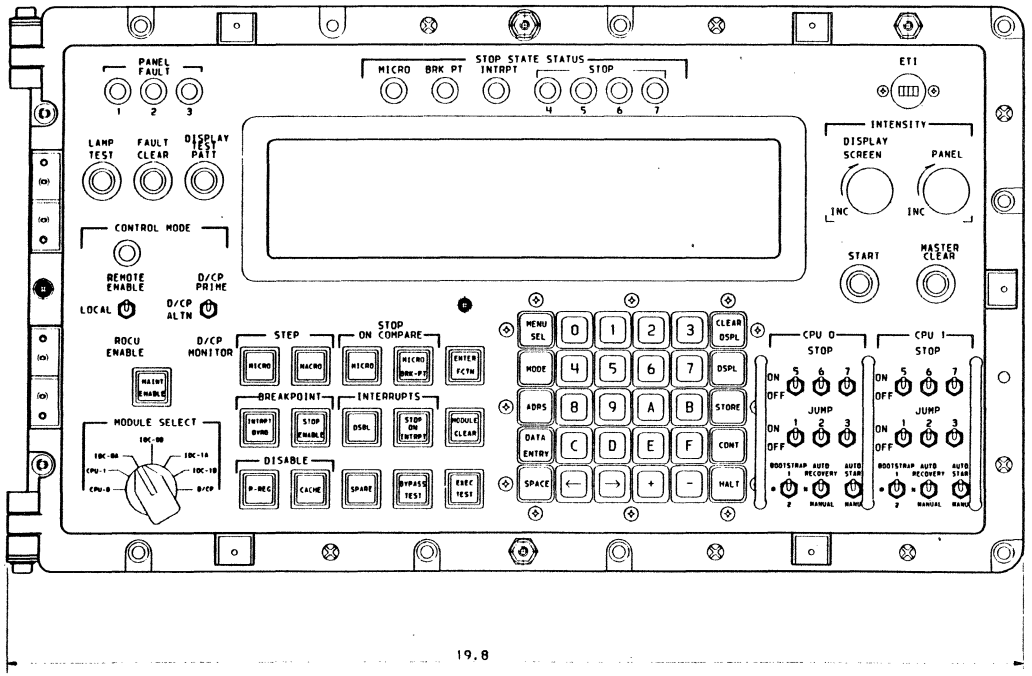
NOTES

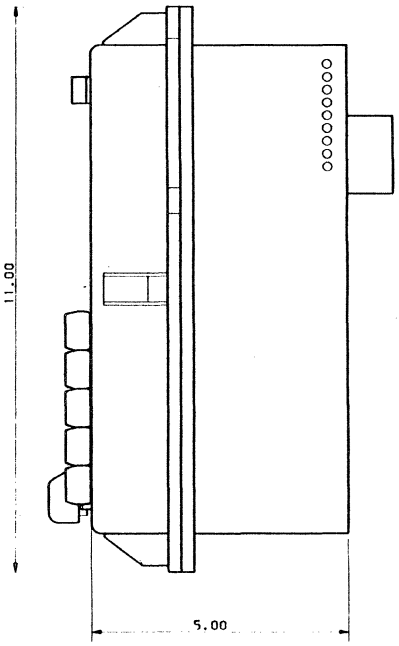
[1] INPUT POWER CONNECTOR MS3102R16S-1P

[2] I/O CONNECTOR M28840/12AE1S1

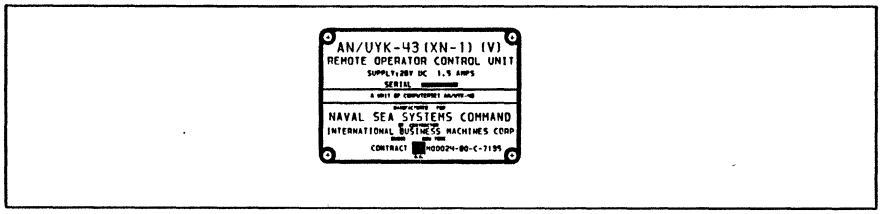
[3] WEIGHT = 30 LBS APPROX

[4] POWER = 60 WATTS APPROX





ROCU
INSTALLATION DIAGRAM

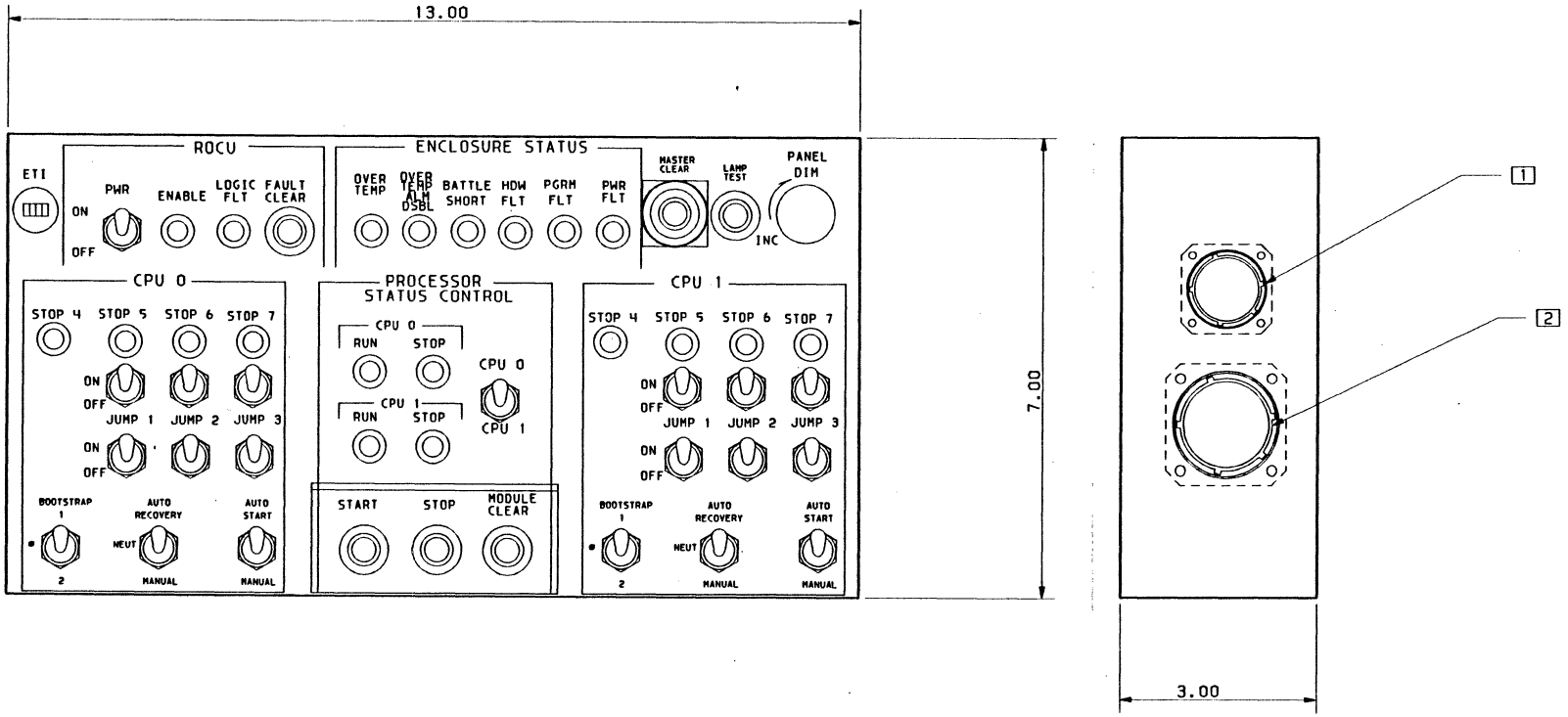


NOTES

[1] POWER CONN.MS3102R16S-1PW

[2] I/O CONN.M28840/12AC1S1

3 POWER 25 WATTS



DISPLAY PANEL SELECTION

Technology	Accept	Reject	Reasons
CRT		X	• Size • Power • Packaging to meet environment
LED		X	• Size problem for required number of characters • Not hermetically sealed • No brightness control • Excessive power
Electro-Luminescence		X	• Large area grid • Potentially non shock resistant • Technology not hardened
Gas Panels			
D.C. Plasma		X	• Contains mercury • Requires continuous refresh
A.C. Plasma	X		• Size/form factor • Inherent long life • Used in military application • Controllable brightness • Low power requirements • Character density (704 characters)

IBM

5065-17

LRU MODULE SELECTION

- Standardization
  Modular computer series (MCS) standard IBM Owego
  LRU selected for AN/UYK-43
  – All processes and technologies in place
  – Successful historical data on previous programs, B52, E3A NATO
    -- Thermal characteristics
    -- Shock/vibration resistance
    -- Reliability
- Larger LRU Size Relative to SEM, ISEM Provides Better Logic Partitioning
- Facilitates Fault Detection Design
- Requires Fewer Number of Unique Part Numbers
- Lower Initial Costs Compared to Smaller Modules

IBM

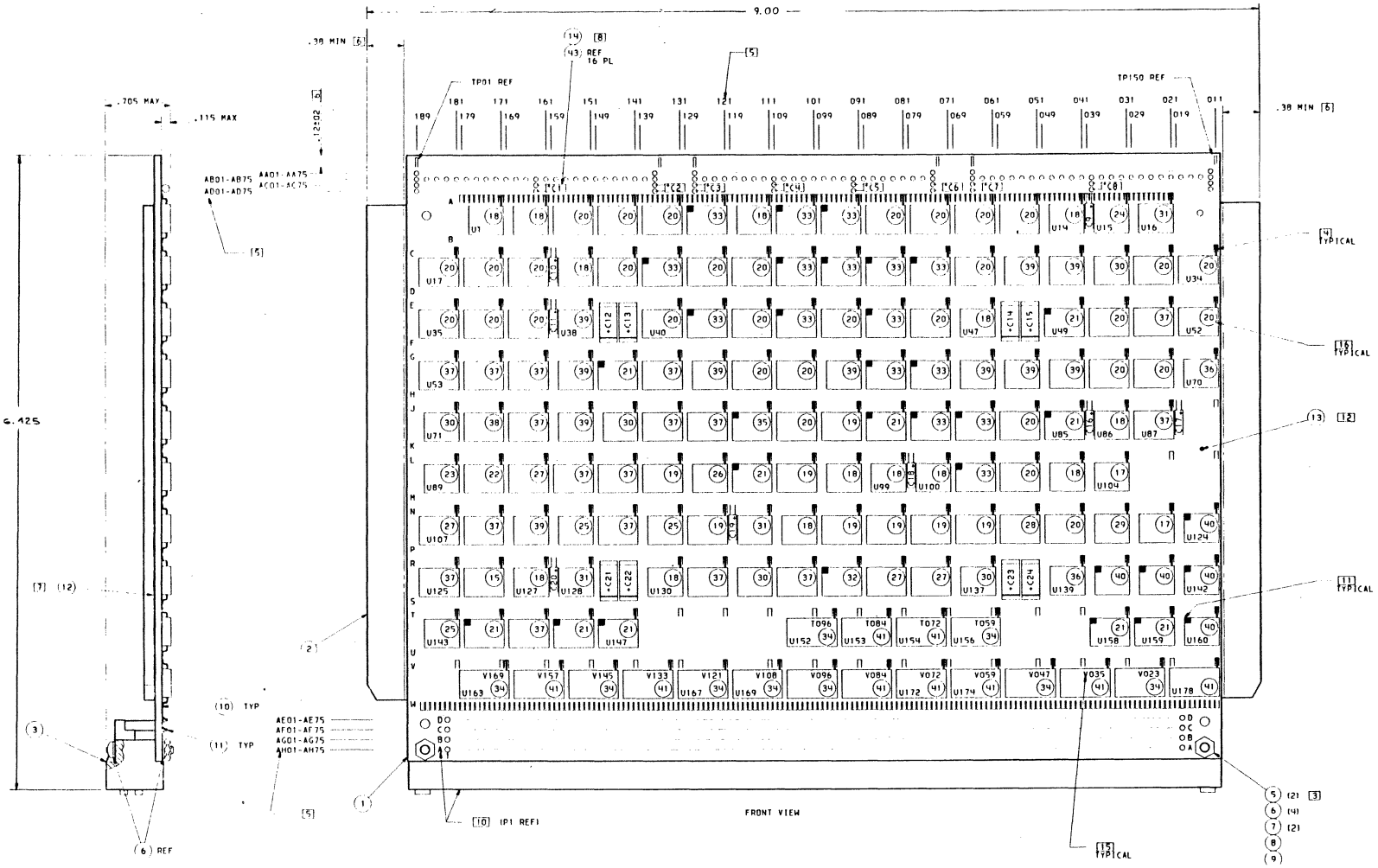
5065-18

AN/UYK-43 LRU Summary

Function	Max. # of Unique LRU's	Page Design		Size of LRU	A Enclosure		B Enclosure	
		Single MIB	Double MIB		# of Functions	# of LRU's	# of Functions	# of LRU's
CPU + Options	17	8	9	9.0 x 6.38 x .72	1	18	2	36
IOC	6	3	3	9.0 x 6.38 x .72	1	7	2	14
IOA	9	6	3	8.1 x 4.80 x .72	24	24	64	64
MEMORY								
Core or	1			9.0 x 6.40 x 1.0	5	10	10	20
SCM	2			9.0 x 6.40 x .72				
Regulator	2			9.0 x 6.40 x 1.0	5	5	10	10
Memory Bussing	8	6	2	9.0 x 6.38 x .72	1	11	1	17
CIS	7	2	5	8.1 x 4.80 x .72	1	10	1	10
POWER SYSTEM								
Converters	2			9.0 x 6.38 x 2.25	5	5	8	8
Regulators	1			8.1 x 4.80 x 2.60	1	1	2	2
28V Protect	1			8.1 x 4.80 x .72	1	1	1	1
UNIQUE LRU's	56			MAX LRU's		92		182

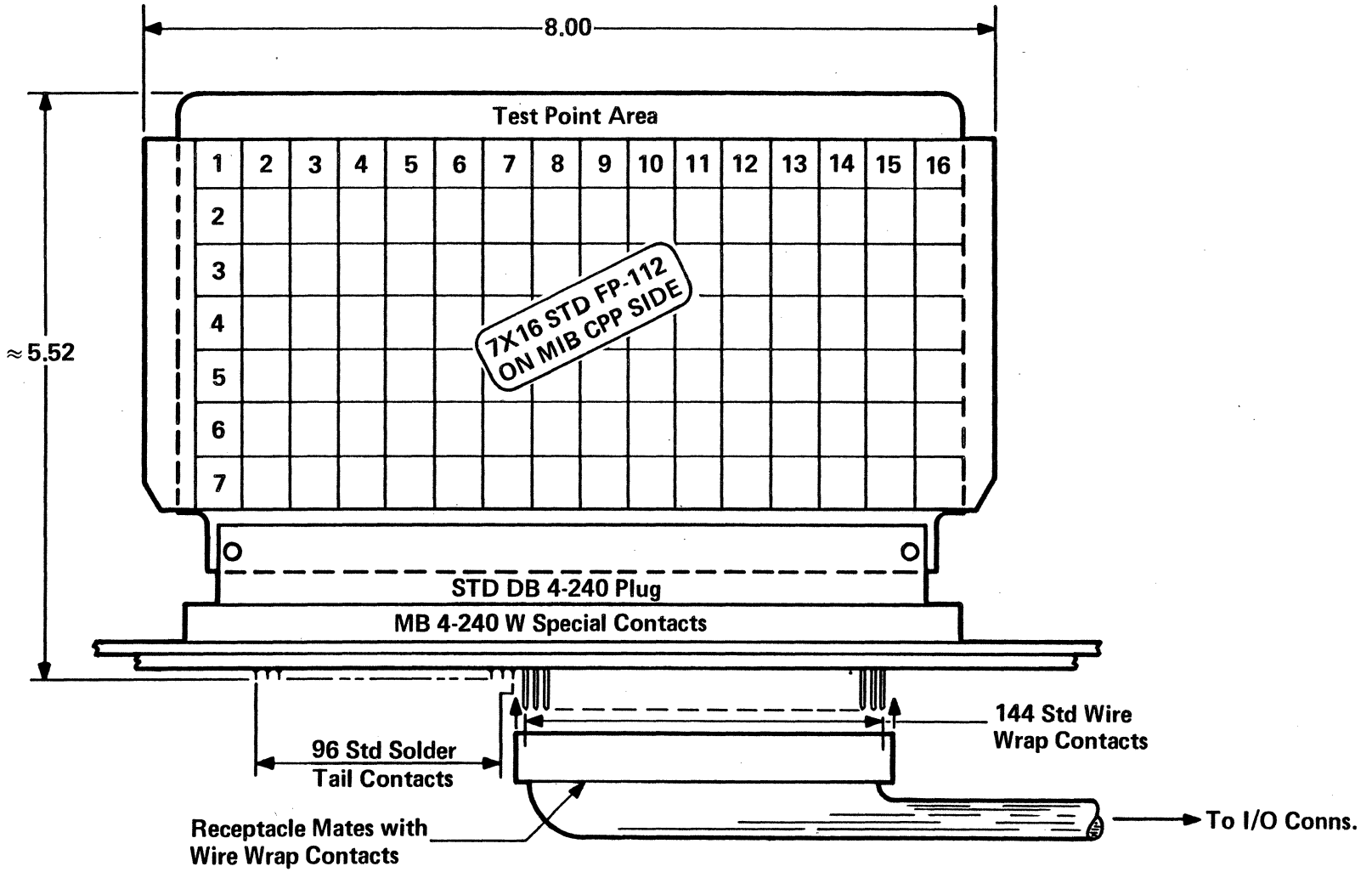
*Does not include PTP, DCP, or ROCU

TYPICAL STANDARD LOGIC LRU



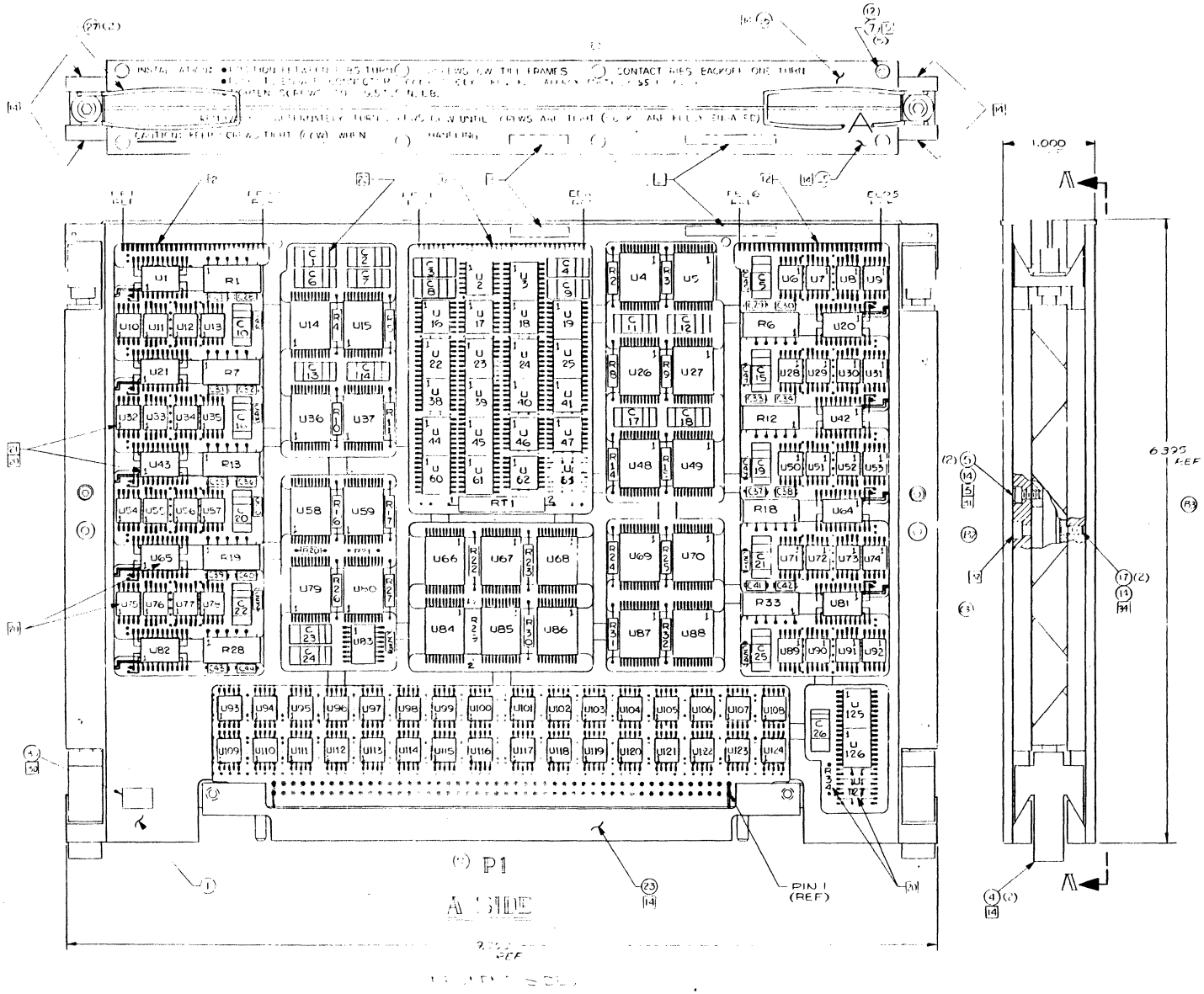
	1 MIB	2 MIBs
I/O	225/300	225/300
Test Points	300	300
Standard F.P. Pos.	178	258
Feed Thru	–	288

IOA/CIS PAGE

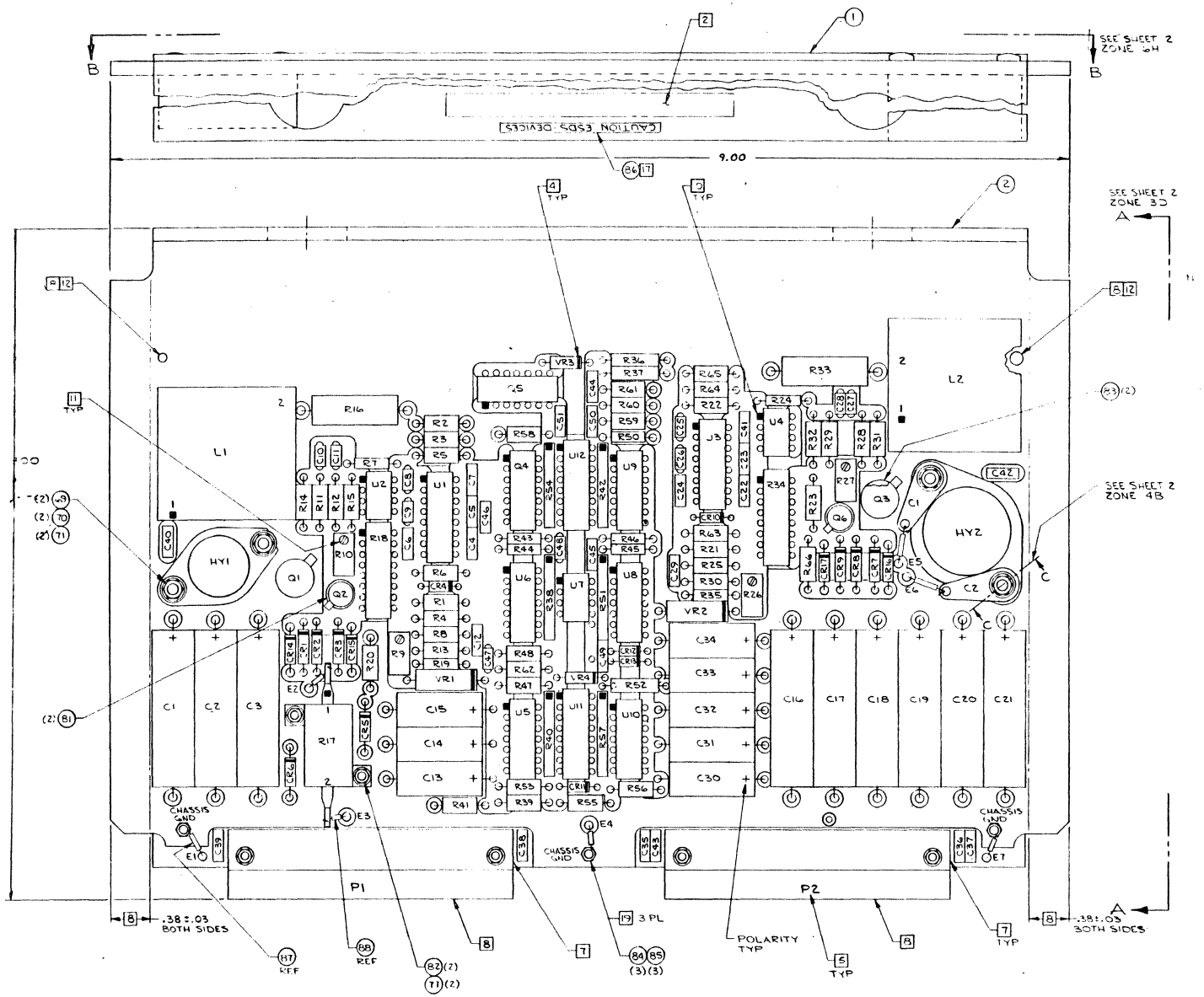


5065-18-3

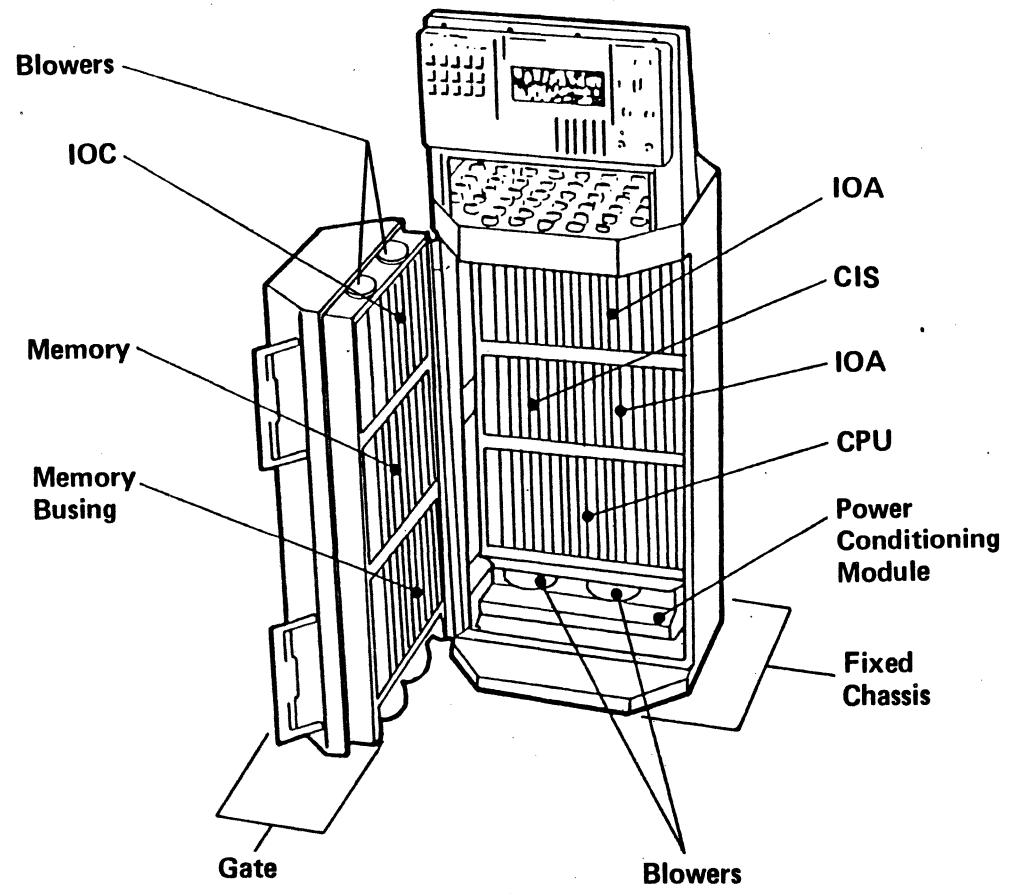
CORE MEMORY



REGULATOR


SEE SHEET 2 ZONE 6H
SEE SHEET 2 ZONE 3D
SEE SHEET 2 ZONE 4B
9.00
.38 ±.03 BOTH SIDES
3 PL
POLARITY TYP
TYP
P1
P2
L1
L2
HY1
HY2
CHASSIS GND
REF

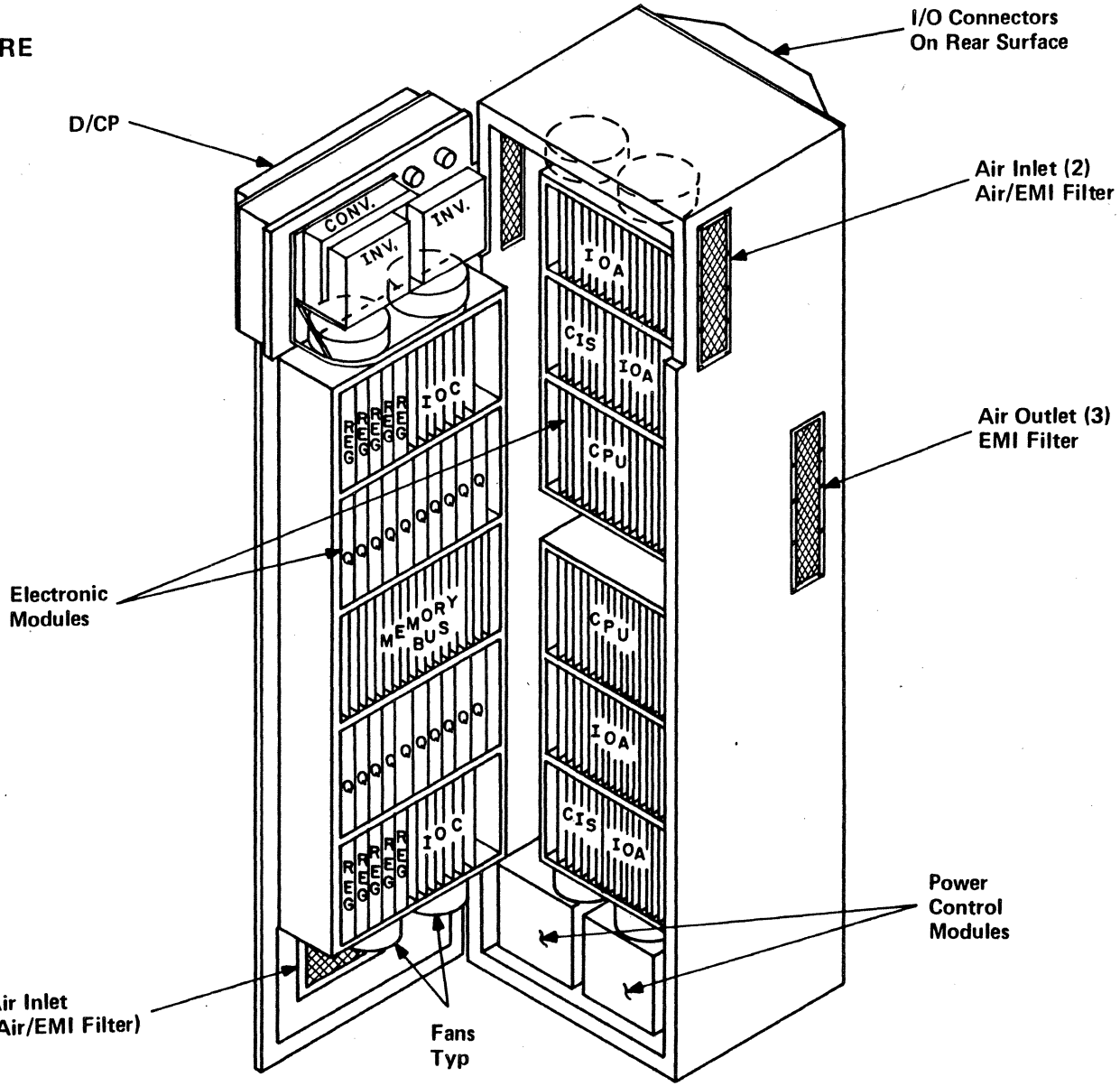
"A" ENCLOSURE



IBM

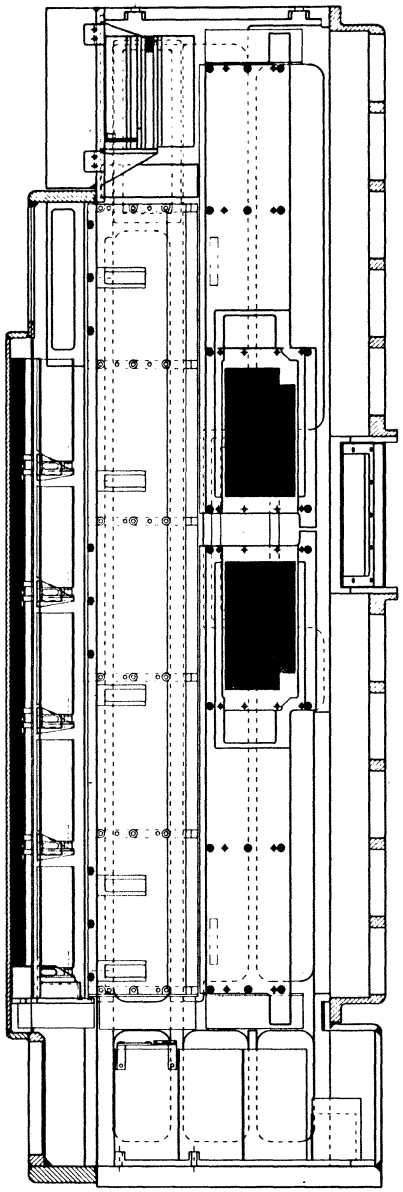
5065-21

"B" ENCLOSURE



IBM

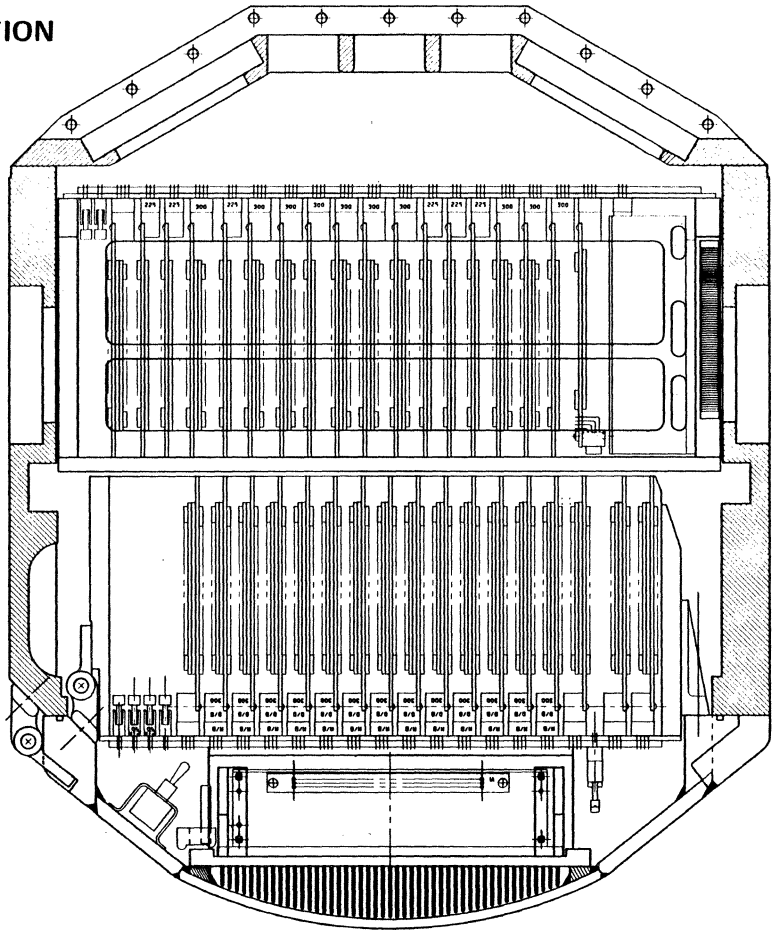
5065-22



IBM

5065-23

AIR EXHAUST SECTION

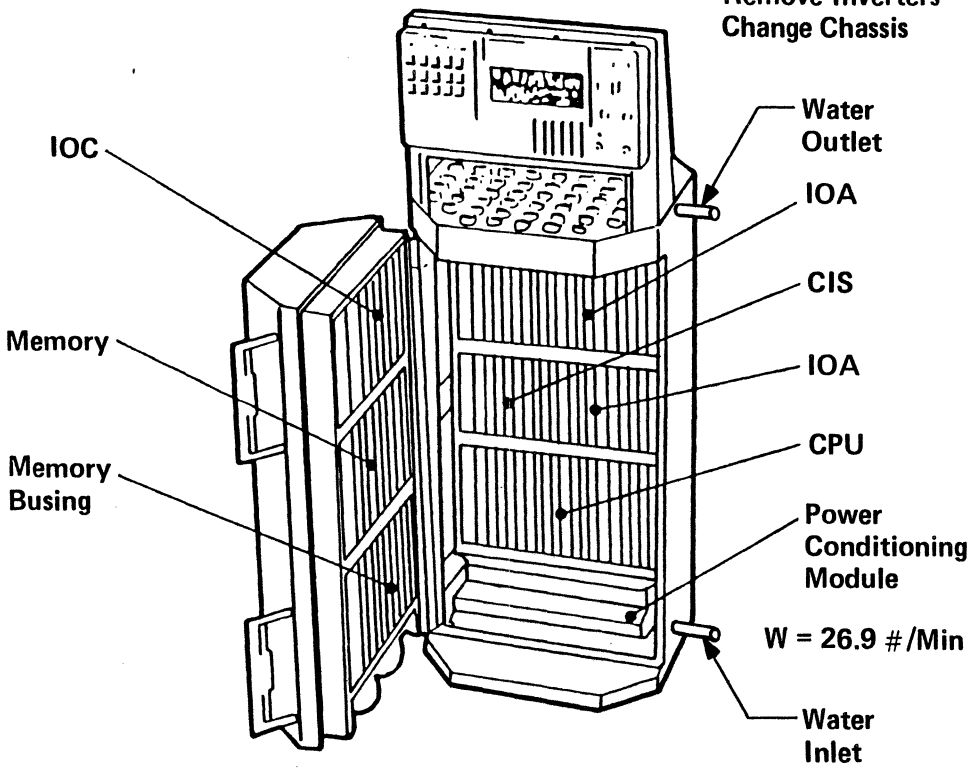


IBM

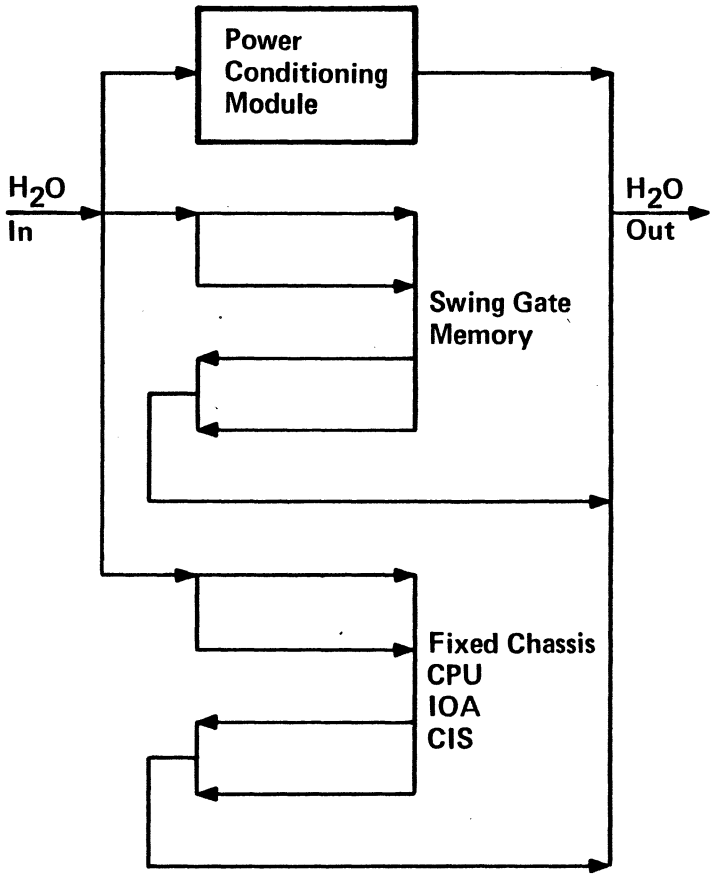
5065-24

LIQUID COOLED A UNIT

Concept: Heat Conduction From LRU's and Heat Producting Modules to Liquid Cooled Copper Heat Sinks.

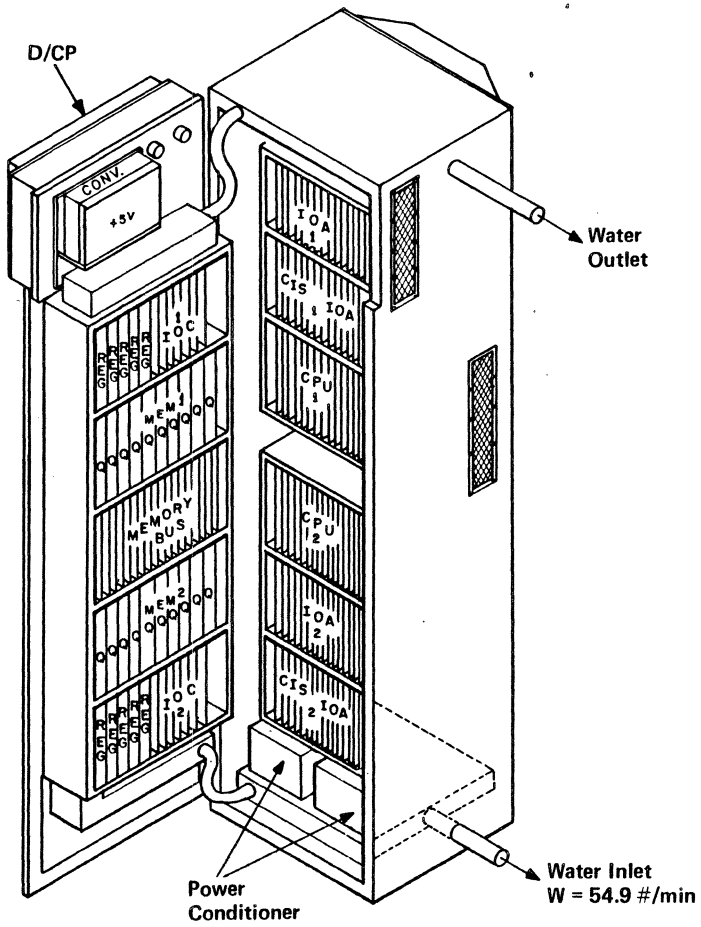


SERIES/PARALLEL FLOW PATHS



LIQUID COOLED B UNIT

Concept: Heat Conduction To A Copper Liquid Cooled Heat Sink



Δ Air to Liquid
Remove Fans
Remove Inverters
Change Chassis

Series/Parallel Flow Path

5065-24-2

DEVELOPMENT TEST DATA

- Following LRU's have been subjected to light weight hammer tests per MIL-STD-901C at independent testing laboratory.
  - Logic LRU
  - Power supply converter
  - Modular core memory
  - Plasma panel
- Shock tested LRU's, which are representative of all AN/UYK-43 modules, exhibited no apparent failures.
- Memory bus backpanels have been designed, built and tested to validate the electrical characteristics of a high impedance backpanel.
- Evaluating structure borne noise from fans.
- Air flow distribution has been evaluated.

IBM

5065-26

PRODUCIBILITY

- All materials, parts, and processes used in the AN/UYK-43 hardware have been in place within the facility or used on previous programs such as B-52D (DBNS), B-52 G&H Computer, and E-3A NATO.
- The memory bus backpanel, previously discussed, also verified manufacturability utilizing existing materials, parts and processes.
- The structural side walls to base has been welded and evaluated.

IBM

5065-27

PERFORMANCE MONITOR LRU MATING CONNECTOR

Item	[3] Bendix Part Number	Quantity
Connector Body	IO4-272C	1
[1] Polarization Key	10-285422-2	4
[2] Crimp Contact	10-502588-3	272

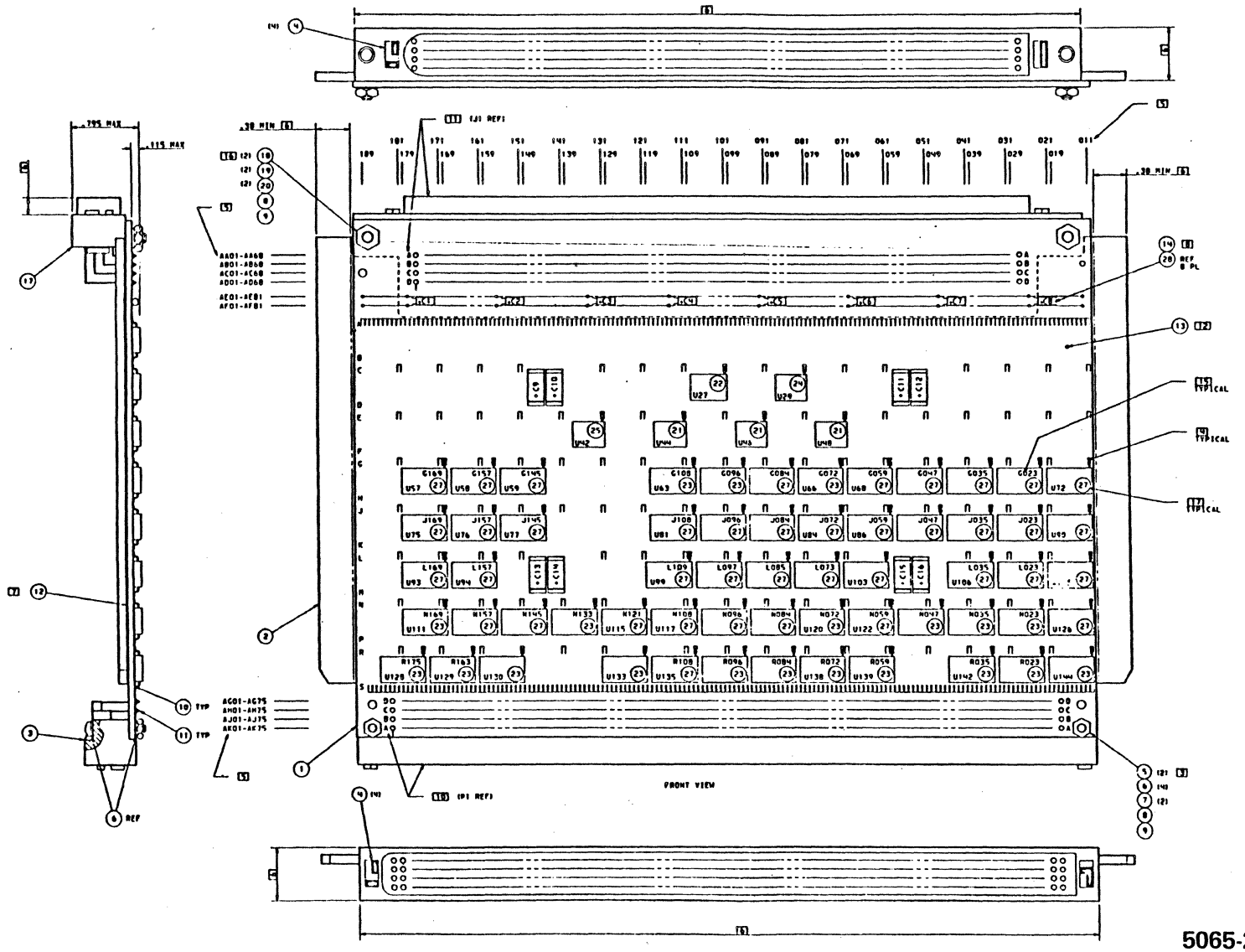
NOTE: [1] Polarization keys to be assembled in key locations 3 & 5 and A & H

[2] Size 22D wire well will accommodate 22 to 28 Awg wire

[3] Bendix Electrical Components Division
Sidney, N.Y., 13838
Phone (607) 563-5301

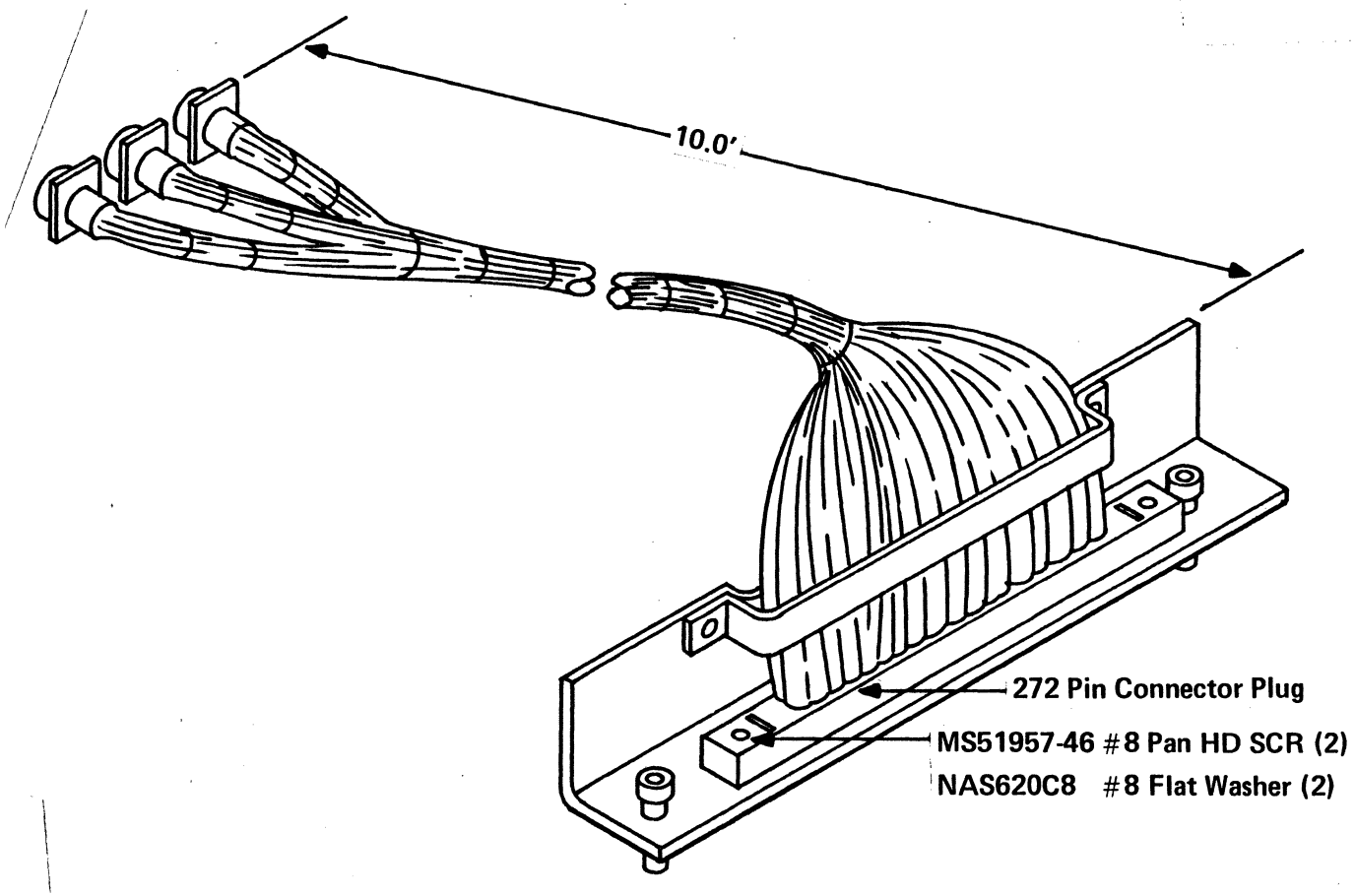
IBM

5065-28



5065-29

INTERFACE CABLE, PERFORMANCE MONITOR



P.D. 3.4.1.1.1.1/3.4.1.1.1.2

A ENCLOSURE SHALL WEIGH NO MORE THAN 500 lbs.

B ENCLOSURE SHALL WEIGH NO MORE THAN 750 lbs.

WEIGHT ANALYSIS

Subassembly	Current Weight
IOA	25.5
CIS	15.5
CPU	24.5
IOC	10.5
Memory	56.0
Power Supply	81.5
DCP and Mount	40.0
P/TP	6.8
Structure/Rack/Cables/Miscellaneous	308.5
Total	568.8

AN/UYK-43 Type A Enclosure Weight

Subassembly	Current Weight
IOA	68.3
CIS	15.5
CPU	50.0
IOC	20.0
Memory	112.0
Power Supply	167.0
DCP	30.0
P/TP	6.8
Structure/Rack/Cables/Miscellaneous	601.0
Total	1070.6

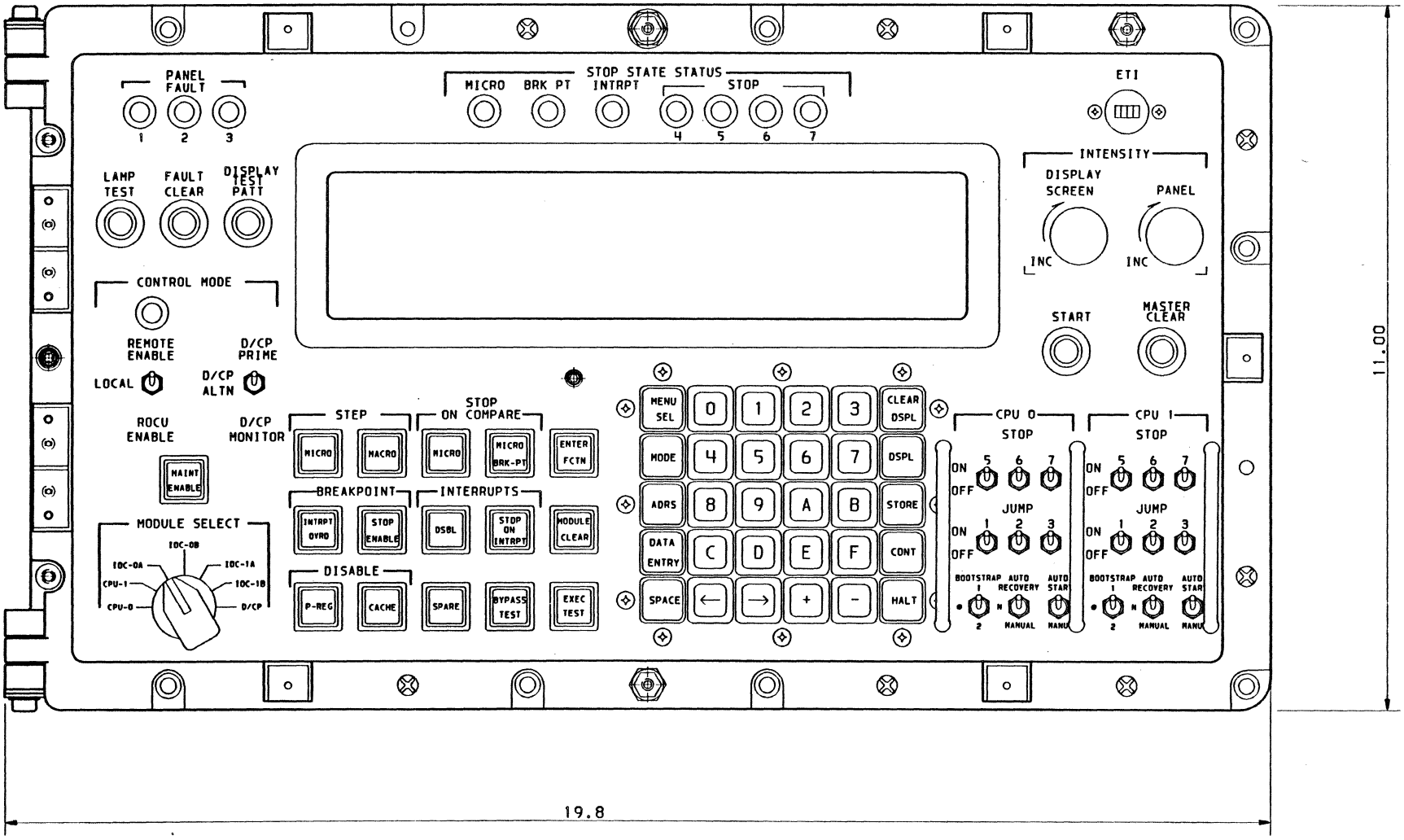
AN/UYK-43 Type B Enclosure Weight

ACTION ITEM

IBM TO REVIEW D/CP AND ROCU SWITCH/BUTTON PROTECTION

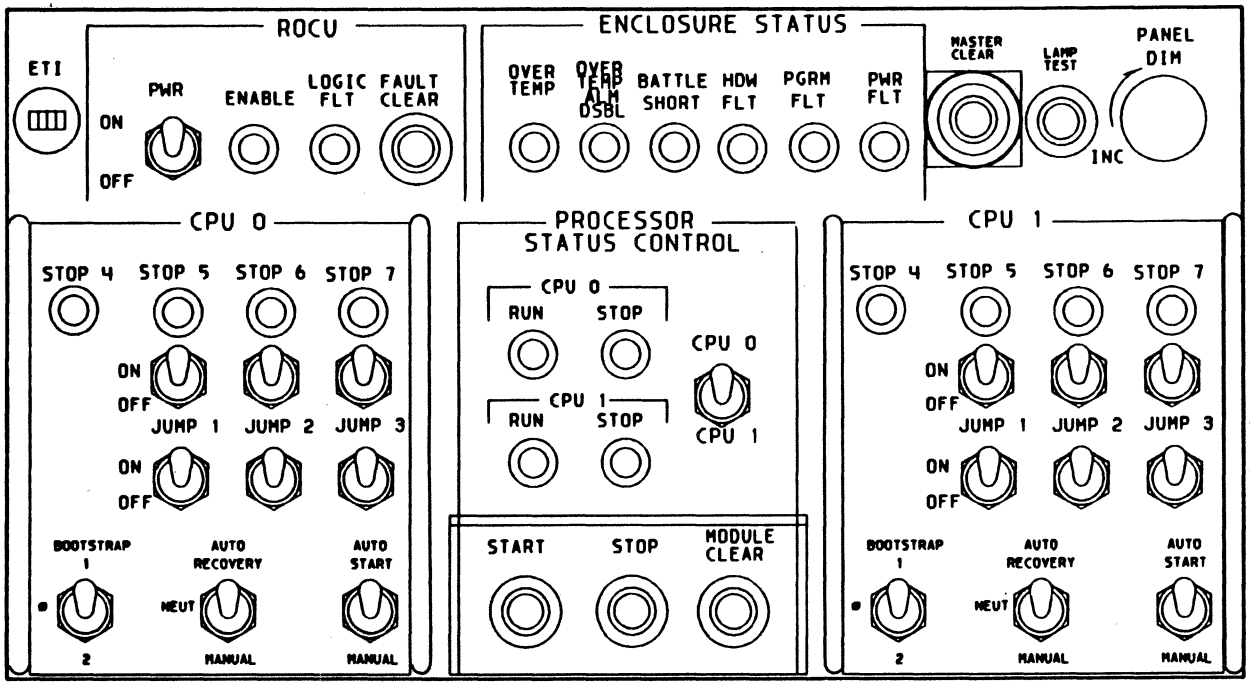
IBM

5065-31


PANEL FAULT
1
2
3
STOP STATE STATUS
MICRO
BRK PT
INTRPT
STOP
4
5
6
7
ETI
LAMP TEST
FAULT CLEAR
DISPLAY TEST PATT
INTENSITY
DISPLAY SCREEN
PANEL
INC
INC
CONTROL MODE
REMOTE ENABLE
D/CP PRIME
LOCAL
D/CP ALTN
START
MASTER CLEAR
ROCU ENABLE
D/CP MONITOR
MAINT ENABLE
STEP
MICRO
MACRO
STOP ON COMPARE
MICRO
MICRO BRK-PT
ENTER FCTN
BREAKPOINT
INTRPT DVRD
STOP ENABLE
INTERRUPTS
DSBL
STOP ON INTRPT
MODULE CLEAR
DISABLE
P-REG
CACHE
SPARE
BYPASS TEST
EXEC TEST
MODULE SELECT
IOC-0B
IOC-0A
IOC-1A
CPU-1
IOC-1B
CPU-0
D/CP
MENU SEL
0
1
2
3
CLEAR DSPL
MODE
4
5
6
7
DSPL
ADRS
8
9
A
B
STORE
DATA ENTRY
C
D
E
F
CONT
SPACE
←
→
+
-
HALT
CPU 0
STOP
ON
OFF
5
6
7
JUMP
1
2
3
BOOTSTRAP
AUTO RECOVERY
AUTO STAR
MANUAL
CPU 1
STOP
JUMP
11.00
19.8

5065-31-1

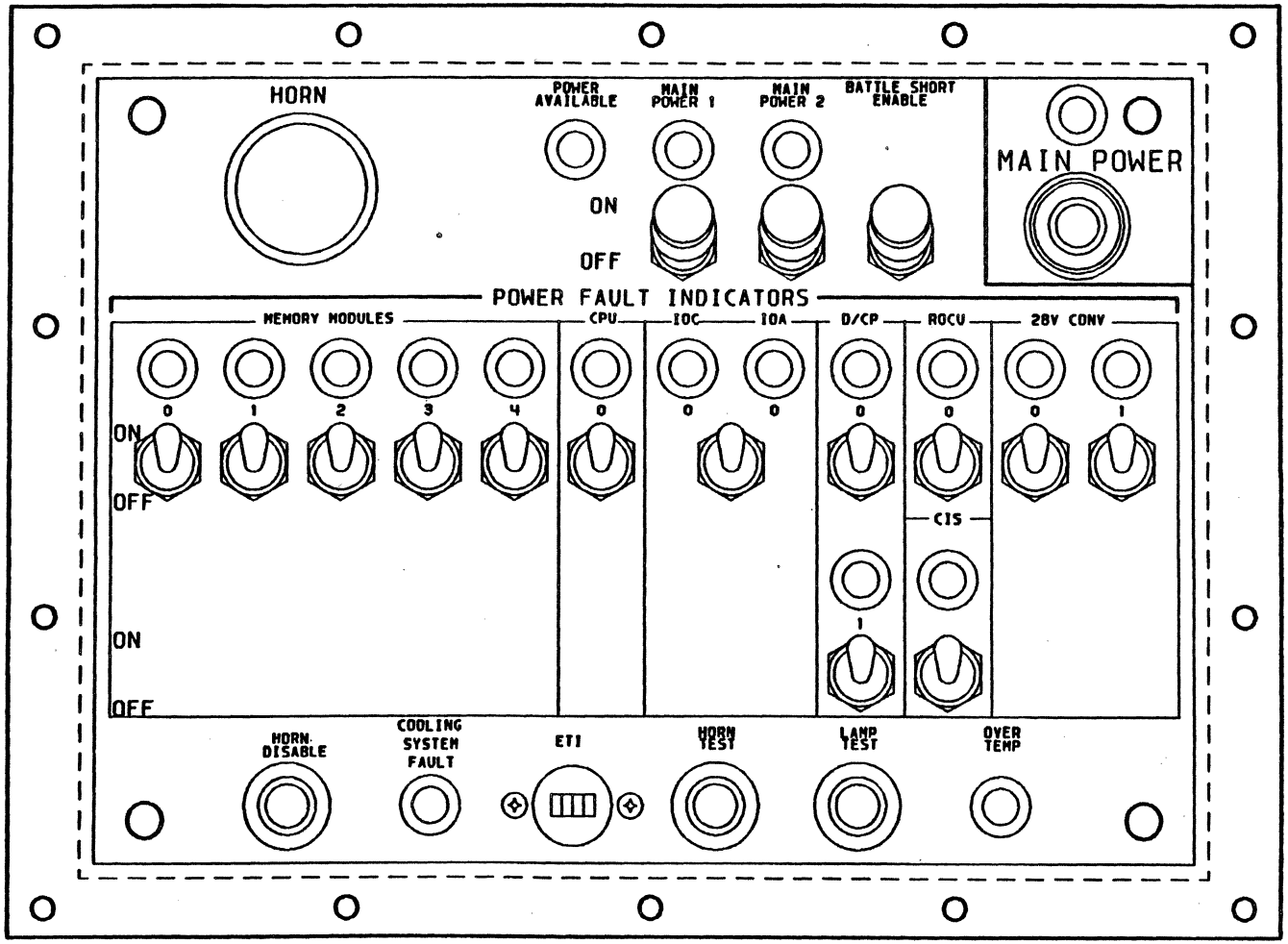
ROCU



IBM

5065-33

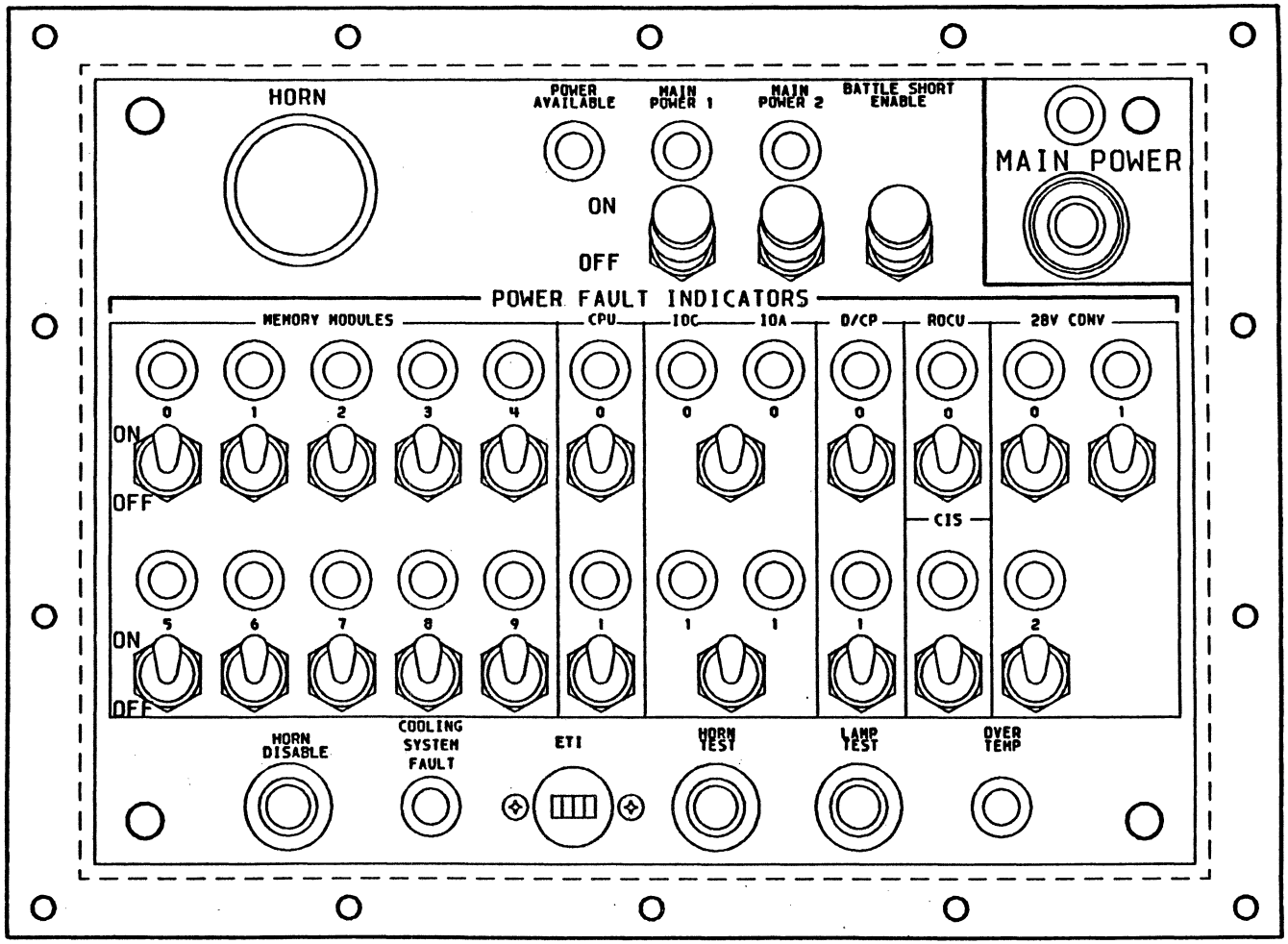
A ENCLOSURE PTP



IBM

5065-34

B ENCLOSURE PTP

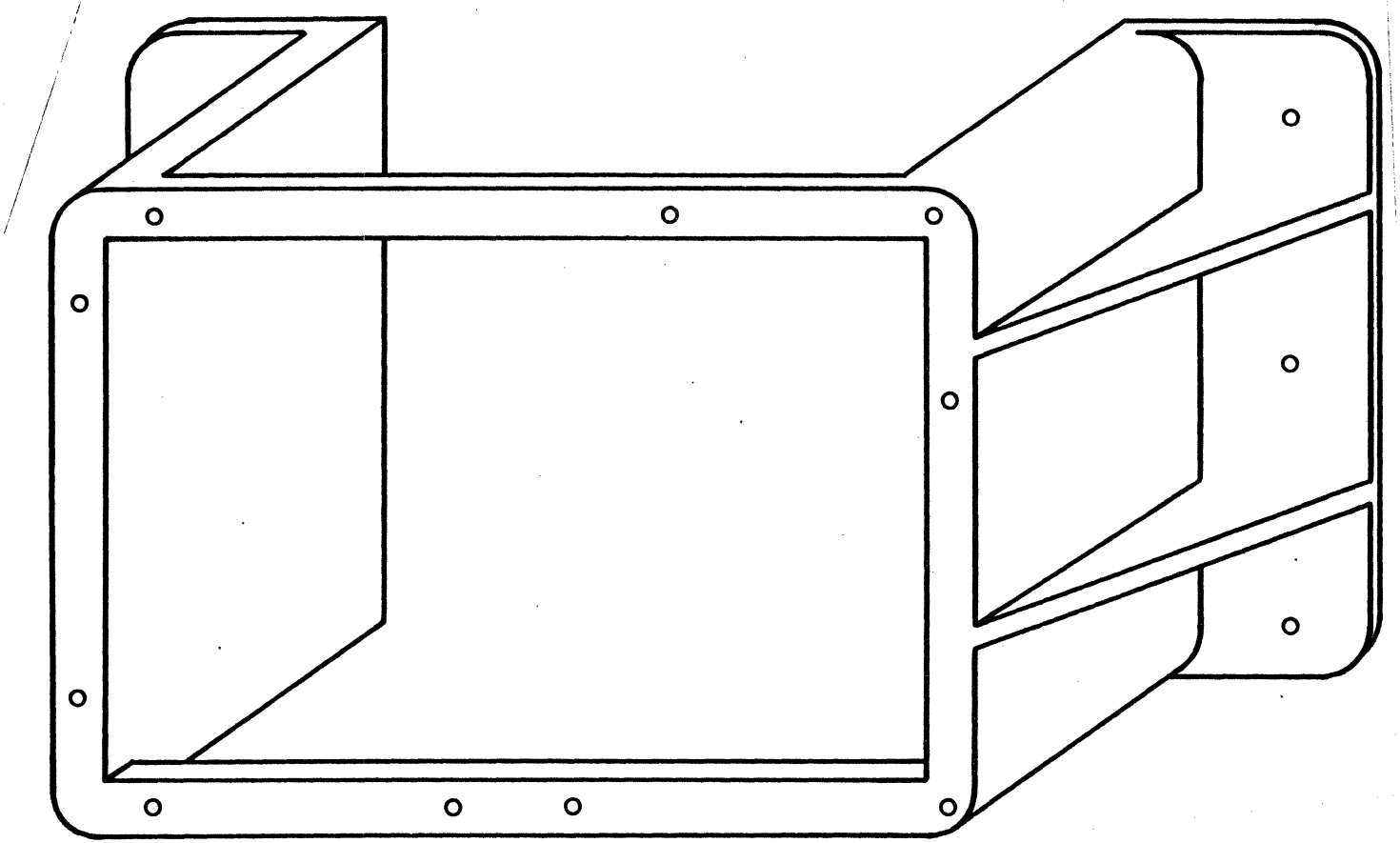


IBM

5065-35

ACTION ITEM

IBM MUST PROVIDE BULKHEAD MOUNTING OF D/CP



IBM

5065-36

ACTION ITEM

IBM to review the door interlock switch safety requirement.

DOOR INTERLOCK SWITCH SAFETY REQUIREMENT

- MIL-STD-454 REQMT 1

  Paragraph 5.8.a. No interlocks are required when all potentials in excess of 70 volts are completely protected with guards or barriers to prevent accidental contact under all conditions of operation or any level of maintenance.

- IBM will provide guards or barrier to prevent accidental contact under all conditions of operation or any level of maintenance on voltages greater than 70 volts.

IBM

5065-37

IBM to review possibility of front removal of backpanels.

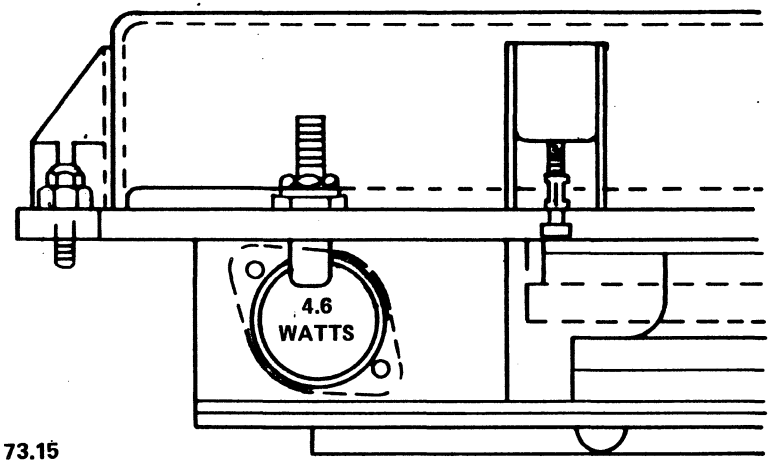
- For production the CPU backpanels will be made front removable. Presently no change anticipated for the EDM's.
- Due to the volume of cabling from the IOA and CIS there appears limited potential for front removal of these backpanels.
- On the EDM's there is accessibility to the backpanels thru the rear of the unit.
- There is access to the memory and IOC backpanels through a swing gate arrangement.

IBM

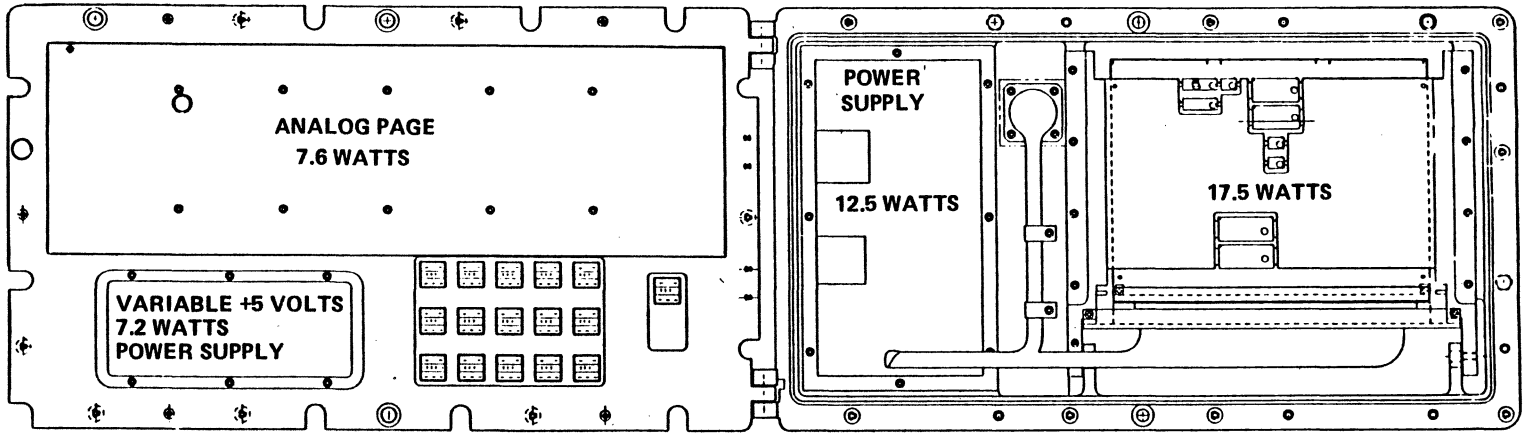
5065-38

D/CP POWER DISSIPATION

	POWER/WATTS
MP LRU	10.2
CP LRU	7.35
ANALOG PAGE	7.6
PLASMA PANEL	4.2
FRAME MOUNTED TRANSISTOR	4.6
FRONT PANEL LAMPS	19.5
POWER SUPPLY	12.5
VARIABLE POWER SUPPLY	7.2



73.15



FRONT FACE 23.7 WATTS LAMPS

SIDE & REAR SURFACE 49.3 WATTS OVER 446 IN^2

$Q = hA\ (\Delta T)$

$$49.3 \times 3.413 = 2 \times \frac{446}{144} \Delta T$$

$\Delta T = 15^{o}C$

STRUCTURE ANALYSIS

IBM

5065-61

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

OVERVIEW

- Requirements
- Design Goals
- Philosophy
- Procedures
- Results
  - Analytical
  - Empirical

IBM

5065-62

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

REQUIREMENTS

- Vibration: MIL-STD-167, Type I

Frequency Range (Hz)	Table Amplitude (inch)
4 to 15	0.030 ± .006
16 to 25	.020 ± .004
26 to 33	.010 ± .002

- Shock: MIL-S-901 HI
  Grade A, Class I, Type A, Mediumweight

- Structureborne Noise: MIL-STD-740
  Grade A, Type 3 (-20 dB)

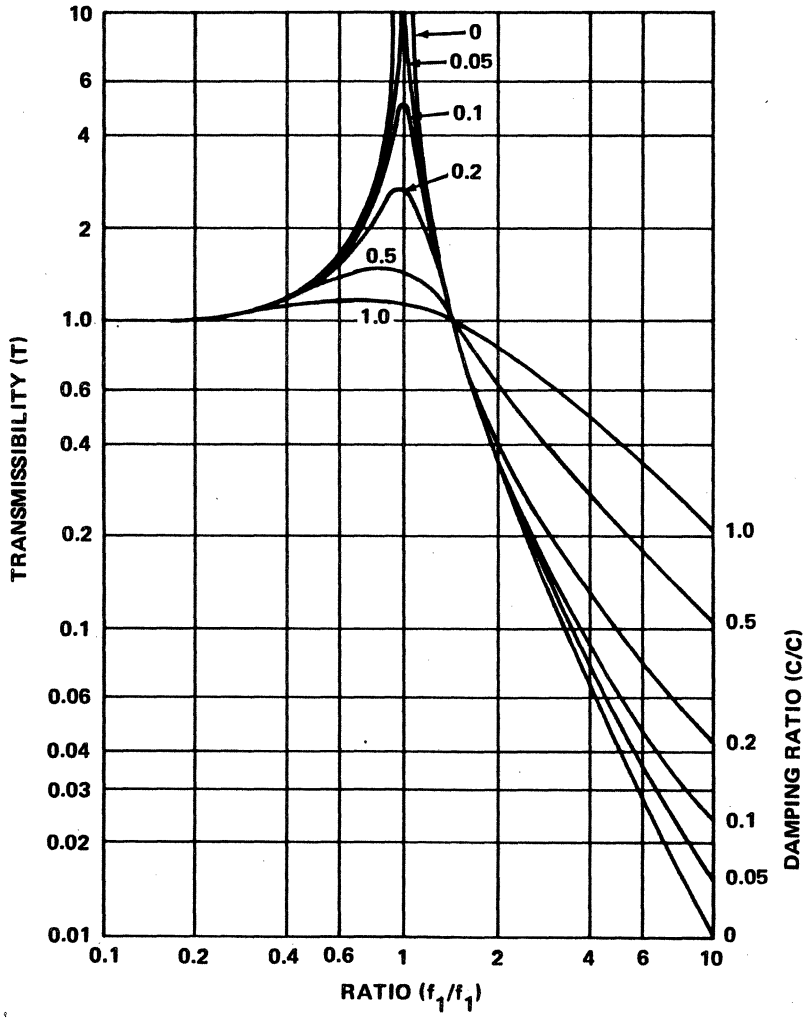
IBM

5065-63

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

DESIGN GOALS

- Vibration
  - Enclosure
    All $f_n \geq 40$ hz
  - LRUs
    $f_n \gg 40$ hz
    $(f_n)_{LRU} \neq (f_n)_{ENC}$
- Shock
  - Enclosure
    FEM analysis: $\sigma < \sigma_{ALL}$
  - LRUs
    MIL-S-901 lightweight testing

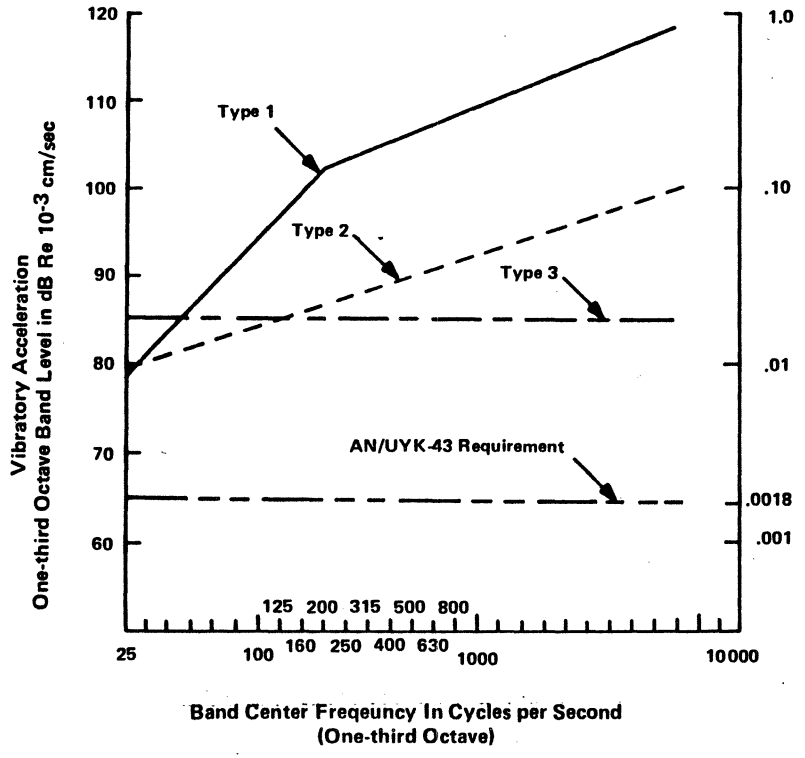


5065-64

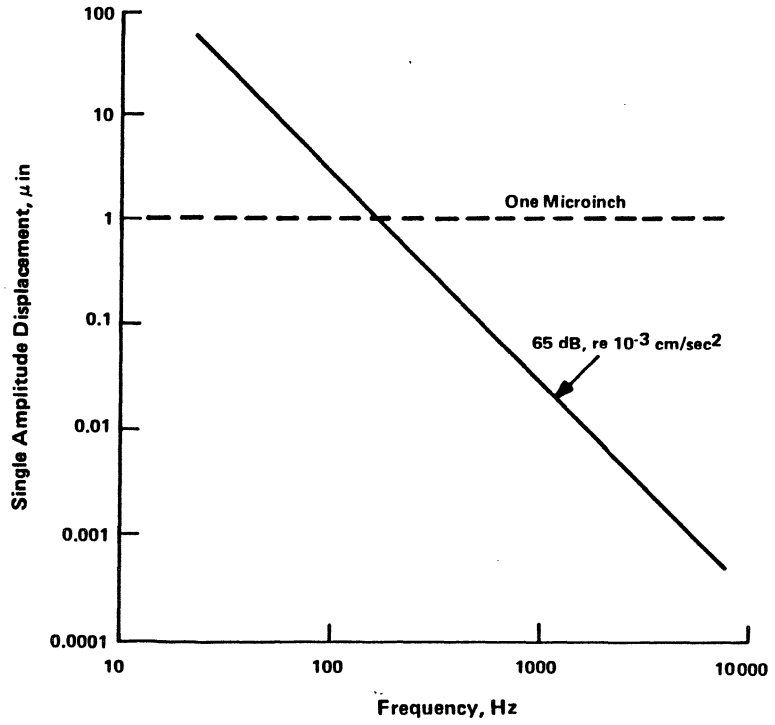
DESIGN GOALS – Continued

- Structureborne Noise

Acceleration Spectrum



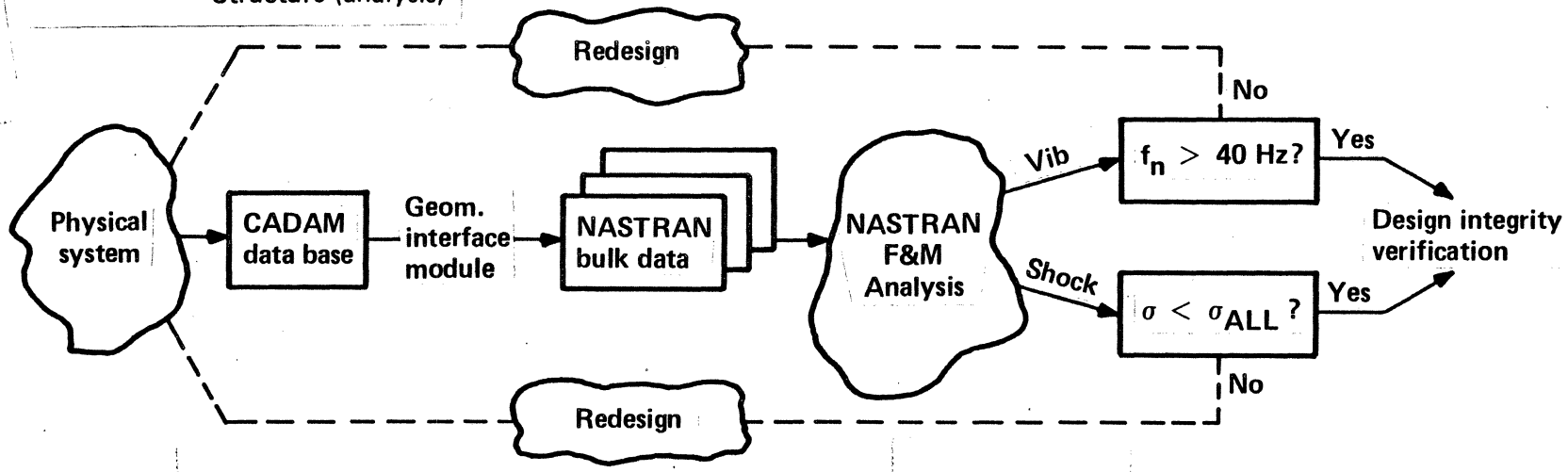
Displacement Spectrum



AN/UYK-43 DEVELOPMENT VIBRATION & SHOCK

PHILOSOPHY

- Vibration & Shock
  - Structure (analysis)



IBM

5065-65

AN/UYK-43 DEVELOPMENT
VIBRATION AND SHOCK

PHILOSOPHY

- Vibration & Shock – Continued
  - – Electronic Subassemblies (empirical)
    - – Vibration
      Similarity of design; comparison of requirements for other applications
    - – Shock
      MIL-S-901 lightweight compatibility

- Structureborne Noise
  Minimize S/B transmission from all potential sources
  (early & thorough treatment)
  - – Subassemblies
    - Supplier awareness
    - Consultation to vendors
  - – Structural design (enclosure & subassembly)
    - Minimize VIB susceptibility from disturbance
    - Attenuate levels from discrete sources

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

PROCEDURES

- Structure
  - — Vibration analysis

    Eigenvalue solution(s)
  - — Shock analysis
    - MIL-S-901 " equivalent" static analysis
      - -- 130 G, (vertical)
      - -- (113 G vert, 65 G horiz), inclined
    - Technique developed in early '70's
      - -- Utilized on AN/BQQ-5, AN/BQQ-6, TAC MK-105, STM TACTAS/SURTAS, LAMPS, etc.
      - -- Technique correlated with NUSC mediumweight test characterization data
      - -- Analytical results correlated with unit test data
- Electronic Subassemblies
  - — Vibration

    Comparison of dynamic characterization data to spec requirements, enclosure analysis
  - — Shock

    Mil-S-901 lightweight testing

IBM

5065-66

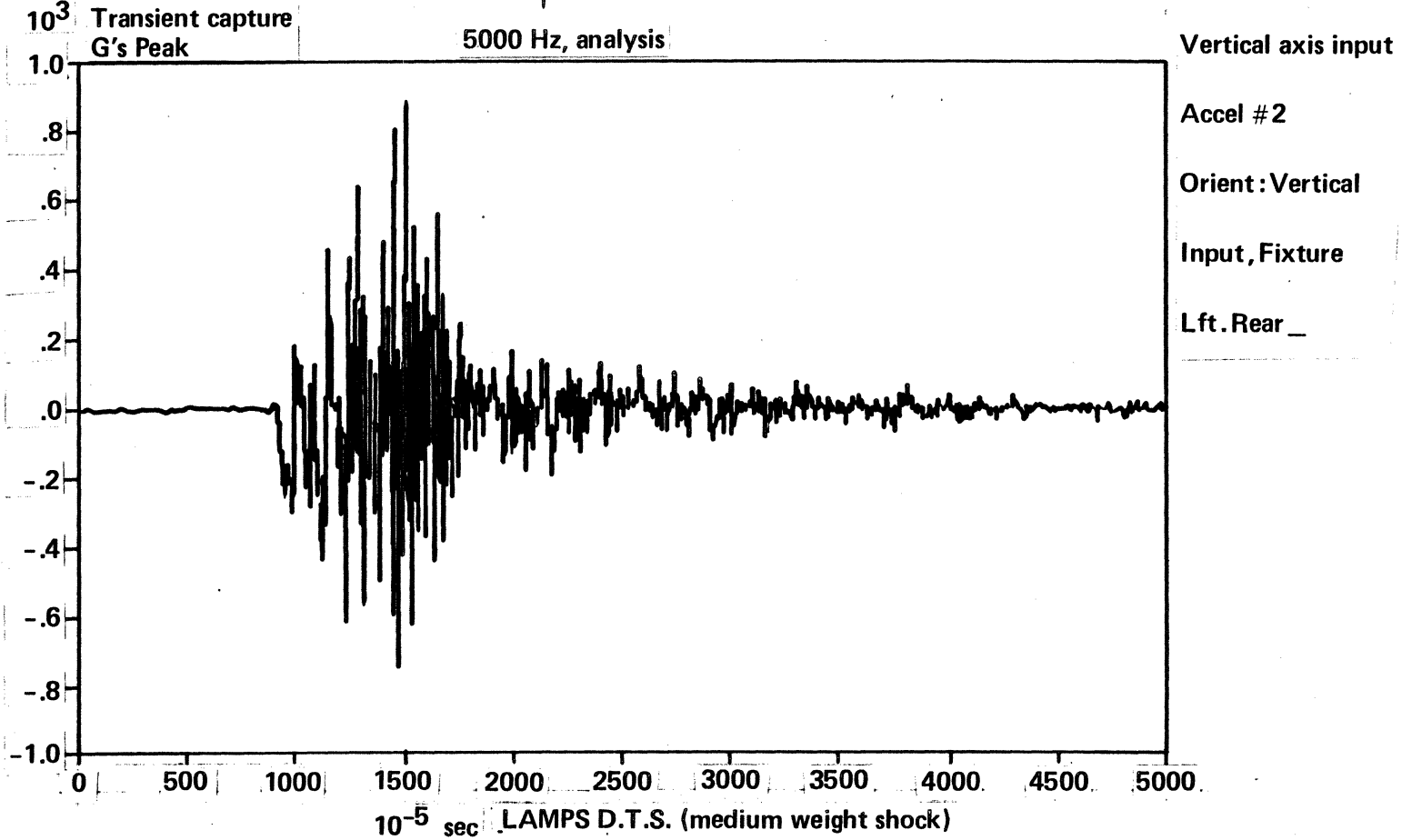
AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

PROCEDURES – Continued

- Structureborne Noise
  - – Discrete sources
    - Mechanical (fans)
      - -- Alternate bearing selection
      - -- Effect of RPM reduction
      - -- Balancing techniques
    - Electrical (transformers, RFI filters, line inductors, inverters, etc.)
      - -- Internal damping
  - – Structural design and packaging techniques
    - Stiffness of items exposed to airstream
      - -- Air plenum construction
      - -- General structural stiffness
      - -- Interfaces
    - Discrete source mounting
      - -- Differential stiffness
      - -- Mechanical isolation

PROCEDURES (CONTINUED)

9/16/80 —— ship board rack ---+--- Blow 2 -- —— (footage – 150)



IBM

5065-67

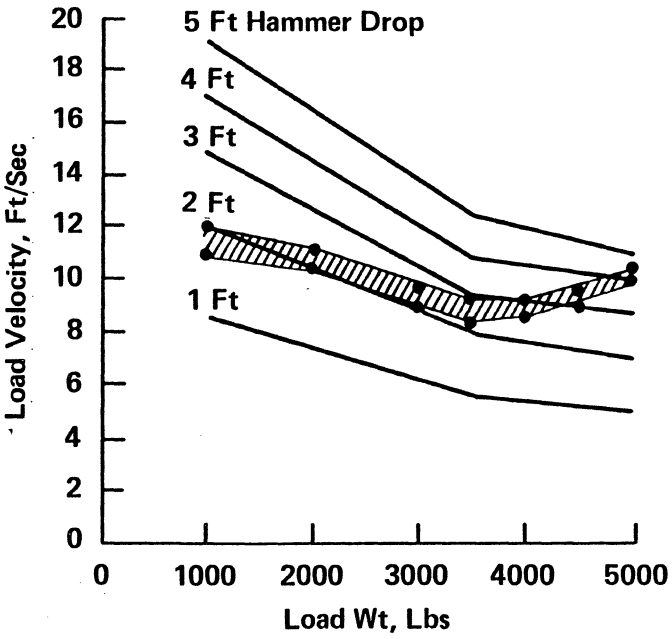
PROCEDURES (CONT'D)

MIL-S-901C(NAVY)

Table I - Test schedule for medium weight shock machine.

Group number----------	I	II	III
Number of blows----------	2	2	2
Anvil table travel, inches------	3	3	1-1/2
Total weight on anvil table, [1] (Pounds)	Height of hammer drop [2] (Feet)		
250 – 1,000	0.75	1.75	1.75
1,000 – 2,000	1.0	2.0	2.0
2,000 – 3,000	1.25	2.25	2.25
3,000 – 3,500	1.5	2.5	2.5
3,500 – 4,000	1.75	2.75	2.75
4,000 – 4,200	2.0	3.0	3.0
4,200 – 4,400	2.0	3.25	3.25
4,400 – 4,600	2.0	3.5	3.5
4,600 – 4,800	2.25	3.75	3.75
4,800 – 5,000	2.25	4.0	4.0
5,000 – 5,200	2.5	4.5	4.5
5,200 – 5,400	2.5	5.0	5.0
5,400 – 5,600	2.5	5.5	5.5
5,600 – 6,200	2.75	5.5	5.5
6,200 – 6,800	3.00	5.5	5.5
6,800 – 7,400	3.25	5.5	5.5

[1] Total weight on anvil table is the sum of equipment weight plus weight of mounting.
[2] The height of hammer drop shall be measured by means of the existing markings on the scale of the machine, no corrections being made for the added anvil table travel for the blows of groups I and II.

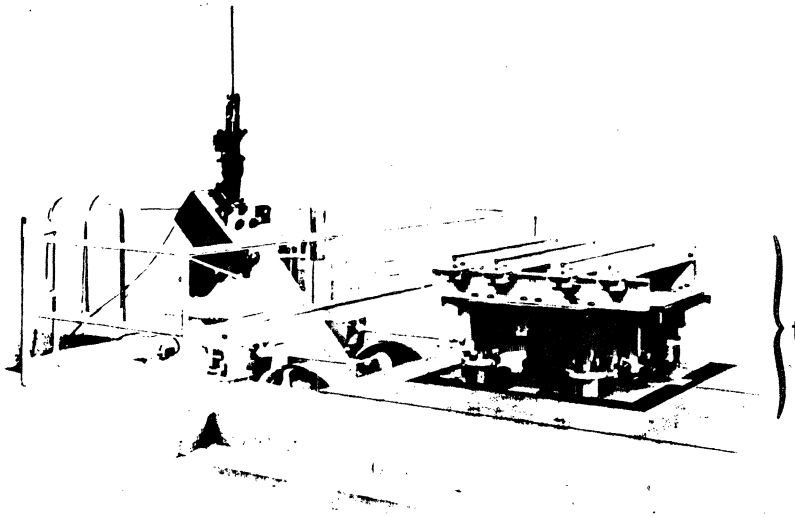


NRL Report 5618 (AD 260008)
"Navy High Impact Shock Machines for Light Weight & Medium Weight Equipment"
I. Vigness, U.S. Naval Research Laboraotry
June 1, 1961

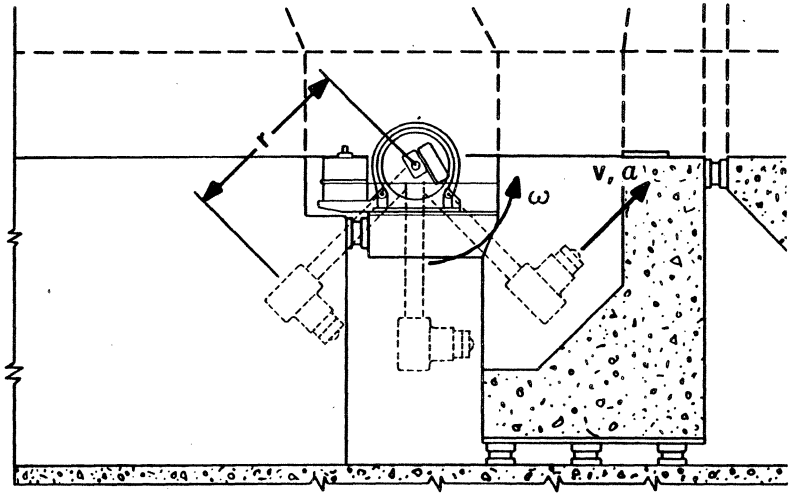
Conclusion: 10 ft/sec (120 in/sec) constant velocity vector is an accurate representation of the effect of MIL-S-901 medium weight hammer test

AN/UYK-43 DEVELOPMENT VIBRATION & SHOCK

PROCEDURES (CONT'D)



f = 65 to 70 Hz



- $a = \frac{v^2}{r}$

  $(v = r\omega;\ \omega = \frac{v}{r})$

- $a\ v\omega$

  $(\omega = 2\pi f)$

- $a = 2\pi fv$

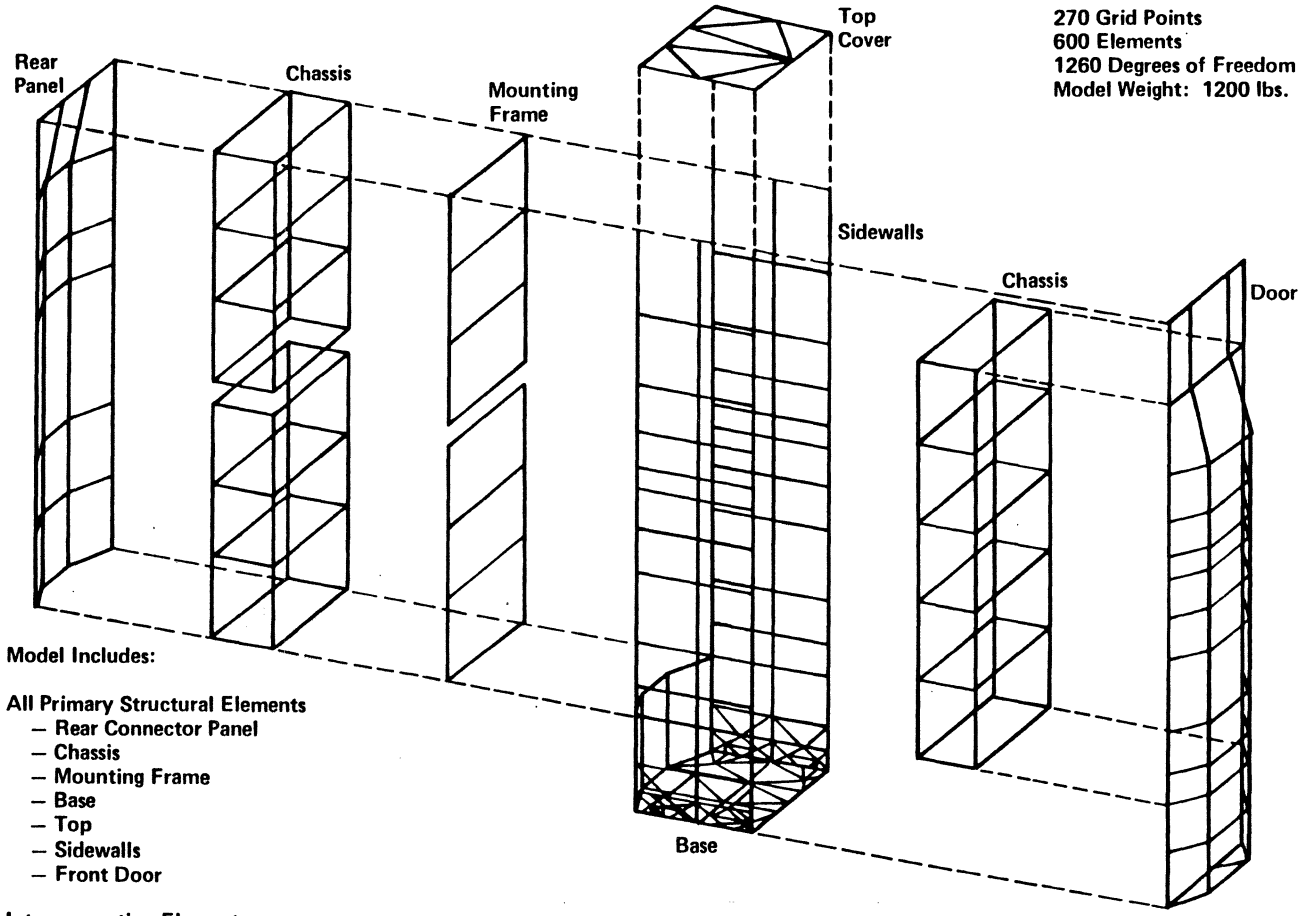
- $G = \frac{2\pi fv}{g}$

G = 130g = Static acceleration @ 67 Hz equivalent to a 120 in/sec velocity vector.

IBM

5065-70

AN/UYK-43 B CABINET FINITE ELEMENT MODEL



270 Grid Points
600 Elements
1260 Degrees of Freedom
Model Weight: 1200 lbs.

Model Includes:

All Primary Structural Elements
- Rear Connector Panel
- Chassis
- Mounting Frame
- Base
- Top
- Sidewalls
- Front Door

Interconnection Elements
- Bolts
- Hinges
- Latches
- Pins

IBM

5065-71

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

ANALYSIS VS TEST COMPARISON

Application	Date	Program	Equipment	Install Condition	Mode	Dynamic Response, f_n (Hz) Analytical Prediction	Test Result
Shipboard	1976	Proteus STM	TACTAS/SURTAS	Hard Mt	S-S/1	70	69
				Hard Deck	S-S/2	125	124
				Base and Top Stab.	S-S3	146	146
					F-R	124	122
					V	—	—
				Hard Mt	S-S	30	31
				Hard Deck	F-R	120	118
				Base Mt Only	V	—	—
Avionics	1977	LAMPS	Mission	Hard Mt	S-S	25	23
			Avionics Rack	Base Only	F+R	42	38
					V	51	55

B CABINET STRUCTURAL ANALYSIS RESULTS

- Vibration
  - Front to rear: 42 Hz
  - Side to side: 50 Hz
  - Vertical: >100 Hz
  - All/$\sigma < \sigma_{END}$ (T_r = 3 assumed)
- Shock

	Minimum Margin of Safety*		
	Vertical	Inclined Front-rear	Inclined Side
Primary structural elements			
Sidewalls	>5	1.69	4.39
Base	>5	>5	>5
Rear panel	>5	.30	.65
Mounting frame	>5	1.18	3.50
Chassis	>5	1.76	.70
Front door	>5	>5	.59
Interconnection elements			
Chassis bolts	>5	.27	.36
Hinges	3.47	0.47	.29
Latches	4.06	.20	.95
Pins	>5	.68	.53
Welds	>5	1.73	.40
Mounting bolts	2.65	.26	.73

*M.S. calculations based upon ultimate material strength

AN/UYK-43 DEVELOPMENT
VIBRATION AND SHOCK

A CABINET STRUCTURAL ANALYSIS RESULTS

- Vibration
  - Front to rear: 53 Hz
  - Side to side: 74 Hz
  - Vertical: >100 Hz
  - $\sigma \ll \sigma_{END}$
- Shock

  Based upon structural design similarities to "B" enclosure and reduced mass
  - All stresses are within allowable material limits
  - "A" structure M.S. > "B" structure M.S.

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

RESULTS – Continued

- Electronic Subassemblies

  – Vibration Comparison

Subassembly Configuration	Forcing Frequency Range (MIL-STD-167)	Cabinet Resonances, Side to Side A	Cabinet Resonances, Side to Side B	Subassembly Resonances (Normal to the Plane of the Subassembly)
Regulator	4-33 Hz	74 Hz	50 Hz	170 Hz
Converter	4-33 Hz	74 Hz	50 Hz	220 Hz
Hi Density Logic Page	4-33 Hz	74 Hz	50 Hz	310 Hz
Lo Density Logic Page	4-33 Hz	74 Hz	50 Hz	150 Hz
QMCM Memory Page	4-33 Hz	74 Hz	50 Hz	325 Hz

  – Vibration History: B-52 G/H OAS Processor Qualification

Subassembly	Unit Qual Vibration Test Level Freq. (Hz)	Level	Test Duration
Regulator, Converter, Hi Density Logic, Lo Density Logic, QMCM Memory	10-25	.0015 G^2/Hz	33 Hrs. Total:
	25-158	+6 dB/oct	11 Hrs./Axis,
	158-400	.06 G^2/Hz	7.5 Hrs. @ Room. Temp.
	400-800	-6 dB/oct	1.75 Hrs. @ -54°C
	800-1200	.015 G^2/Hz	1.75 Hrs. @ +71°C
	1200-2000	-6 dB/oct	
	(6.5 G_{rms} overall)		

  – Lightweight Hammer Drop Shock Test

Subassembly	Test(s)	Post Test Inspection Visual	Post Test Inspection Functional
Converter	Top, Edge & Back Blows @ 1, 3, & 5 ft. Hammer Height	No Damage	–
Hi Density Logic		No Damage	–
Lo Density Logic		No Damage	–
QMCM		No Damage	O.K.
D/C Plasma Panel		No Damage	–

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

RESULTS – Continued

- Structureborne Noise
  - Discrete sources
    - Fans
      - -- Inverter design capable of automated fan RPM reduction, if required
    - Power system
      - -- AN/UYK-43 design switching frequency ~ 50 KHz
      - -- Switching frequency >> upper limit of requirement
  - Structure and packaging
    - Structural excitation minimized
      - -- Rigid structure, subassemblies
      - -- Rigid interfaces
    - Damping of fan plenums easily incorporated if needed
    - Fan isolation preliminary studies encouraging
      - -- At least 20 dB reduction attainable if required
  - Experience
    - Requirement met for AN/BQQ-6 standard hardware cabinet

AN/UYK-43 DEVELOPMENT
VIBRATION & SHOCK

SUMMARY OF CONCLUSIONS

DESIGN DYNAMIC INTEGRITY VERIFIED

- Vibration
  - Enclosure(s)
    - $f_n \gg 33$ Hz
    - $\sigma < \sigma_{END}$
  - LRUs
    - $f_n \geqq 150$ Hz
    - OP integrity demonstrated through 33 hrs @ 6.5 g_{rms}
- Shock
  - Enclosure(s)
    - For all primary structure and interconnections
      - -- $\sigma < \sigma_{ULT}$
      - -- $\sigma \leqq \sigma_{YIELD}$
  - LRUs
    - Lightweight hammer drop test confirmation
- Structure borne Noise
  - High confidence in compliance through design considerations & test experience
  - Alternate approaches established if needed

SDEX/COMMON PROGRAM

SDEX/COMMON PROGRAM

- Requirements/Limitations
- Functions and Storage Allocation
- Development Approach
- Interface
- Changes to Software
- Program Control
- Schedule
- Deliverable Items

EXECUTIVE/COMMON PROGRAM REQUIREMENTS

1. Support IBM UYK-43 Casualty Reaction System
   - FTRM
   - OTP
2. Use Share/7 System for Development
   - Compile
   - Assemble
   - Generate load tapes
3. Submit ECP's for all Functional Changes

DESIGN GOALS AND LIMITATIONS

Limit modifications to those necessary to demonstrate OTP and FTRM

- Run in UYK-43 Mode (Executive and Tasks)
- Support 2 CPU's
- Support 2 IOC's
- No Inter-Computer Messages
- Devices Supported – DEAC

ESTIMATED STORAGE ALLOCATION (32-BIT WORDS)

	A - Enclosure: 1 CPU, 1 IOC		B-Enclosure: 2 CPU, 2 IOC	
	UYK-7	UYK-43	UYK-7	UYK-43
SDEX	5.3 K	6.1 K	6.3 K	7.2 K
Common Systems (Without math routines)	3.2 K	3.6 K	3.8 K	4.2 K
Common Peripheral (DEAC support only)	6.8 K	7.8 K	6.8 K	7.8 K
Debug	3.8 K	4.3 K	3.8 K	4.3 K
Dynamic Modular Replacement	2.1 K	2.2 K	2.2 K	2.3 K
Total	21.2 K	24.0 K	22.9 K	25.8 K

SOFTWARE DEVELOPMENT APPROACH

1. Use Share/7 to generate an unmodified SDEX-7/CP to run on UYK-7

   - Gain Share/7 experience
   - Study SDEX/CP internals on operational UYK-7
   - Use for FTRM and OTP development on UYK-7

2. Run unmodified system above on UYK-43 in UYK-7 mode

   - Establish UYK-43 SDEX/CP Software Baseline
   - Test UYK-43 hardware and firmware in 7 mode

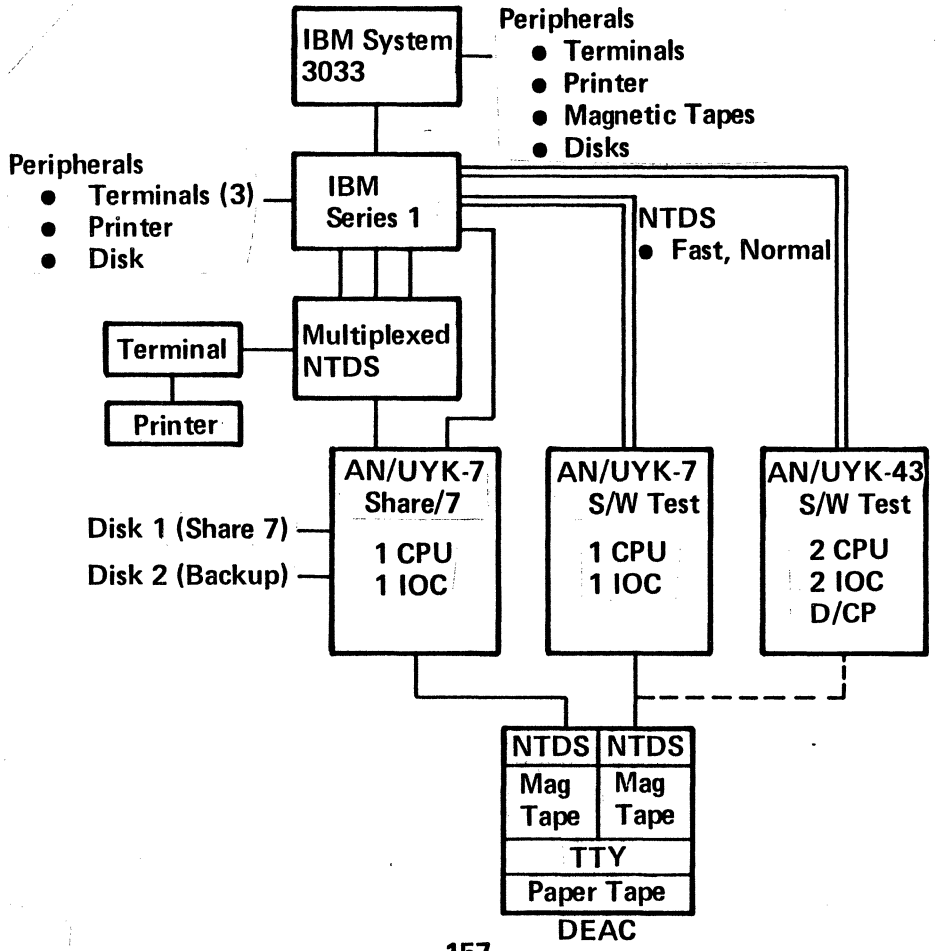
3. Test and release UYK-43 SDEX/CP for A-Enclosure

   - Test UYK-43 hardware and firmware in 43 mode
   - Use for FTRM and OTP development on UYK-43

4. Test and Release UYK-43 SDEX/CP for B-Enclosure

   - Demonstrate Casualty Reaction

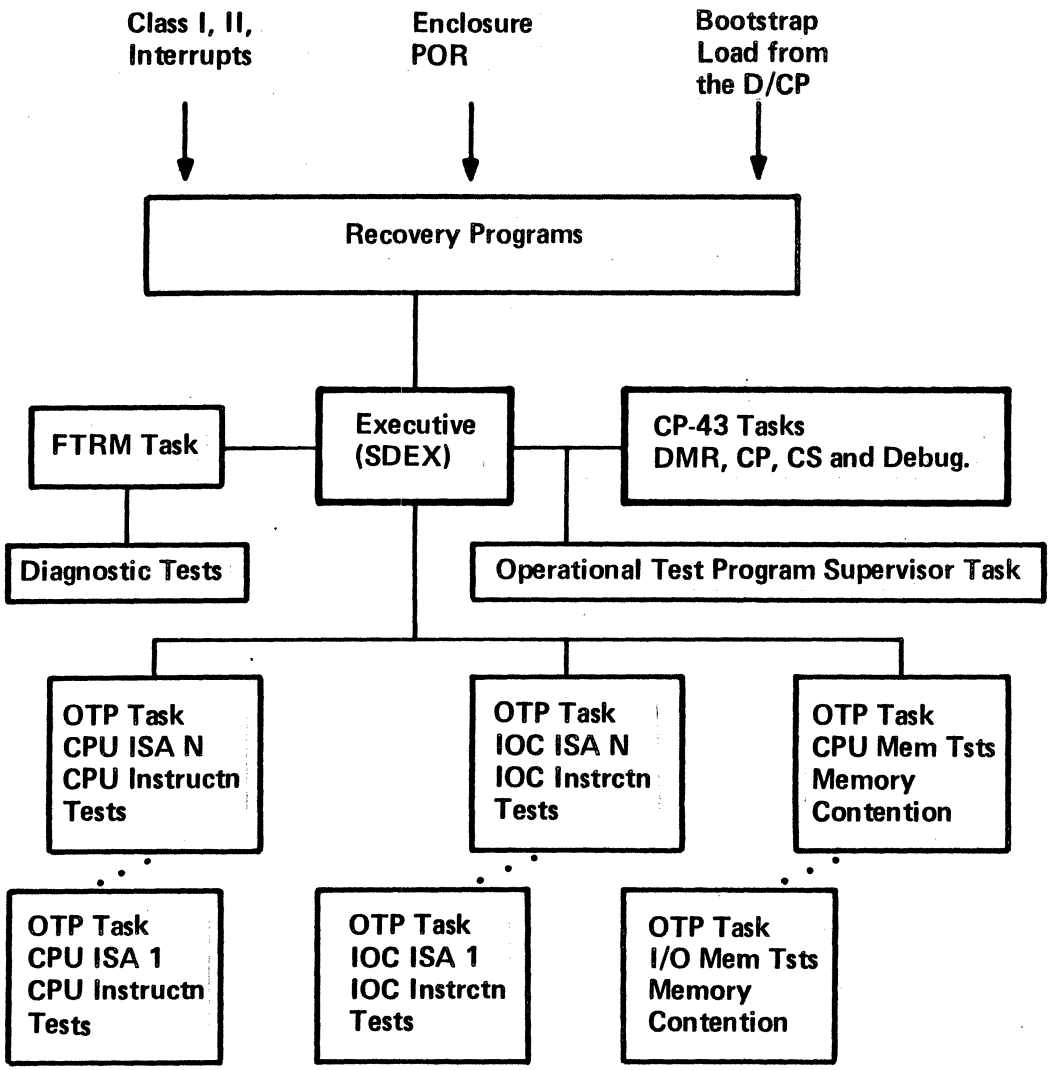
AN/UYK-43 DEVELOPMENT LAB



IBM

5065-364

EXECUTIVE AND COMMON PROGRAM INTERFACE



CHANGES BASED ON ARCHITECTURE

Module \ Architectural Change	Address expansion to 32 bits	IOC controls 32 channels	CP/IOC Monitor Clocks 32 Bits	New and Modified Interrupts	Modified Interrupt Status Codes	Status Via New Instructions	Access ASR via CMR 70	Four Sets of Exec State Registers	IOC Base Regs - CAR, CAP, Buffer	IOC Memory Protection	Breakpoint Extensions	Stack Registers
SDEX-7	X	X	X	X	X	X	X	X		X	X	X
Common Systems	X											
Common Peripheral	X	X							X	X		
Dynamic Modular Replacement	X			X	X		X	X	X	X		
Debug	X					X			X			

CHANGES BASED ON CASUALTY REACTION

SDEX/7

- Expand Error Packet
  P-History, Real Time Clock, I/O Registers

Common Systems

- Remove Alternate Recovery Routines
- Move Memory and IOC Confidence Testing to FTRM
- Add Vital Data Checkpoint Services

Common Peripheral

- Flag Unrecoverable Device Errors in System Resource Table

MODIFICATIONS TO SDEX (EXECUTIVE)

	PPS Reference
Modify for 32-Bit Addresses, 5-Bit Channel Numbers, Etc.	
• Tables	3.2.4.2 & Fig. 3-1
• ESRs	Table 3-1
Class I, II, III, IV Interrupts	3.3.3.2
• New Interrupts and Status (CMR, ASR, ISC)	Table 3-2
• Use Four Sets of Interrupt State Registers	
• Save Stack Registers	3.3.2.4.4.1
• Process Breakpoint Register Interrupts	3.3.3.2.2
Expand Error Packet	3.3.5.2
• P-History	
• Real Time Clock	
• I/O Registers - CAR, CAP	
IOC Monitor Clock – 32 Bits	N/A
CP Monitor Clock – 32 Bits	N/A
I/O Storage Protection	Table 3-1.14

CHANGES TO SDEX/7 TABLES

REFERENCE: User's Reference Manual 15 Feb. 1980

		Table Number:
Segment Allocation Packet (SAP)	32 Bit Base Address	3-3
Task List (CCTASL)	32 Bit Base Address	C-1
SAP Linkage Table (CCLINK)	32-Bit Base Address	C-3
I/O Channel Assignment (CCICAT)	Increase Table Size for 32 Channels Per IOC	C-10
Entry Assoc. with CPU Data Table (CCDAT)	32 Bit Abs. Address	C-13
Message Processing List (CCMEST)	32 Bit Abs. Address	C-16
Error Packet Storage Table (CCERRPKT)	Include Additional Data	C-17

CHANGES TO SDEX/7 ESRS

REFERENCE: User's Reference Manual 15 Feb. 1980

		ESR Numbers
I/O Interrupt Registration/Changes	Alter Packet 5 Bits for Channel Storage Protection Data	111, 112, 113
Enable/Disable Interrupts	5 Bits for Channel	302, 303
Enter Module on Task List	32 Bit Abs. Address	401
Breakpoint	Support Debug	405, 406, 413, 414, 415

MODIFICATIONS TO COMMON SYSTEM

	PPS Reference
Modify for 32-Bit Addresses, 5-Bit Channel Numbers, Etc. • Tables • Messages	
Add Vital Data Update/Fetch for Restart/Reload	3.4.1
Move Memory and IOC Confidence Testing to FTRM	1.3.2.4 3.4.4.1
Move Alternate Recovery Memory Routines to FTRM	1.3.2.5 3.3 3.3.5 3.3.5.6 3.4.5

MODIFICATIONS TO COMMON PERIPHERAL

	PPS Reference
Modify for 32-Bit Addresses, 4-Bit Channel Number, Etc. • Table • ESR Data • Messages	
IOC Storage Protection	New
IOC Base Registers – CAR, CAP, Buffer	New
Devices Supported – DEAC	3.3.1

MODIFICATIONS TO DYNAMIC MODULAR REPLACEMENT

	PPS Reference
1. Modify for Expanded Addressing and I/O	
• New SAP Format and Size	3.4.1.2.a
• I/O Base Registers and Storage Protection	3.4.2.2
2. Move Casualty Processing Function to FTRM	1.3.2.3 3.2.1.c
• FTRM will Use DMR Services	3.4.3 3.3.5.3
3. Send Preset Initialization Message to FTRM	3.4.1.2.f

MODIFICATIONS TO DEBUG

Modify to Support Lab Software Checkout As Necessary

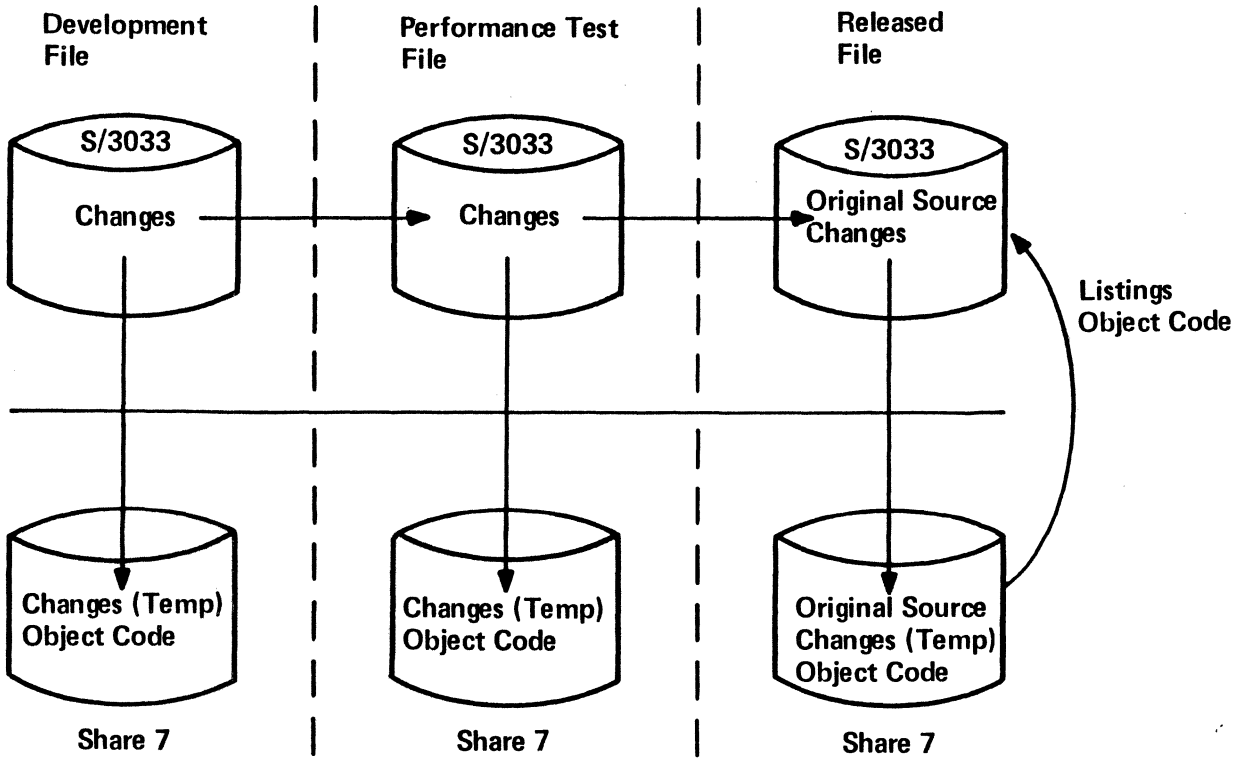
Functions Being Assessed:	PPS Reference
Change Words	3.4.5
Immediate Memory Dump	3.4.9
Snap Dump	3.4.6.2
Intermodule Message Transfer	3.4.12

I/O STORAGE PROTECTION

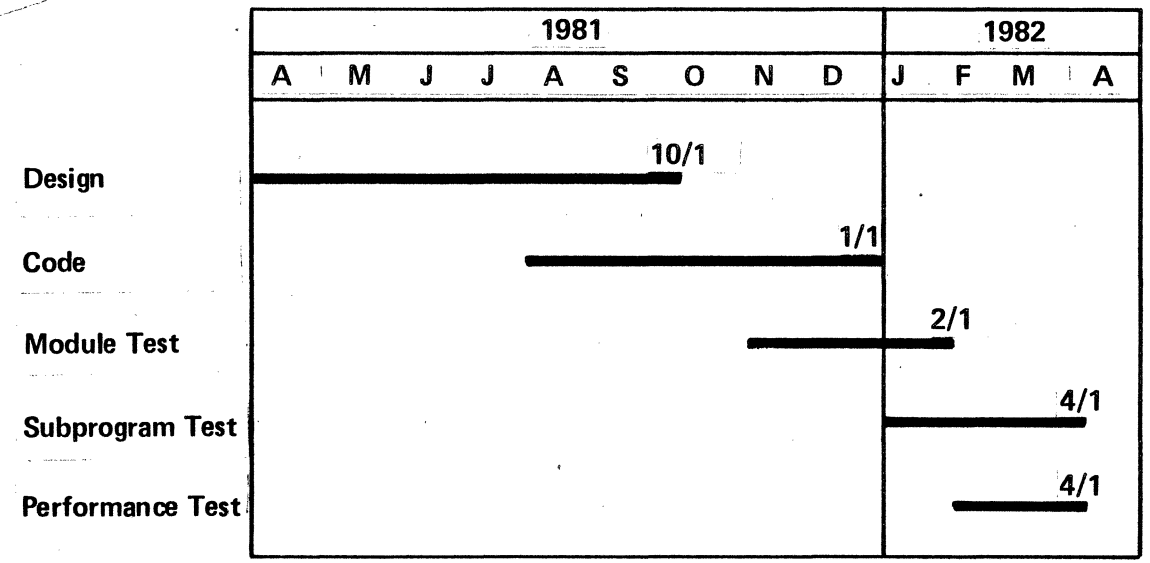
Design Objectives and Approach

1. Protect Program Segments from Being Destroyed by Another Segment's I/O.
   - Define min and max buffer address limits for each segment in the SAP table at system generation time.
   - Limits for Common Program segments may be set wide open for using Debug functions and loading programs.
2. Protect Each Segment from Destroying Itself By It's Own I/O.
   - At I/O Registration time permit a segment to "Fine Tune" its own storage protection limits.

PROGRAM DEVELOPMENT AND MANAGEMENT SYSTEM



SDEX/CP Schedule



DELIVERABLE ITEMS

Software

- Source Code on Magnetic Tape
- Object Code on Magnetic Tape
- Assembler Output Listing (SDEX, CS, DMR, Debug)
- Compiler Output Listing (Common Peripheral)

Documentation

- ECP's for all Functional Chanages
- Changes to Source Code – Share 7 Correction File

NDRO PROGRAMS

OBJECTIVES FOR AN/UYK-43 INITIALIZATION

- Automatic, Fault-Tolerant Recovery from Power Transients
- Automatic, Fault-Tolerant Diagnostic Load and Simple, Accurate Load-Final Analysis
- Single NDRO Part Number
  - Exclusive of User-Specified Code
  - User-Code Segregated with Respect to Both Physical Devices and Linkage
- Equivalent Operator Control Capability to AN/UYK-7
- Accommodate Various Initialization Environments

INITIALIZATION ENVIRONMENTS

	AN/UYK-43 With FTRM	Without FTRM	AN/UYK-7
Power Transient Recovery	√	√	√
Operational IPL	√	√	√
On-Line Repair	√	NA	NA
Off-Line Repair	√	√	√
Laboratory IPL	√	√	√

AN/UYK-7 ENVIRONMENT

- Existing NDRO Function
  - Recovery
  - Interrupt Switcher
  - Entries
- Existing Memory Allocation
  - No Reserved Areas Assumed
- Existing Load Records
  - No Assumptions About First Load Record
  - Only Diagnostic Records Modified
- AN/UYK-43 Unique Initialization Must Precede 7 Code NDRO/DRO

SINGLE NDRO PART NUMBER – OBSTACLES

- User-Specified Code
- Alternatives to FTRM
  – Existing 7 Environment/Code
  –43 Without FTRM (User Recovery)
- Multiple Peripherals
- Multiple Channels
- Multiple Boot Programs
- Multiple Entries

SINGLE NDRO PART NUMBER – APPROACH

- User-Specified Code – Segregate
  – Eliminate Need
- Alternatives to FTRM – Accommodate with Option Prom Switch
- Multiple Peripherals – Index into Table Per Option Prom
- Multiple Channels – Option Prom
- Multiple Boot Programs – Eliminate
- Multiple Entries – ? Equivalent Function

OPTIONS PROM

- Single Field-Replaceable Component
- PROM Contains All Essential Default Values of User-Specified Initial System Parameters
- All Values Derived from the PROM May Subsequently Be Overridden by Software and/or D/CP
- Bootstrap Parameters
  - -7/-43 Bootstrap
  - IOC Load Device & Loader Channel
  - Absolute Addresses of FTRM Pointers
  - CIS Initial ID
- Ordering Options
  - Memory Module Priorities
  - IOC Channel Mode (Normal, ESA, ESI, IC)
  - CIS Lengths
  - REI & DMI Priorities
  - RTC Granularity

POWER TRANSIENT RECOVERY

- With Multiple NDRO Part Numbers Total Flexibility for Recovery or Reboot Using NDRO or DRO
- With a Single NDRO Part Number
  - Provide for Automatic, Fault-Tolerant Recovery in Concert with FTRM (43 with FTRM)
  - And Permit Alternatives Through NDRO 777 (As in AN/UYK-7) or Option Prom Defined Address (43 without FTRM)

OPERATIONAL IPL/BOOT

- Invoked Manually (Master Clear/Smart), by Software, or Automatically
- With Single NDRO Part Number Automatically Invoked if Automatic Power Transient Recovery Fails
- May be Invoked by Recovery Software
  - FTRM
  - User-Specified NDRO/DRO
- In AN/UYK-7 Environment (Per Option PROM), Automatically Invoked if "Nested Interrupts"* Occur and Autorecovery = Auto
- In AN/UYK-43 with FTRM, Automatically Invoked if, when Requiring Casualty Reaction, No Valid FTRM Can be Found

*Illegal Instruction while in Interrupt Mode

OPERATIONAL IPL/BOOT - Continued

- Boot Program Entries Are
  NDRO 1, 2, 3, 4097, 4098, 4099
- Selection of Boot Program may be Determined by the Boot Switch and by the State of ASR31 (7/43 Exec)
- In AN/UYK-43 Automatic IPL/Boot is Performed Under IOC Control with Incorporated Fault-Tolerance and Automatic Load-Fail Analysis

ON-LINE REPAIR

- To Accommodate On-Line Repair Individual FHM's may be Powered Off/On
- Individual Module Power-On Resets are Distinguished from Enclosure Resets; the Module is Reset and Stopped to Await Restart by FTRM

OFF-LINE REPAIR

- A Single, Pervasive Environment
  - Diagnostics Constitute the Total Box Function
  - Diagnostics Own All of Memory
  - Diagnostic Load Record is Used
- The Entire Diagnostic Process is Automatic (Master Clear/Start; Auto Rec = Manual)
- IOC Controls Boot – Greatly Reducing Hardcore
  - IOC is Central to Boot and Smarter than the AN/UYK-7 IOC
  - IOC is Simpler than the CPU and Incorporates some Redundancy
- Load-Fail Analysis is Further Improved By:
  - Processor Cross Monitoring
  - Multi-Path Communication: Control Bus & Memory
  - Known Sum-Check of First Record
  - 4,000 Lines of CPU NDRO for IOC/Load Path Diagnostics
- In B Enclosure Second IOC will Attempt Boot if First IOC Fails

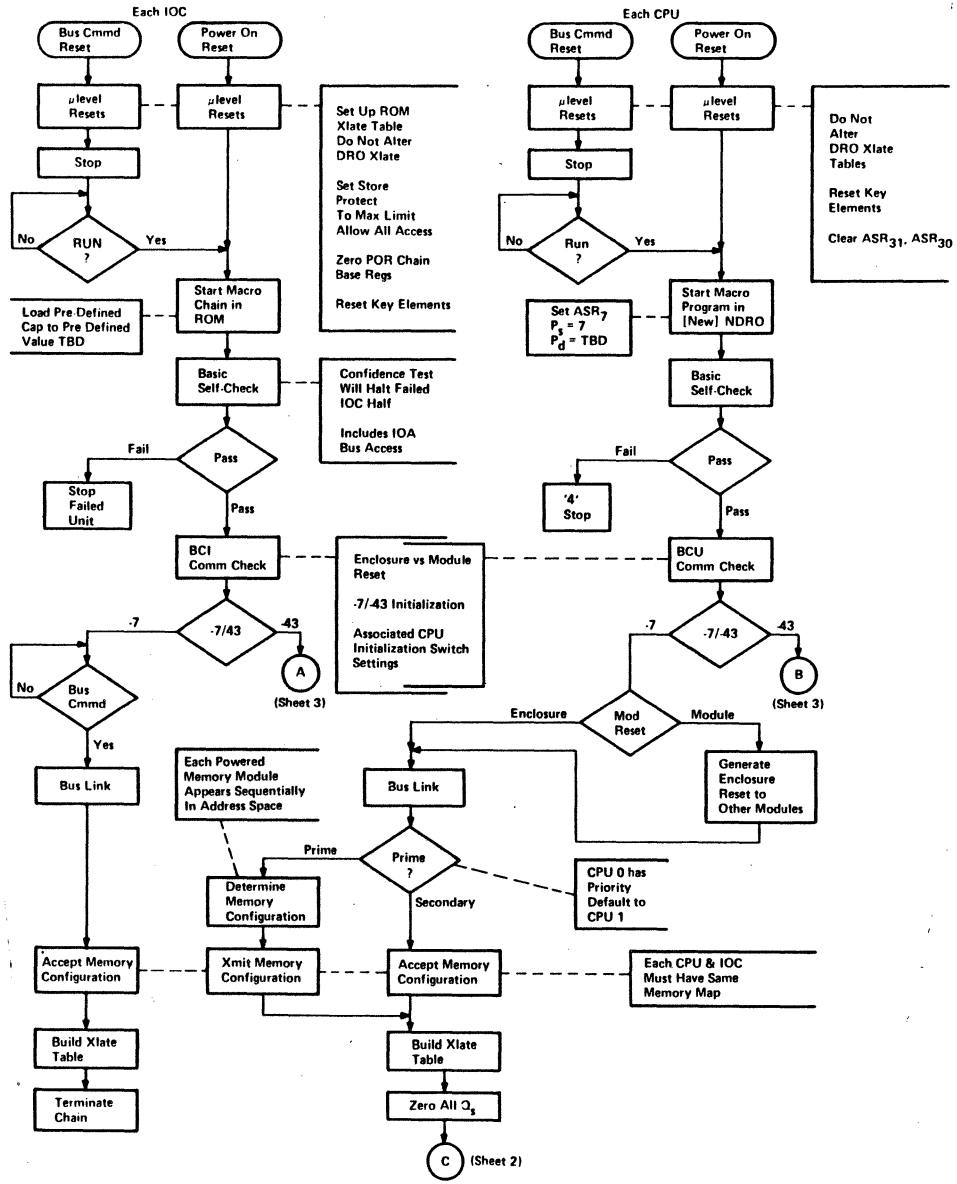
LABORATORY IPL/BOOT

- Automatic Processes in Multiple "Environments" Strongly Suggests Multiple NDRO Part Numbers
- Single NDRO Part Number Provides Total Operator (Manual) Control

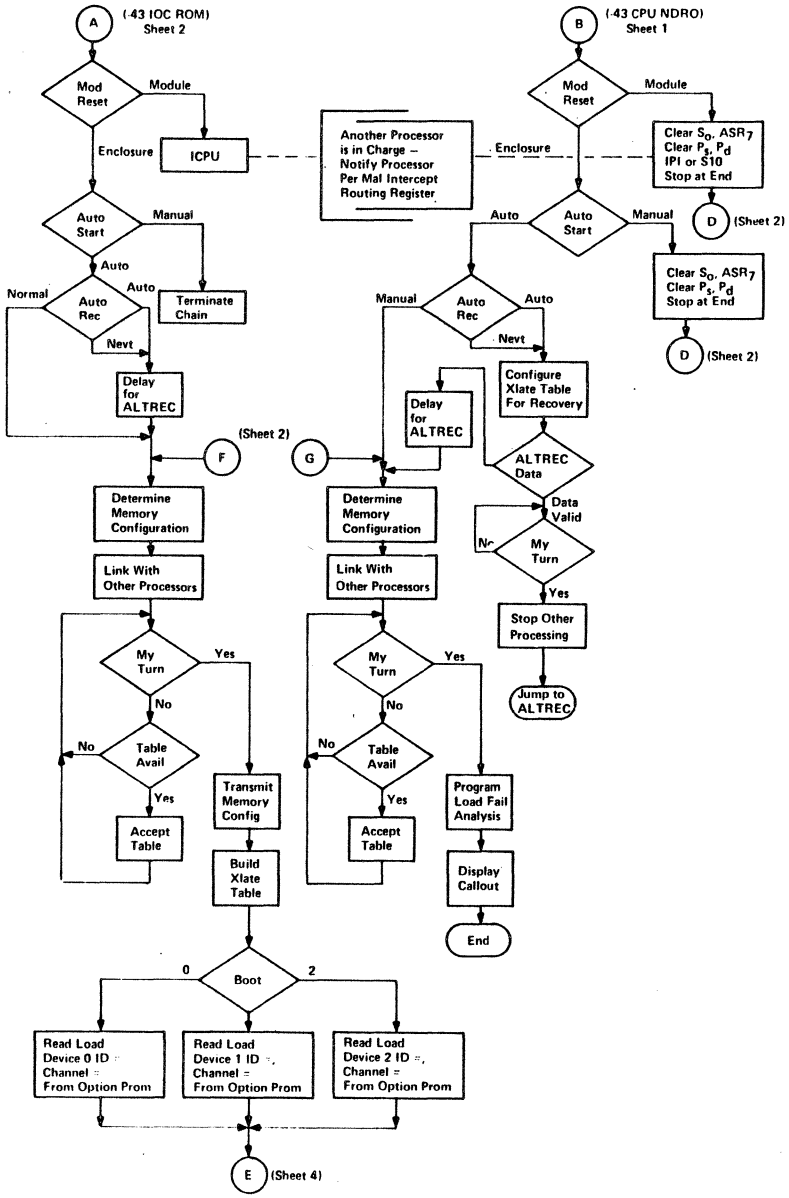
AN/UYK-43 OPERATOR CONTROL SWITCHES

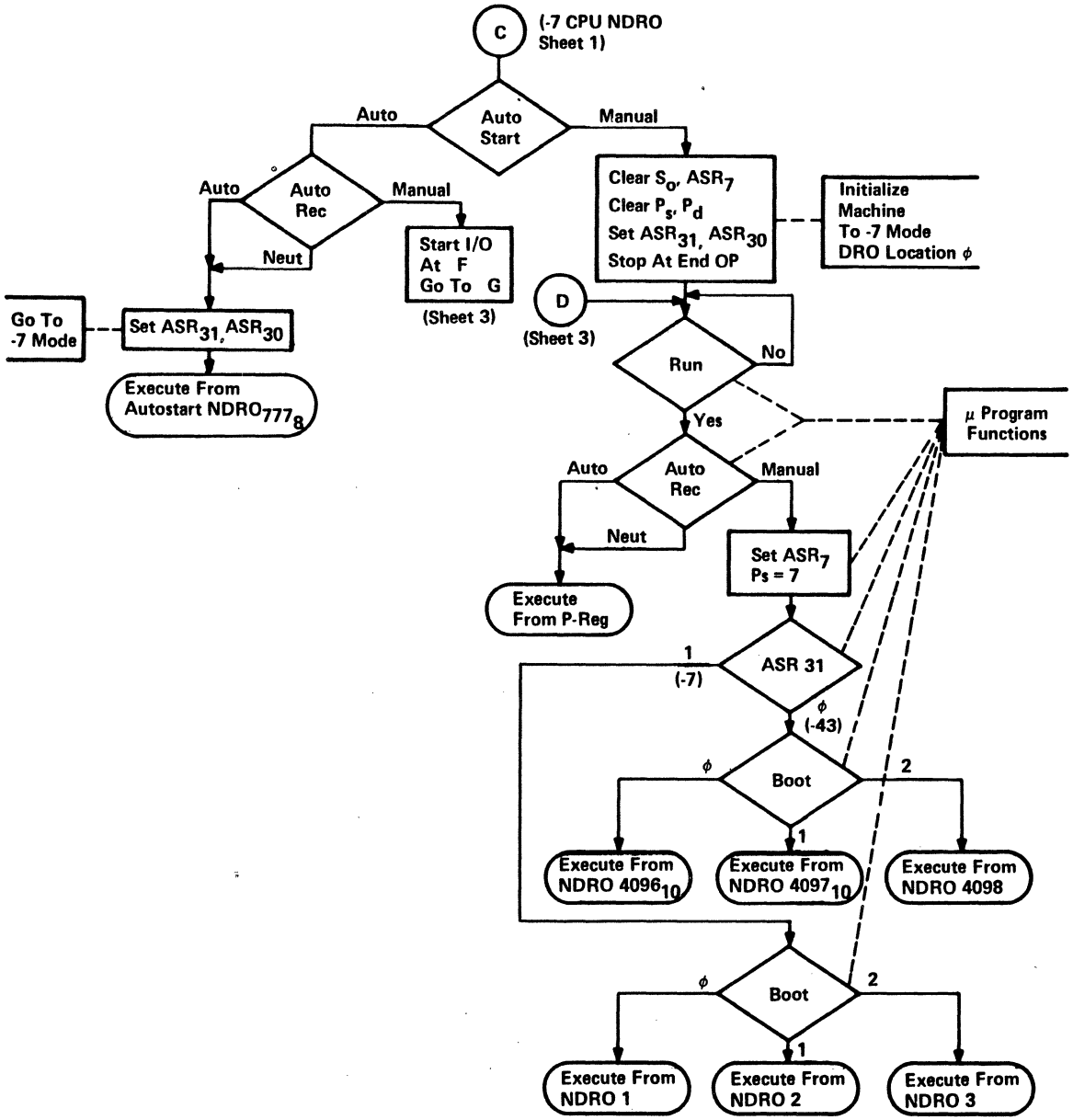
	Autostart	Autorecovery	Other	
Normal Operation	Auto	Auto/Neut*	(43 Boot)[1]	Attempt recovery, else IOC loader per boot[2]
	Auto	Auto/Neut	(7 Boot)[1]	Execute highest NDRO address (Note: Autorecovery = auto causes reboot[3] on nested Class II interrupts)
Load (Diagnose)	Auto	Manual*	–	IOC loader per boot[2] (Load record may include SASD)
Execute NDRO	Manual[4]	Manual	–	Execute NDRO address 1, 2, 3, per boot[2] (If ASR 31 = 0[5] execute NDRO addresses 4097, 4098, 4099)*
Execute DRO	Manual[4]	Auto/Neut	–	Execute DRO address in P register
Modify Load	–	–	Stop 6[4]	Stop before load. To allow device, channel to be changed
Modify Start	–	–	Stop 7[4]	Stop before execution of first load block to allow start address to be changed

* Unique to AN/UYK-43; all other modes are comparable to AN/UYK-7
1 Information from the options PROM
2 Boot = Bootswitch 0, 1, 2
3 Reboot = Execute NDRO address per boot
4 Computer will stop to allow modification, must be started again
5 ASR 31 will be set automatically per options PROM but may be modified

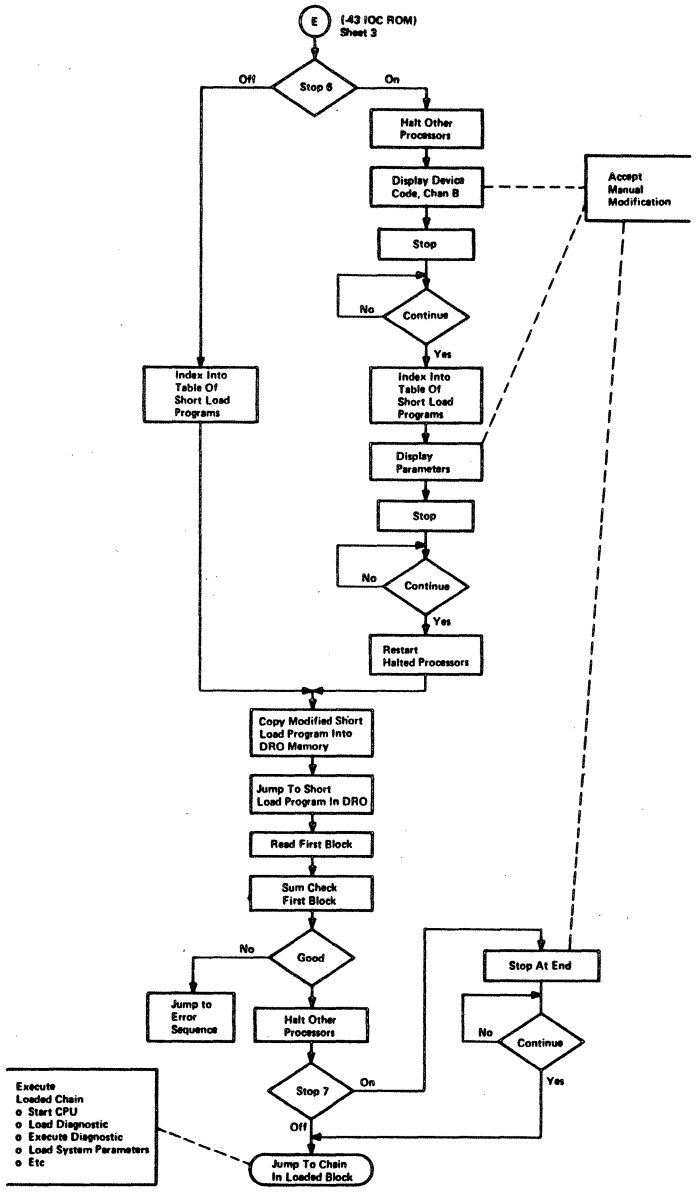

Each IOC
Bus Cmmd Reset
Power On Reset
μlevel Resets
Stop
No
RUN ?
Yes
Load Pre Defined Cap to Pre Defined Value TBD
Start Macro Chain in ROM
Basic Self-Check
Fail
Pass
Stop Failed Unit
BCI Comm Check
·7
·7/43
·43
No
Bus Cmmd
Yes
Bus Link
Accept Memory Configuration
Build Xlate Table
Terminate Chain
A
(Sheet 3)
Set Up ROM Xlate Table
Do Not Alter DRO Xlate
Set Store Protect To Max Limit Allow All Access
Zero POR Chain Base Regs
Reset Key Elements
Confidence Test Will Halt Failed IOC Half
Includes IOA Bus Access
Enclosure vs Module Reset
·7/·43 Initialization
Associated CPU Initialization Switch Settings
Each Powered Memory Module Appears Sequentially In Address Space
Prime
Determine Memory Configuration
Xmit Memory Configuration
Each CPU
Bus Cmmd Reset
Power On Reset
μlevel Resets
Stop
No
Run ?
Yes
Set ASR7 Ps = 7 Pd = TBD
Start Macro Program in [New] NDRO
Basic Self-Check
Fail
Pass
'4' Stop
BCU Comm Check
·7
·7/43
·43
B
(Sheet 3)
Enclosure
Mod Reset
Module
Generate Enclosure Reset to Other Modules
Bus Link
Prime ?
Secondary
CPU 0 has Priority Default to CPU 1
Accept Memory Configuration
Each CPU & IOC Must Have Same Memory Map
Build Xlate Table
Zero All Ωs
C
(Sheet 2)
Do Not Alter DRO Xlate Tables
Reset Key Elements
Clear ASR31, ASR30

SYSTEM INITIALIZATION




C
(-7 CPU NDRO Sheet 1)
Auto Start
Auto
Manual
Auto Rec
Auto
Manual
Neut
Start I/O At F Go To G
(Sheet 3)
Clear S_o, ASR_7
Clear P_s, P_d
Set ASR_{31}, ASR_{30}
Stop At End OP
Initialize Machine To -7 Mode DRO Location ϕ
Go To -7 Mode
Set ASR_{31}, ASR_{30}
Execute From Autostart $NDRO_{777_8}$
D
(Sheet 3)
Run
No
Yes
μ Program Functions
Auto Rec
Auto
Manual
Neut
Execute From P-Reg
Set ASR_7 Ps = 7
ASR 31
1 (-7)
ϕ (-43)
Boot
ϕ
1
2
Execute From $NDRO\ 4096_{10}$
Execute From $NDRO\ 4097_{10}$
Execute From NDRO 4098
Boot
ϕ
1
2
Execute From NDRO 1
Execute From NDRO 2
Execute From NDRO 3

SYSTEM INITIALIZATION



AN/UYK-43 NDRO Presentation

- Mission
- Capabilities And Services
- CPU NDRO Hierarchy Diagram
- IOC NDRO Hierarchy Diagram
- D/CP – NDRO SWITCH CONTROLS
- NDRO Function List
- NDRO Function Size Estimates

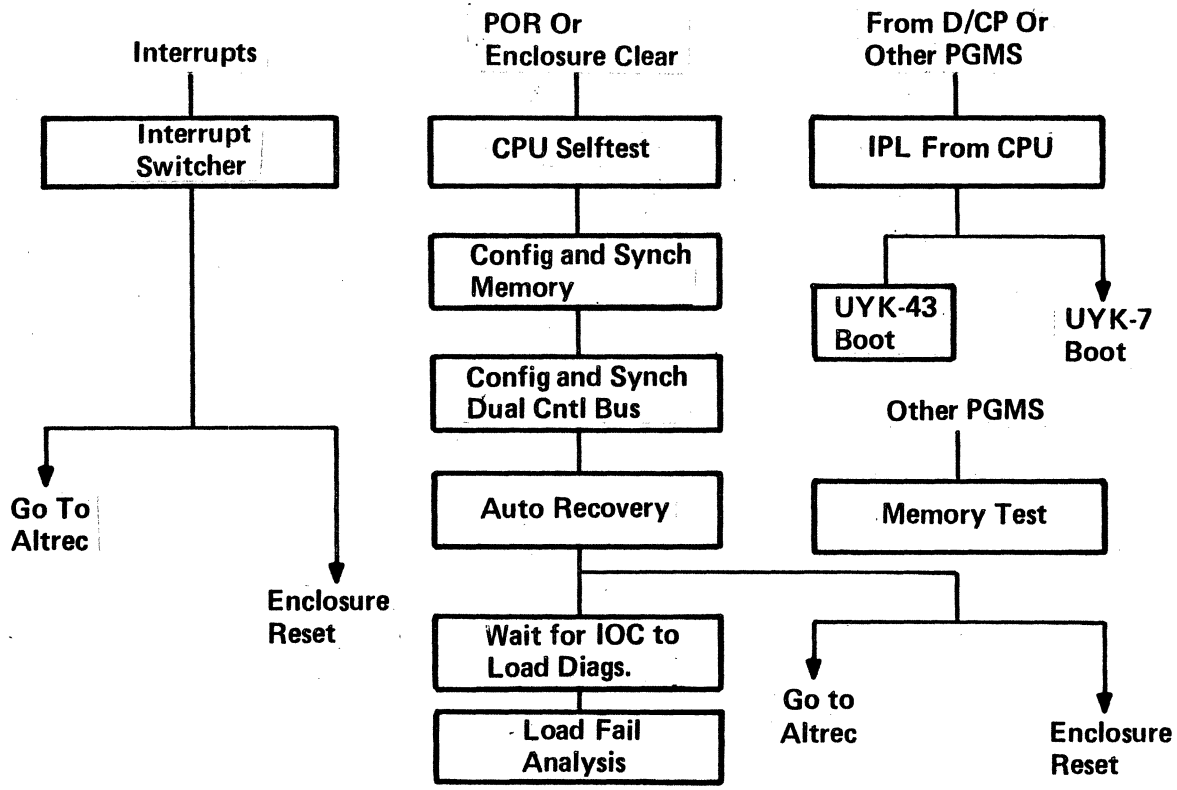
MISSION

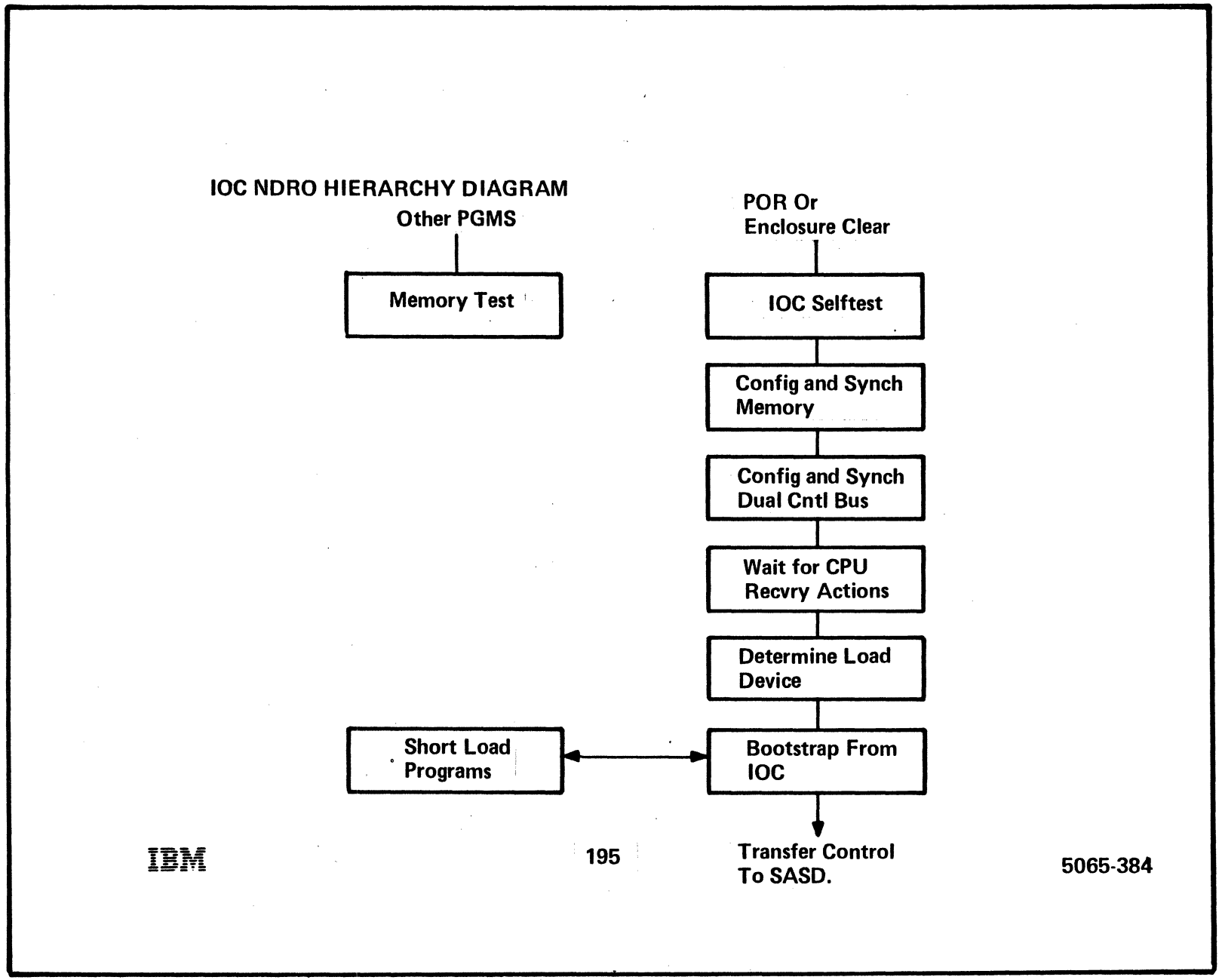
Provide the basic program capabilities that are necessary to load and initialize or re-initialize a system operation.

CAPABILITIES AND SERVICES

- AN/UYK-7 NDRO:
  - An existing user specified AN/IYK-7 NDRO shall be part of the CPU NDRO. All capabilities of the AN/UYK-7 NDRO shall be as specified in the existing PPS for that NDRO.
- AN/UYK-43 NDRO Basic Capabilities:
  - Loading of programs into a specifiable area of main memory from a specified peripheral,
  - Control of automatic program execution upon application of power to the computer,
  - ROCU initiation of program execution or the bootstrap load operation, and
  - Prevention of a program hang condition caused by a failed functional memory module.
- AN/UYK-43 NDRO Diagnostic Capabilities:
  - Automatic verification of the control, status, data, and address interfaces among the functional modules of the computer, and
  - Automatic isolation of a failure which prevents load of the diagnostic programs.
- Other Provisions:
  - 4096 32-bit words reserved for inclusion of User-Specified Program(s), and
  - A minimum of twenty percent unused NDRO memory locations available for future growth after all required functions have been implemented.

CPU NDRO HIERARCHY DIAGRAM




IOC NDRO HIERARCHY DIAGRAM
Other PGMS
Memory Test
POR Or
Enclosure Clear
IOC Selftest
Config and Synch
Memory
Config and Synch
Dual Cntl Bus
Wait for CPU
Recvry Actions
Determine Load
Device
Short Load
Programs
Bootstrap From
IOC
Transfer Control
To SASD.
IBM
195
5065-384

D/CP – NDRO SWITCH CONTROLS

UNIT = RSETY

AN/UYK-43 reset sequence activated by FHM reset. FHM reset is caused by power on reset or may be simulated from another processor, or panel interface.

This sequence will be activated simultaneously on several processors if enclosure power is restored. The logic defined by this PDL describes the interaction between the FHM's. It is a time filtering sequence, where one processor is designated by time slot to do something while the others wait their turn to proceed in a pre-arranged sequence of actions.

The auto rec, auto start, bootstrap, module select, stop, start and continue switches, at the D/CP, and data from the options PROM, of the NDRO type and load device type, control the actions of this sequence.

D/CP – NDRO SWITCH CONTROLS (CONT)

Auto Start	Auto Rec	NDRO Mode	Action
Auto	Auto/Neut	7	Recover from NDRO 777. (AUTOSTART)
Auto	Auto/Neut	43	Recover, reload program or load the diagnostics.
Auto	Manual	7/43	Load the diagnostics from an IOC.
Manual	Don't care	7	Stop w/ Xlate tables reinitialized.
Manual	Don't Care	43	Stop w/o Xlate tables reinitialized (the operator can restart in these cases by selection of D/CP switches from NDRO or memory sequences.)
N/A	Manual	7	Micro branch to UYK-7 bootstrap.
N/A	Manual	43	Micro branch to UYK-43 bootstrap.
N/A	Auto/Neut	7/43	Micro branch to preg location.

D/CP – NDRO SWITCH CONTROLS (CONT)

UYK-43 mode bootstrap operations will use stop switches in a manner consistent with most UYK-7 bootstrap programs.

Stop switch 6 shall cause stop before load.

Stop switch 7 shall cause stop before execute.

The start and cont switches at the D/CP are used to restart a stopped program.

Start, causes all processors in enclosure to restart.

Cont, starts 1 processor per module select switch.

NDRO FUNCTION LIST

The functions contained in NDRO are as follows:

- AN/UYK-7 NDRO (Located in CPU NDRO):
  - Bootstrap,
  - Auto start,
  - Computer start, and
  - Interrupt switching.
  - Memory test,
  - Interface test, and
  - Load failure analysis.

NDRO FUNCTION LIST (CONT)

- AN/UYK-43 CPU Functions (Located in CPU NDRO):
  - CPU selftest,
  - Configure and synchronize memory,
  - Configure and synchronize the dual control bus,
  - Auto recovery,
  - Load fail analysis,
  - AN/UYK-43 bootstrap from CPU,
  - Interrupt switcher,
  - BOOT from CPU, and
  - Memory test.

NDRO FUNCTION LIST (CONT)

- AN/UYK-43 IOC Functions (Located in IOC ROM):
  - IOC selftest,
  - Configure and synchronize memory,
  - Configure and synchronize the dual control bus,
  - Short load programs,
  - Determine load device,
  - Bootstrap from IOC, and
  - Memory test.

NDRO FUNCTION SIZE ESTIMATES

CPU NDRO Storage Allocation

Functional Description	Words
User Specified NDRO + AN/UYK-7 NDRO	4096
CPU Selftest. (Initialization)	50
Configure And Synchronize Memory. (Initialization)	200
Configure And Synchronize The Bus. (Initialization)	200
Auto Recovery. (Initialization)	100
Load Fail Analysis. (Initialization)	4000
AN/UYK-43 Bootstrap From CPU. (Initialization)	200
Interrupt Switcher.	100
IPL From CPU.	100
Memory Test	100
Spare	3142
Total	12288

NDRO FUNCTION SIZE ESTIMATES (Cont)

IOC NDRO Storage Allocation

Functional Description	Words
IOC Selftest. (Initialization)	50
Configure And Synchronize Memory. (Initialization)	200
Configure And Synchronize The Bus. (Initialization)	200
Short Load Programs.	200
Determine Load Device. (Initialization)	100
Bootstrap From IOC. (Initialization)	500
IPL From IOC.	50
Memory Test.	200
Spare	5048
Total	2048

FAULT TOLERANCE
DESIGN PHILOSOPHY

FAULT TOLERANCE DESIGN PHILOSOPHY

- Casualty Reaction Document
- Fault Tolerance = System Recovery
- Fault Tolerance = On-Line Repair
- Fault Tolerance For
  - Power Transients
  - Operator/Software RE-IPL
  - Off-Line Diagnostics
- Software Elements of Fault Tolerance

CASUALTY REACTION ON THE AN/UYK-43 – OUTLINE (PRELIMINARY DUE 7/15)

1. Scope
2. Overview (draft 4/15)
3. Fault Detection
4. Automatic Recovery
5. Casualty Reaction Control
6. FHM Isolation
7. Hardware Reconfiguration
8. Software Recovery - Restart
9. LRU Isolation
10. On-line Repair
11. Self-Test
12. Restoration
13. Interfaces & Relationships
14. Initialization Requirements
15. FTRM Requirements
16. Diagnostic Program Requirements
17. Maintenance Procedures
18. User Application Design Guidelines
19. Casualty Reaction Verification
20. System Reliability Models
21. Flow Diagrams

PRINCIPAL PROCESSES IN CASUALTY REACTION

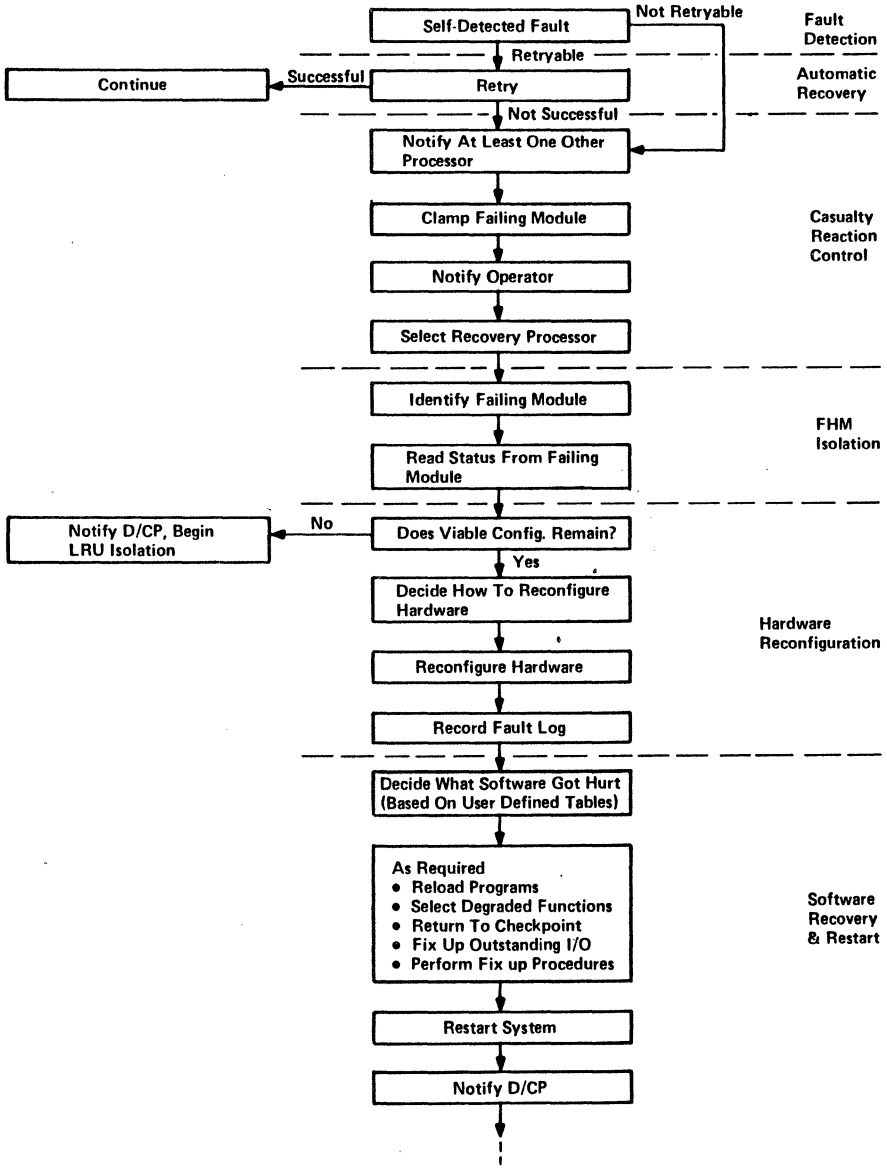
Fault Recovery

1. Fault Detection
2. Automatic Recovery
3. Casualty Reaction Control
4. Functional Hardware Module (FHM) Isolation
5. Hardware Reconfiguration
6. Software Recovery & Restart

Fault Repair

7. LRU Isolation
8. On-Line Repair
9. Self-Test
10. Restoration

FAULT RECOVERY PHASE



KEY CONCEPTS IN FAULT RECOVERY

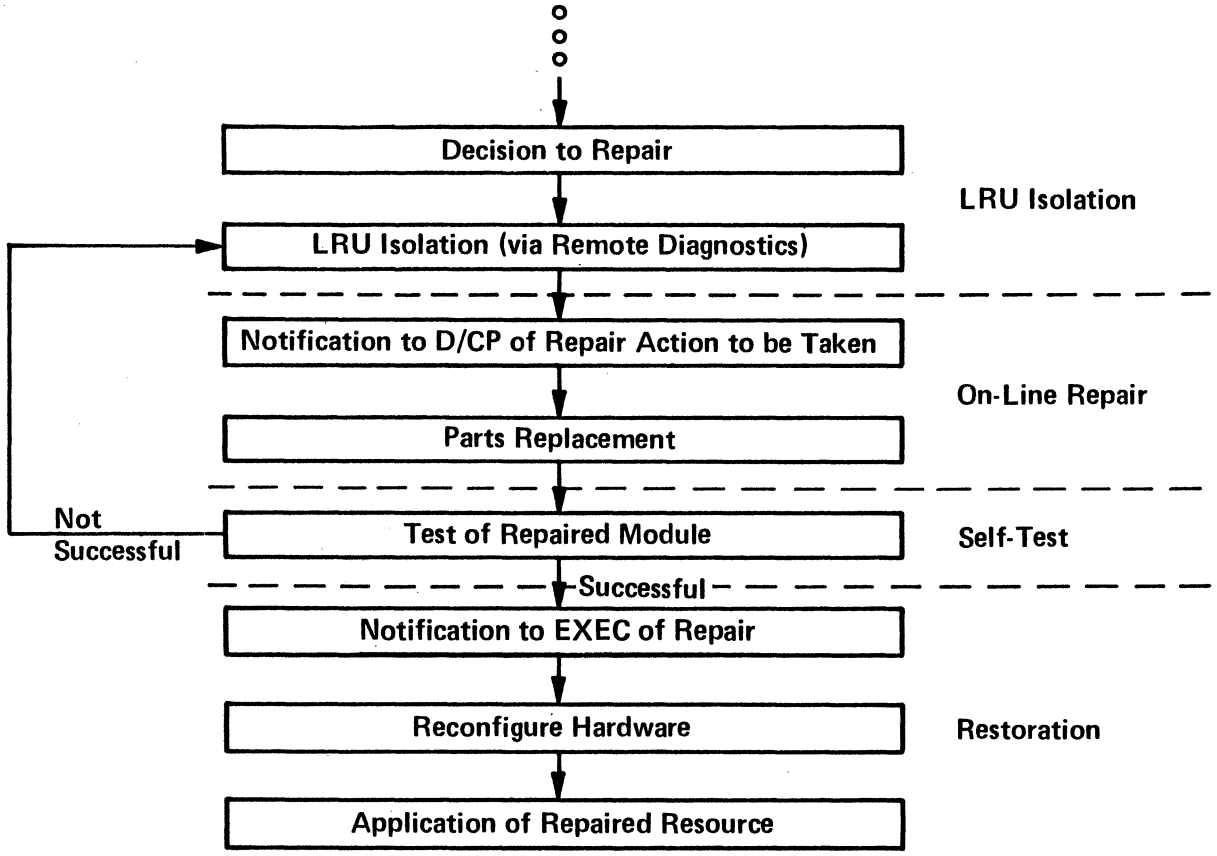
1. Fault Detection
   - Hardware or Microcode
   - Real-Time
   - Check All Transactions
   - Record Status

2. Automatic Recovery
   - Memory Bus
   - Control Bus
   - ECC in Monolithic Memory
   - Core-Backed Monolithic Memory
   - Cache Disable

3. Recovery Processor
   - Any CPU or IOC
   - Immediate Notification
   - Software Control

4. Hardware Configuration
   - Control Bus Interface
   - Memory Bus Interface
   - External Load/Store
   - Start/Stop/Control

FAULT REPAIR PHASE



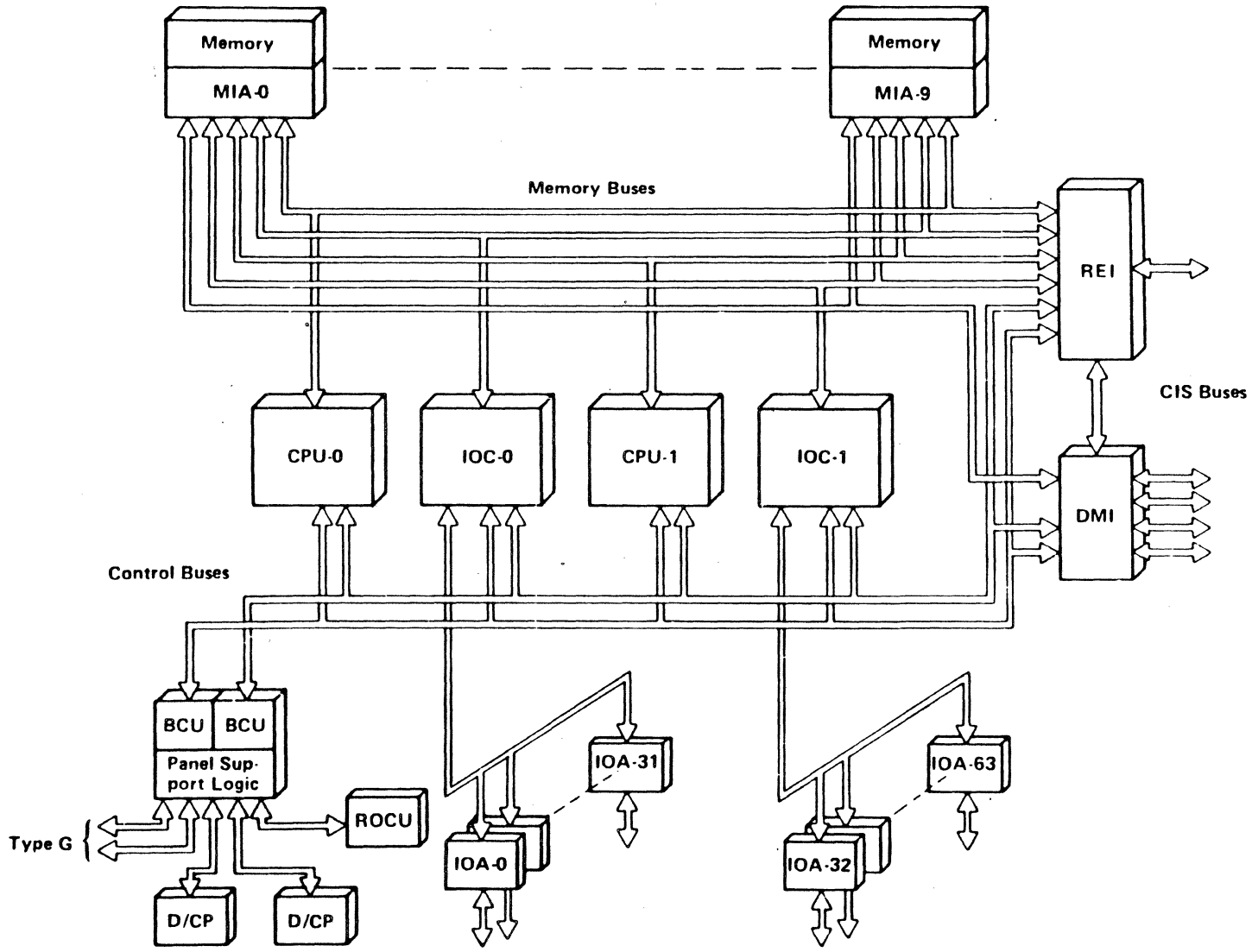
KEY CONCEPTS IN FAULT REPAIR

1. LRU Isolation By Diagnostics
   - Distributed Diagnostic Process
   - Processor Under Test Is Functionally Isolated
2. "One-Button" Repair Scenario
   - Minimal Human Decisions
   - Simple Control

DISTRIBUTED DIAGNOSTIC PROCESS

- No Processor Diagnoses Itself
- Both CPU's and IOC's Are Sufficiently Intelligent to Control Diagnostics Therefore Every System Contains a Processor Other Than the Faulty Processor Capable of Controlling Diagnosis of That Faulty Processor
- Distributed Diagnostic Process Uses Operational Interfaces and Processors Minimizing Diagnostic Hardware and
  - Saving Cost
  - Reducing Possibility of Diagnostic Hardware Not Being Functional When Needed
  - Reducing Fault Group for Initial Diagnostic Checkers
- Distributed Diagnostic Process Avoids Potential Single-Point Failures During Load (Power-Transient Recovery, IPC, Off-Line Diagnostics)

MAXIMUM CAPABILITY CONFIGURATION

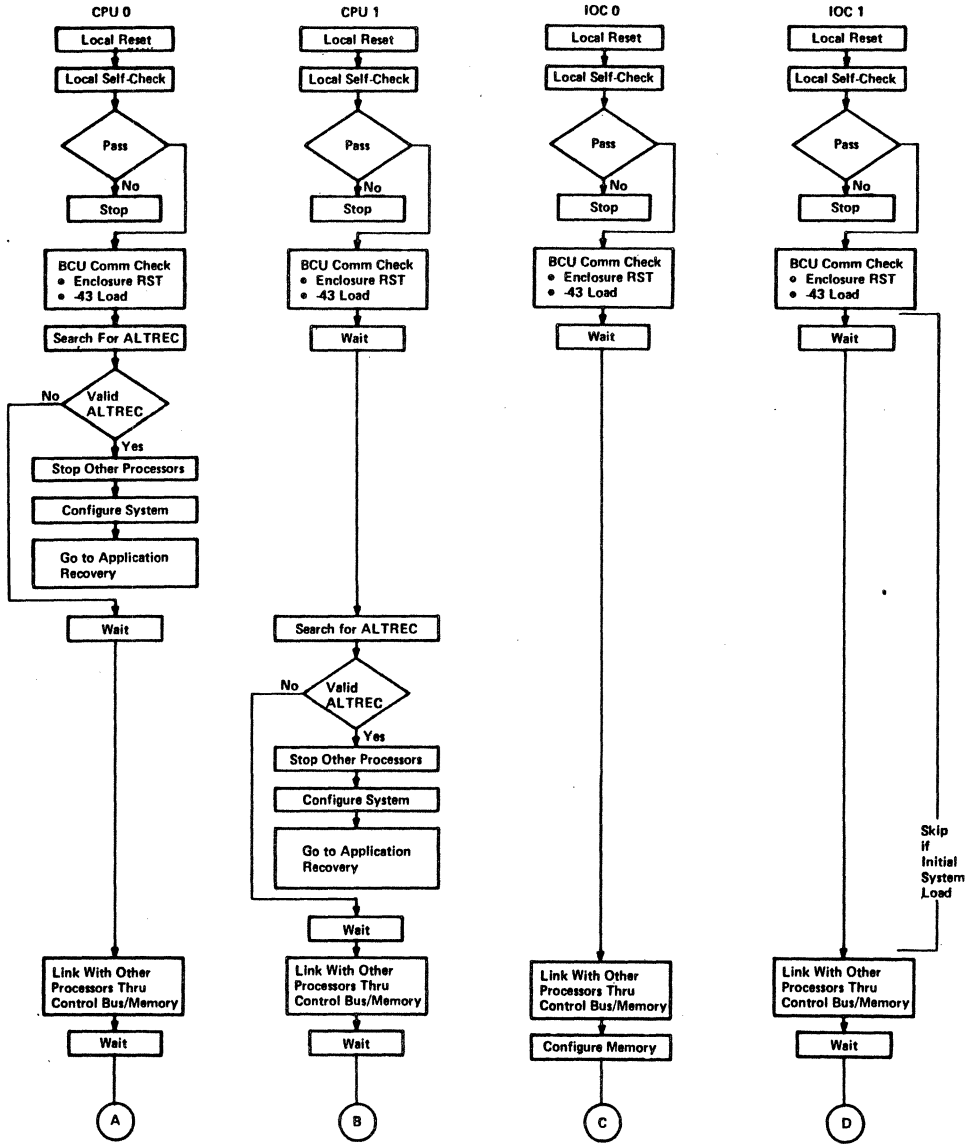


4874-362

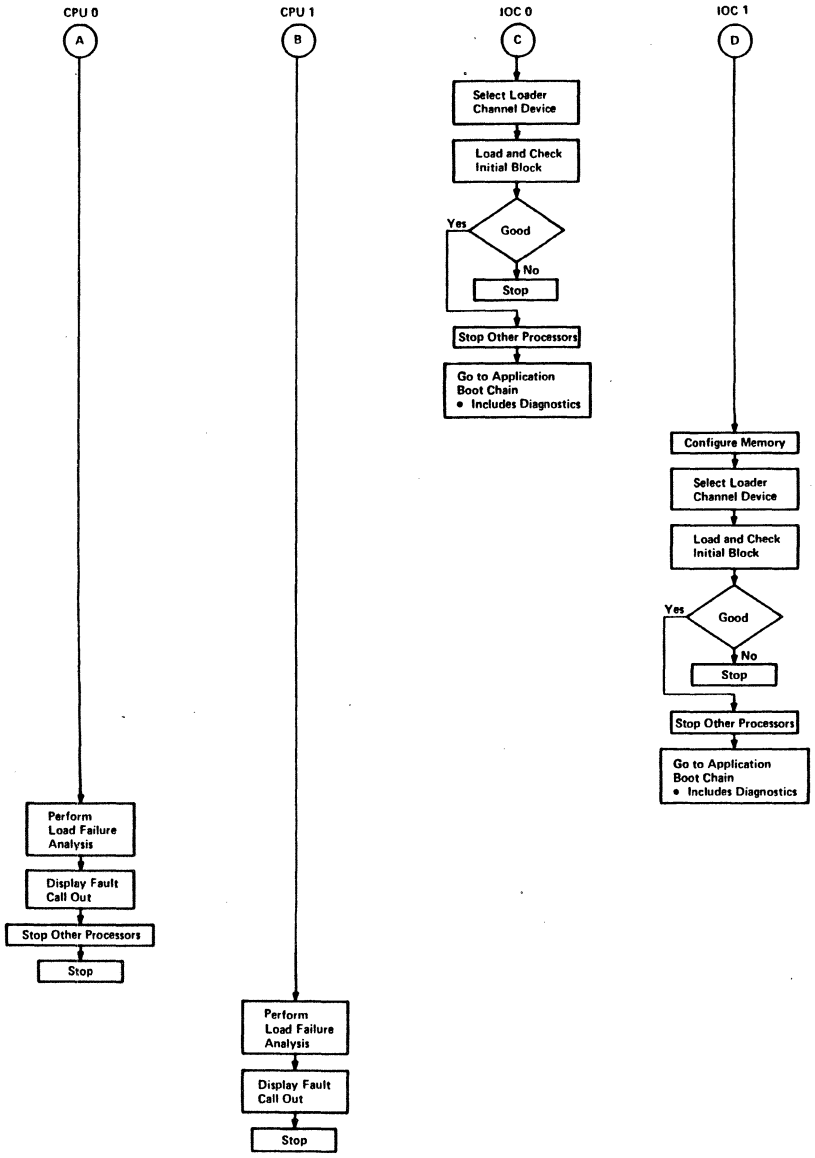
DISTRIBUTED DIAGNOSTIC (RECOVERY) PROCESS

- Avoids Single-Point Failures that Prevent Power-Transient Recovery or Initial Program Load (Boot)
- All Processors Active
  - Cross Monitoring
  - Time Filter Places One Processor at a Time in Charge
- Recovery Process
  - CPU Attempts Recovery
  - IO Controls Load
  - CPU Analyzes Load Failure

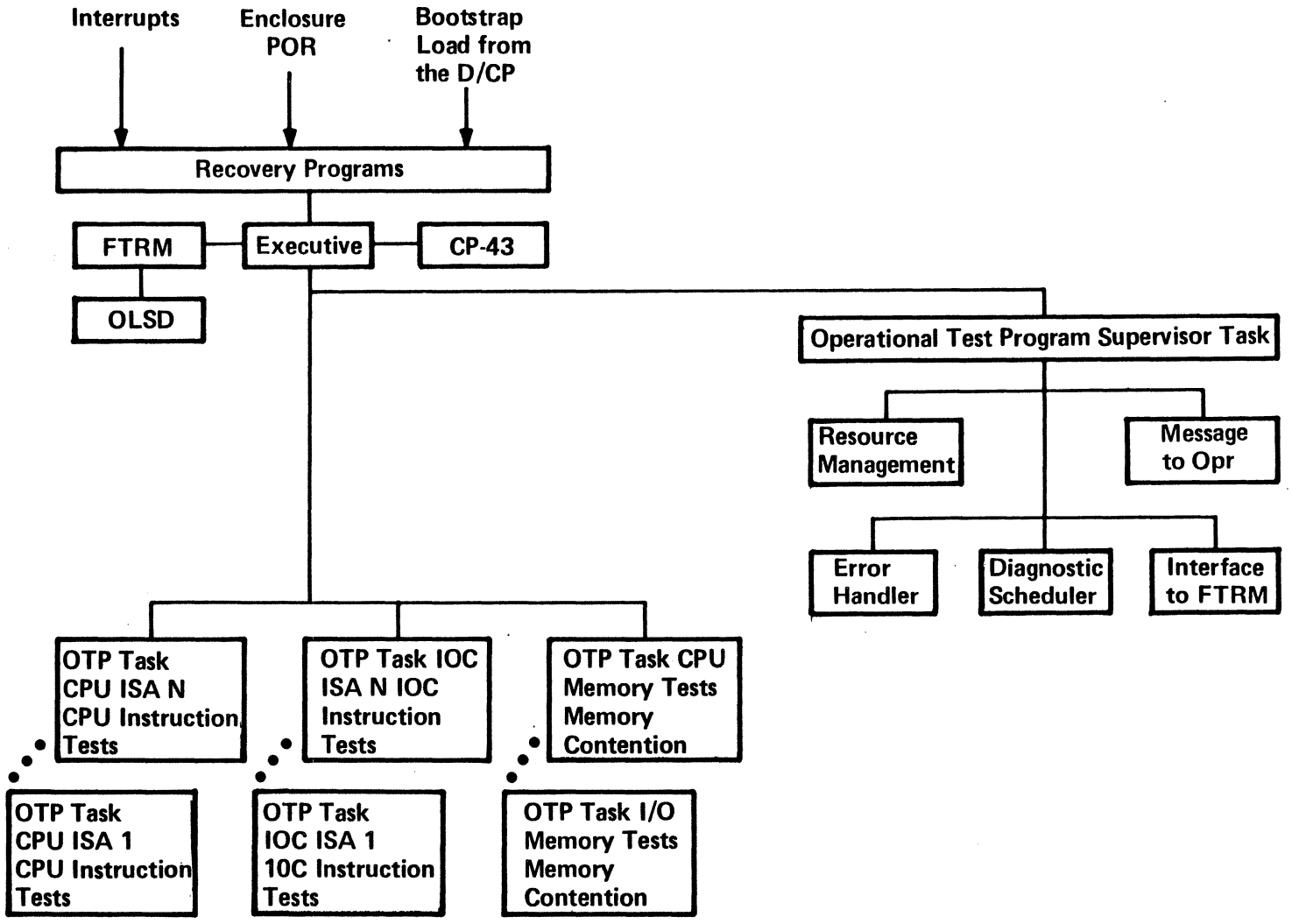
POWER TRANSIENT RECOVERY



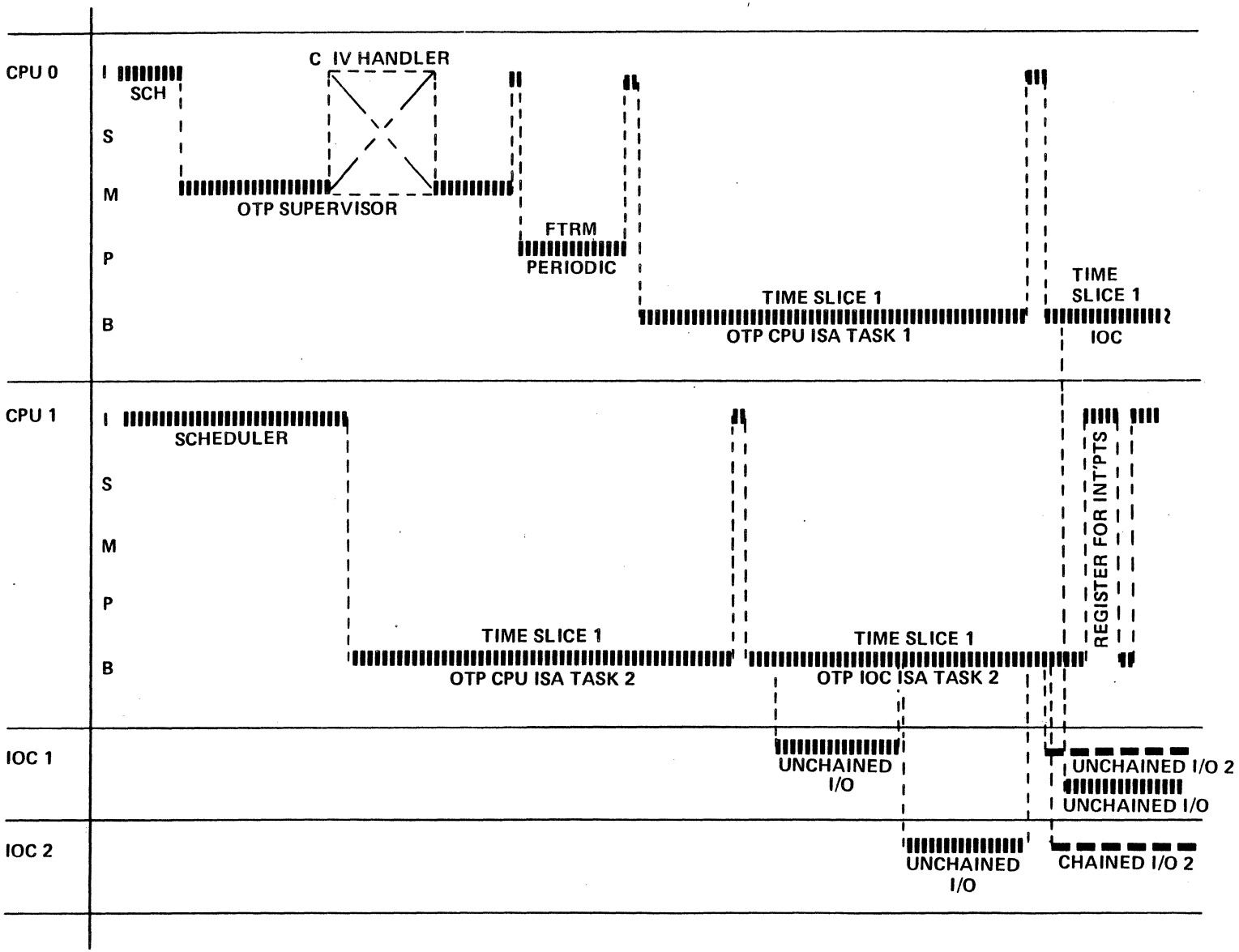
POWER TRANSIENT RECOVERY (continued)



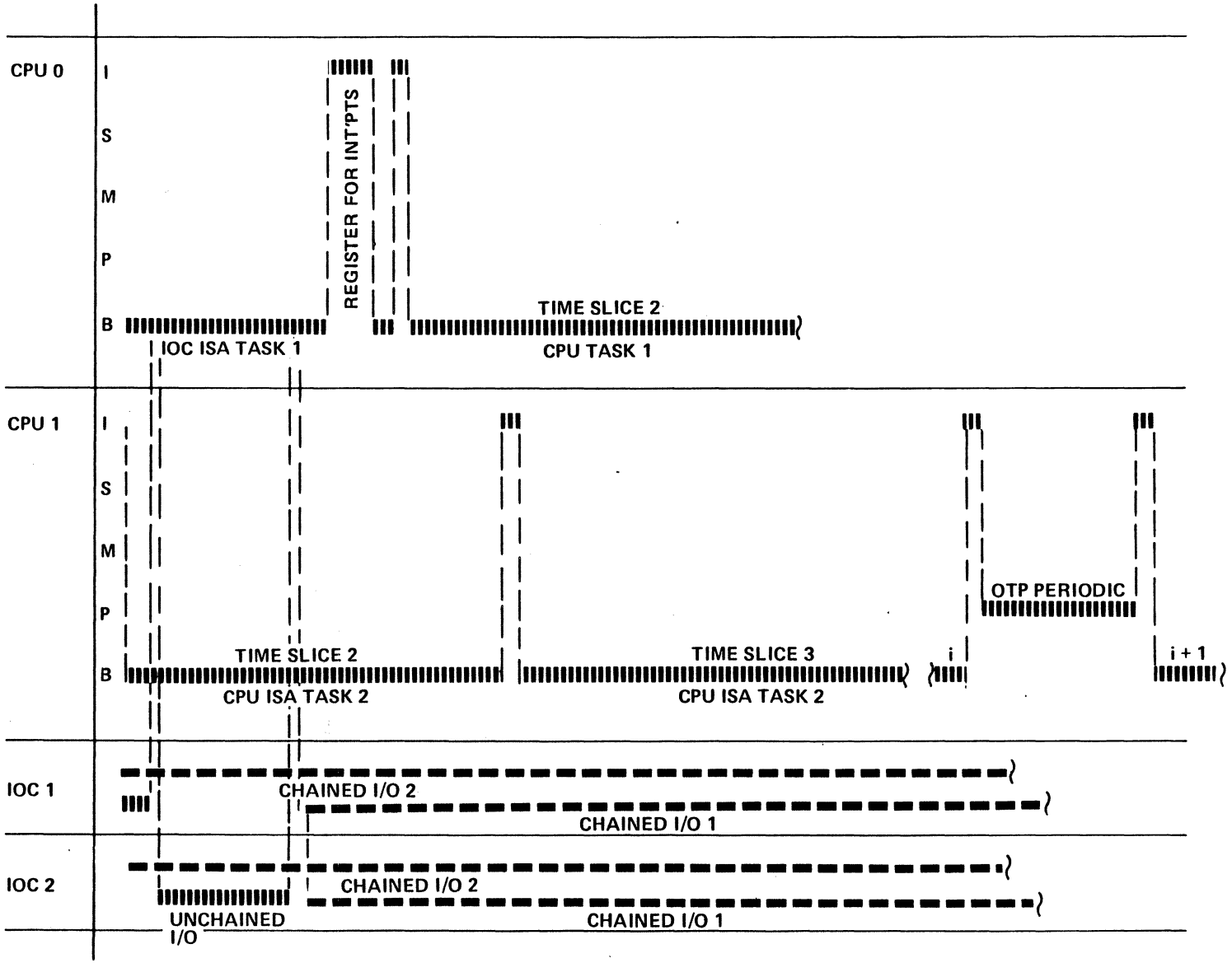
OTP FUNCTIONAL ENVIRONMENT



OTP EXECUTION SEQUENCE FROM START EXECUTION (Sheet 1 of 2)

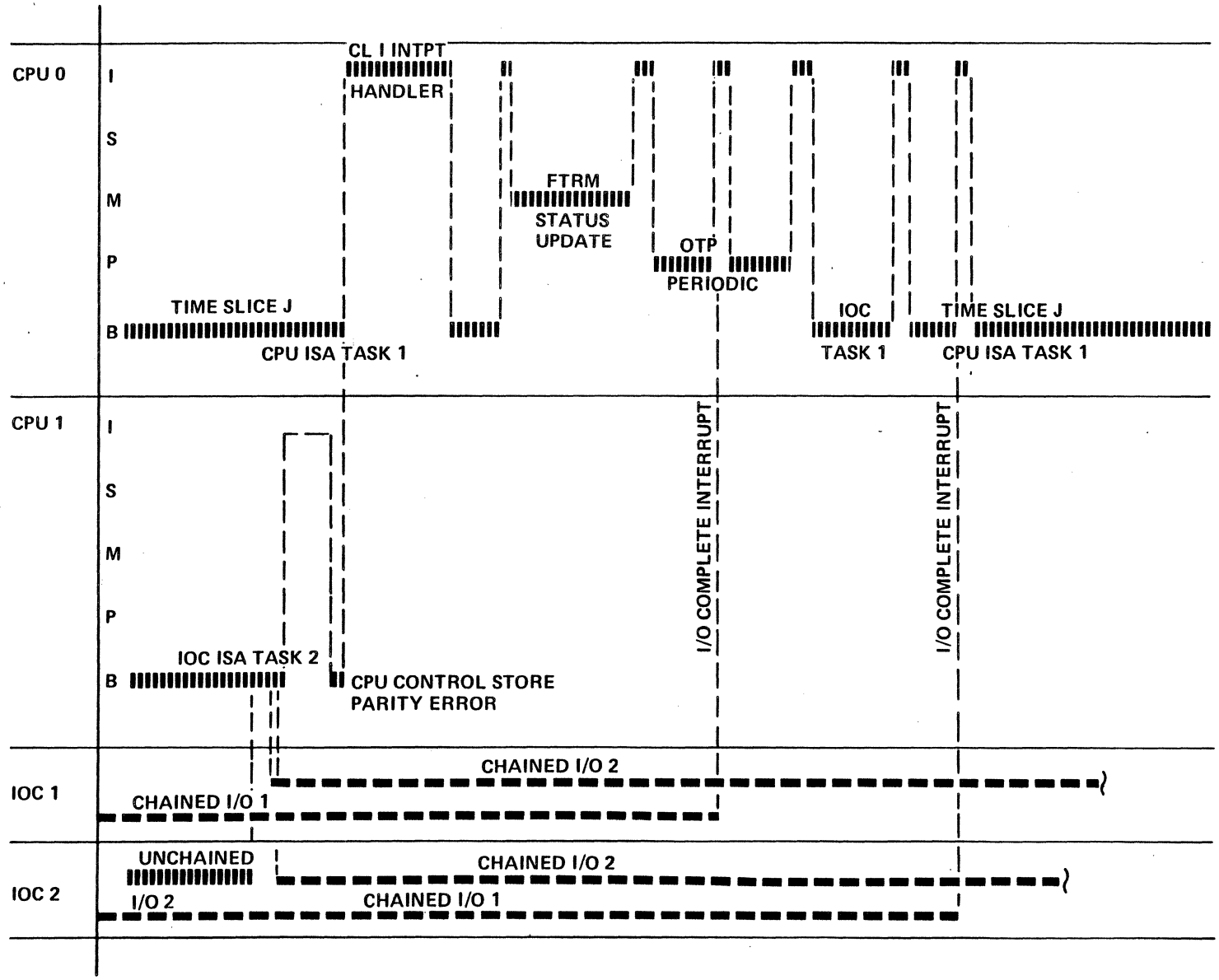


OTP EXECUTION SEQUENCE FROM START EXECUTION (Sheet 2 of 2)

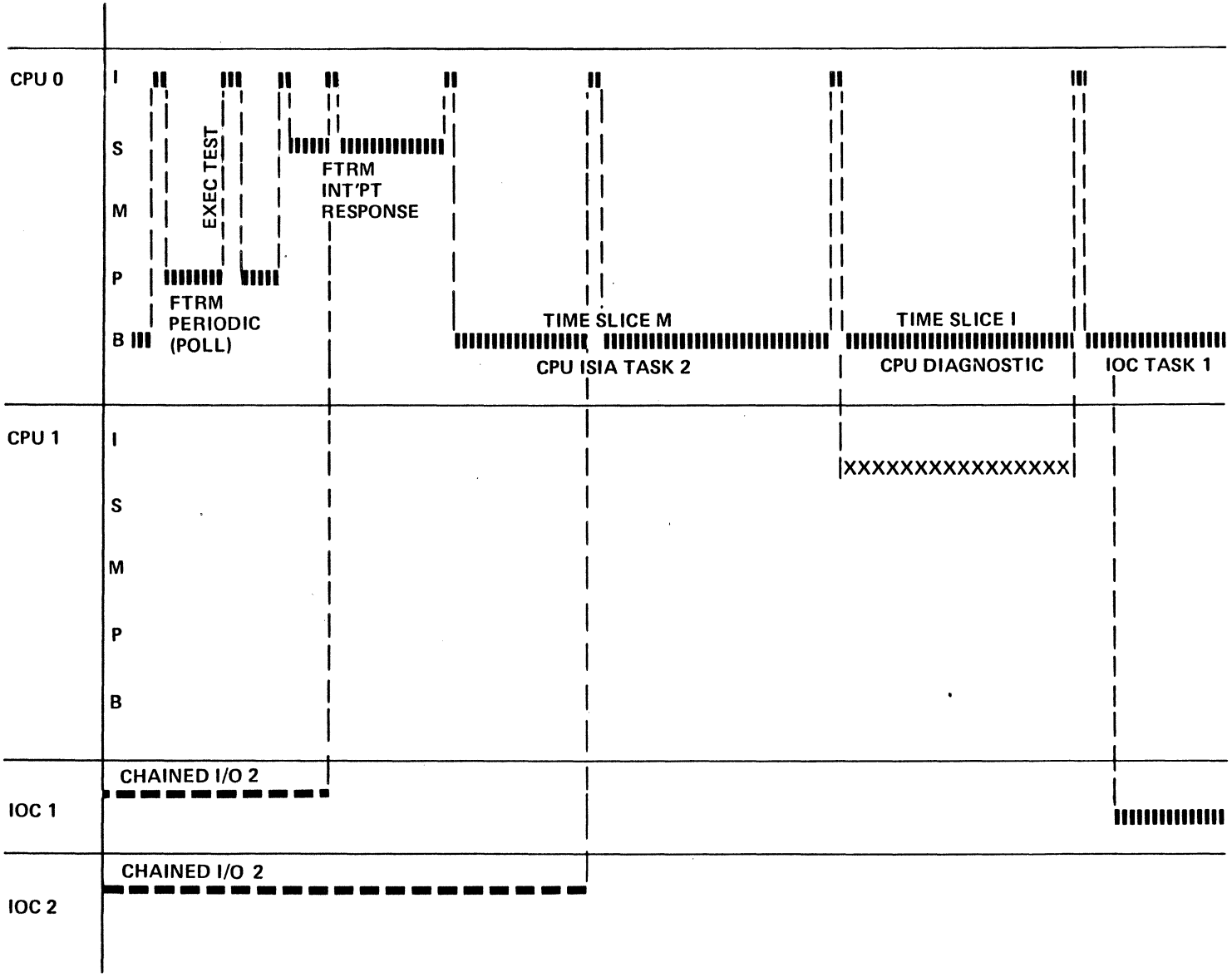


5065-83-6

OTP ERROR RESPONSE (Sheet 1 of 2)



OTP ERROR RESPONSE (Sheet 2 of 2)



5065-83-8

THERMAL DESIGN

IBM

5065-40

OBJECTIVE – MEET DESIGN SPEC/SOW

- Reliability
- Tj Max 80/90/120°C
- Air/H_2O Cooled LRU's Interchangeable
- Acoustics
- Volume
- Performance
- Worst Case Configurations

IBM

5065-41

THERMAL BOUNDARY CONDITIONS

- MIL-E-16400 Class IV
  - 0 to 50°C oper
  - -62 to 71°C non-oper.
- Air Cooled - Self Contained Blowers
  - Ambient air
  - $\Delta T_{max} = 14°C$
- Water Cooled MIL-W-21965
  - +40°C H_2O @ 1.4 GPM/kW @ $\Delta P = 10$ PSI
- Overtemperature Protection

IBM

5065-42

THERMAL PROBLEM

- 4 Computers
  - 2 Air cooled (A&B)
  - 2 H_2O cooled (A&B)
- Dissipations

	Air	H_2O
A	2.7 kw	2.3 kw
B	5.5 kw	4.7 kw

- Upper Temperature Limits (°C)

	Air	H_2O
Microcircuits	90	80
Power	120	120

- Common LRU's

Summary:

Thermal Design Meets Specification Requirements

IBM

5065-43

THERMAL DESIGN APPROACH

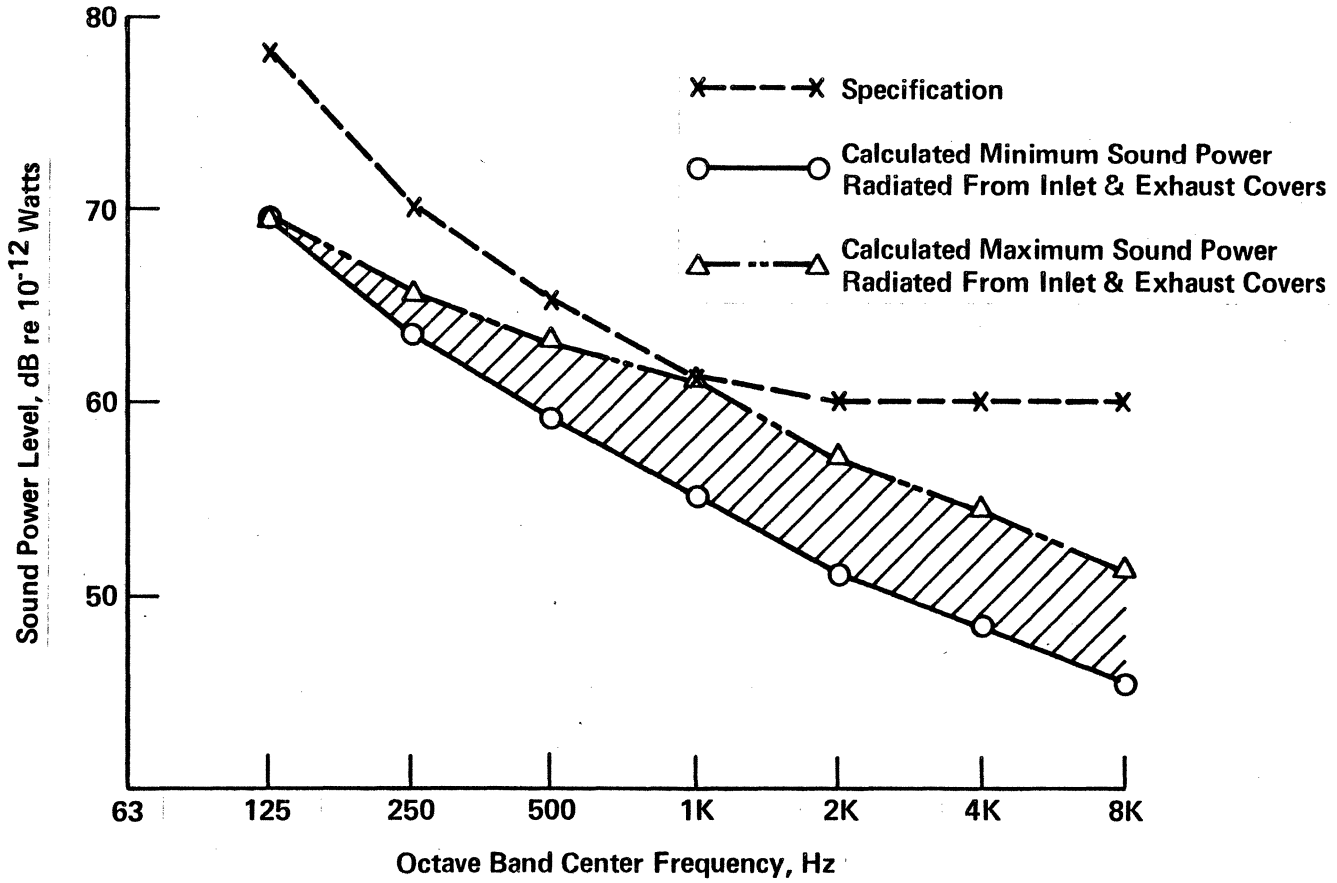
- Combination Mathematical and Empirical
- Cooling Redundancy – Avoid Single Point Failures
- High Reliability { 125°C Microcircuits; 150°C Power Devices
- LRU Commonality

EMPIRICAL DEVELOPMENT PROGRAM (AIR COOLED UNITS)

- Direct Air Cooling
- LRU
  - Non power module parameters
    Air flow parameters
    θ vs air flow (vel.)
  - Power modules
    -- θ vs air flow (vel.)
    -- Mounting concept
- Component Mounting
- θ j-c
- LRU Guidelines/Definition
  - Location of components
  - Mix LRU's by power
  - Bonding
  - Frame material
- Blowers
  - Single vs mult.
  - Acoustics
  - Redundancy
  - Flow @ 60 Hz vs. 90 Hz
  - Failure/degradation detection

AN/UYK-43 ACOUSTIC ANALYSIS

ENCLOSURE A

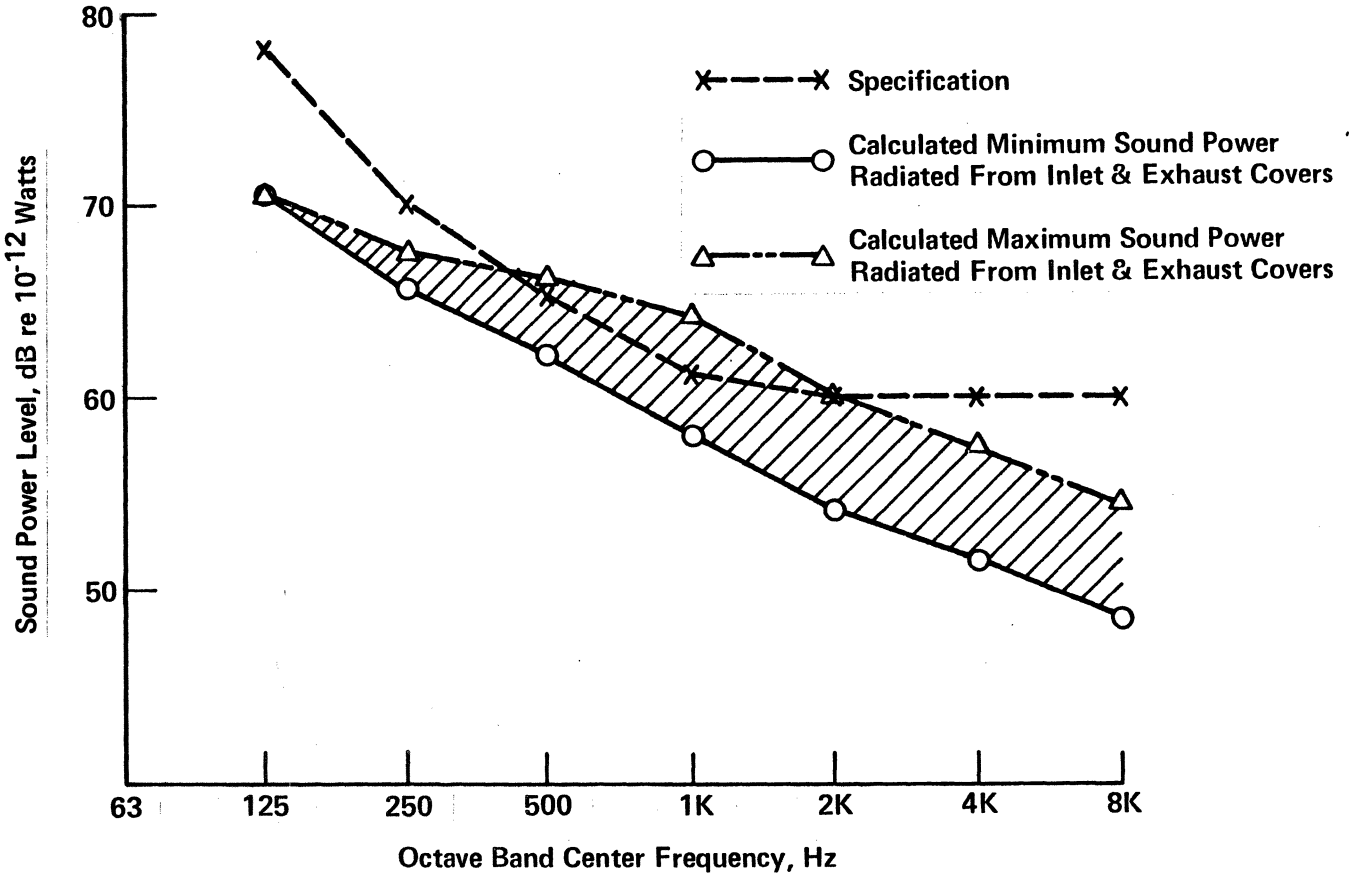


IBM

5065-44-1

AN/UYK-43 ACOUSTIC ANALYSIS

ENCLOSURE B



IBM

5065-44-2

EMPIRICAL DEVELOPMENT PROGRAM (AIR COOLED UNITS) (CONT'D)

SYSTEM

- Full Scale Mockup "B"
  - (Pictures)
  - (A ≈ 1/2 B)
- Blower Circuit Characterization of Modules (ΔP vs W)
  - 4 Fans, 8 Fans } 60 Hz & 90 Hz
- System Interaction
  - EMI/Air filters
  - Inlet areas
  - Distribution
  - ΔT rise
- Measure System Flow (ΔP air circuit)
- Blower Wiring/Inverter
- OTI Concept
- Door Converter Cooling Evaluation
- LRU Dummy Heat Load
  - Non power modules
  - Power modules

MATHEMATICAL:

- Input IBM 370/MCS Thermal Analyses Program For LRU's
- Complete Analyses - 100% Piece Part Output Analyses to Reliability/Designers

RESULTS OF PROGRAM

- High Confidence Thermal Design Concept
- LRU Design Guides Issued

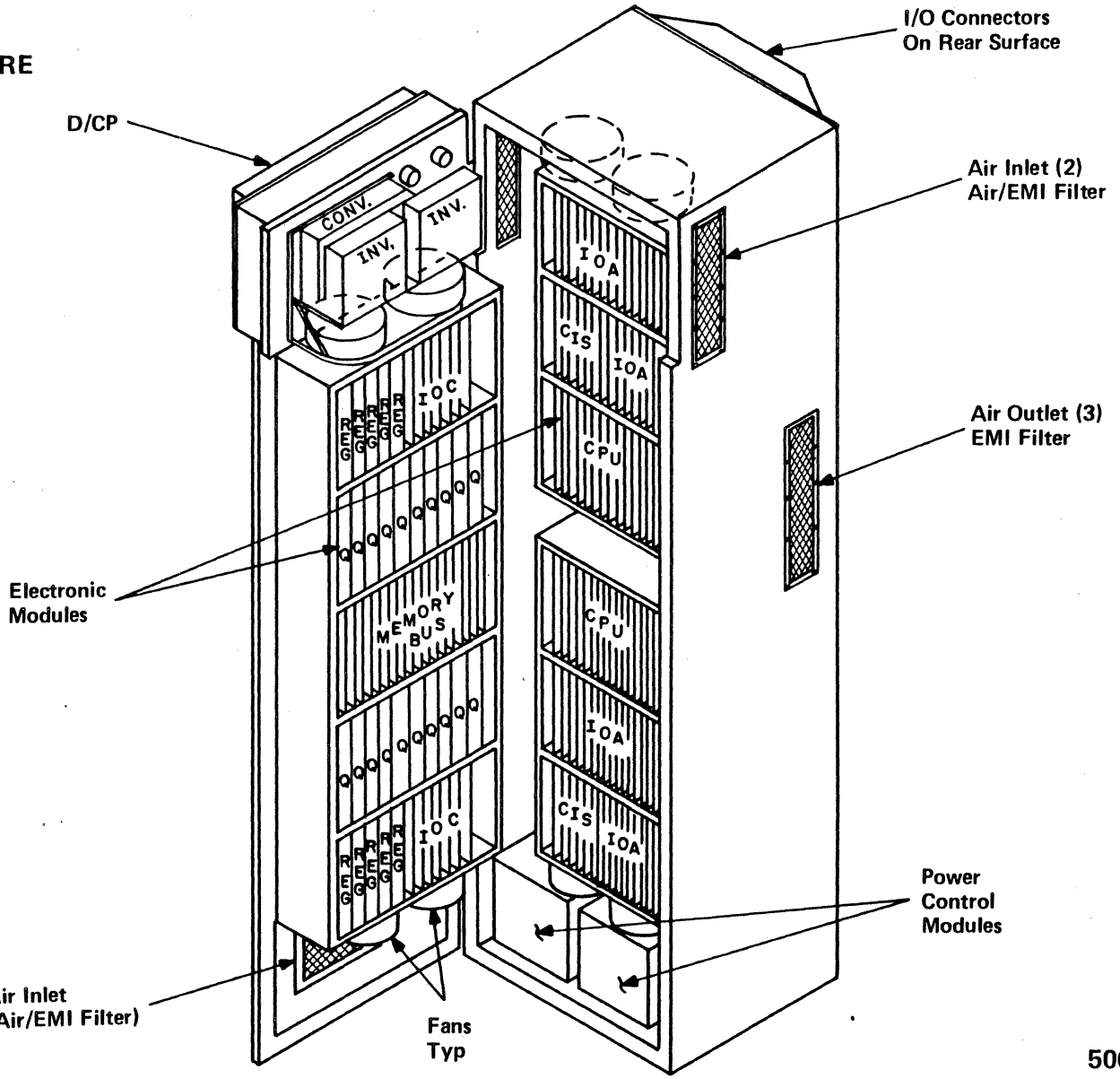
COMPUTER THERMAL DESIGN DESCRIPTION

AIR COOLED

	B	A
Illustration	Fig. 1	Fig. 4
Coolant/concept	Air/direct	Air/direct
Dissipation	5.5 kw (Fig. 2)	2.7 kw (Fig. 5)
Fans	8 MIL-901, 2 Spartan (Fig. 3) — 90 Hz (Hall)	4 MIL-901 — 90 Hz Hall
Air inlets (temp.)	3 Locations (Fig. 3) @ 50°C	1 Location (Fig. 6) @ 50°C
Air out (temp.)	3 Locations (Fig. 3) @ 58°C	1 Location (Fig. 6) @ 50°C
	ΔT = 8°C	ΔT = 8°C
Air Flow	84 #/min (Fig. 3) (4 Air circuits)	42 #/min
OTI Protect	Yes (Fig. 3) Dummy load and Hall effect	Yes (Fig. 6)
Special features	Blower redundancy	Blower redundancy

Projected T_j (°C)	Min	Max	Avg	Allow	Min	Max	Avg	Allow
Micro	53	89	65	90	53	89	65	90
Power	77	118	85	120	77	118	85	120

FIGURE 1.
"B" ENCLOSURE

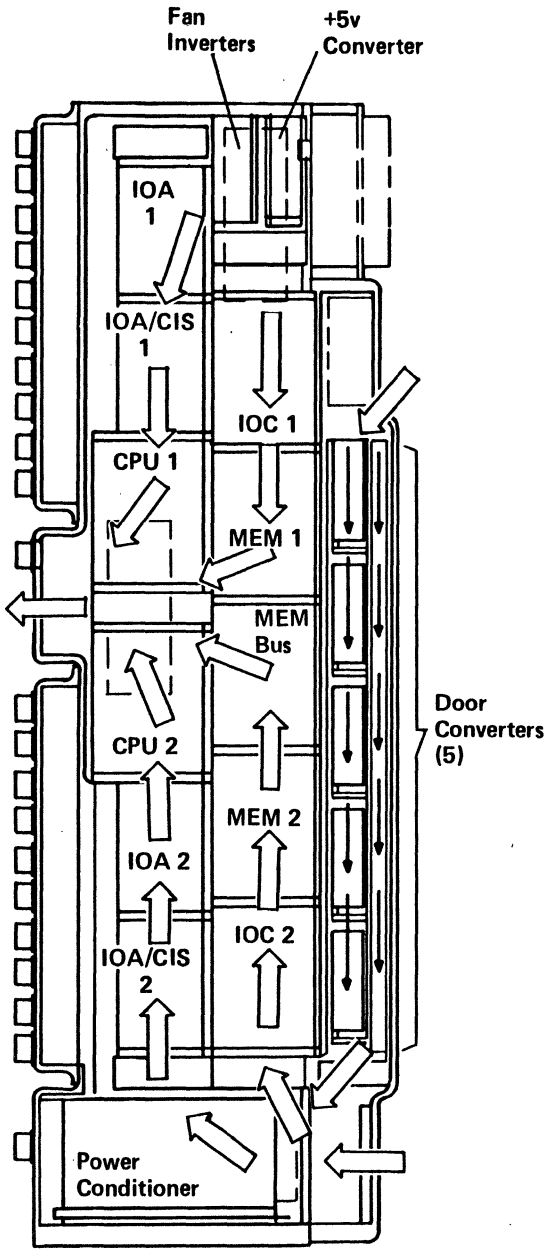


IBM

5065-47

FIGURE 2.

AN/UYK-43 AIR COOLED "B" ENCLOSURE COOLING CIRCUIT AND POWER SUMMARY

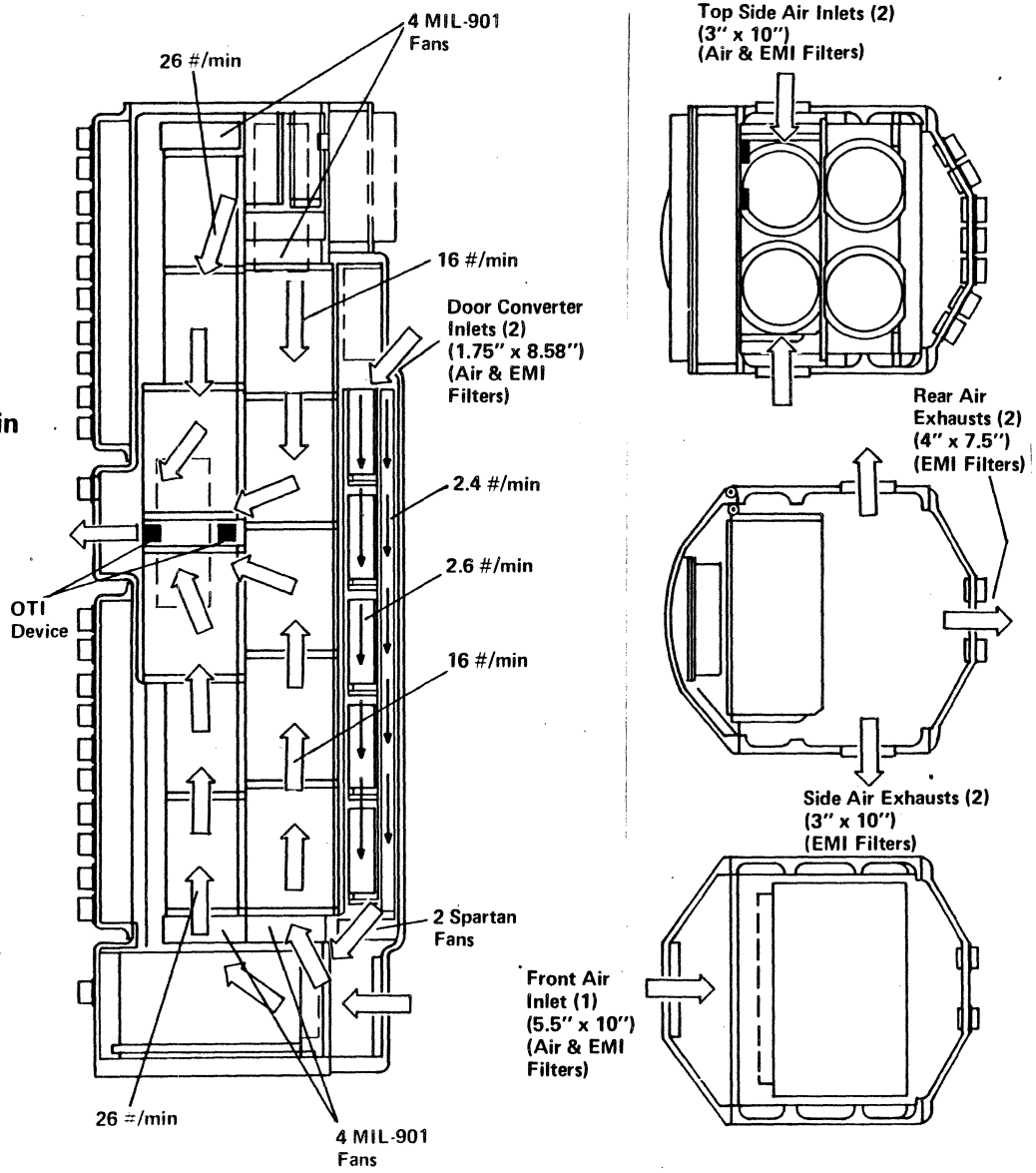


IOA 1	244 w
IOA/CIS 1	357 w
CPU 1	578 w
IOA/CIS 2	273 w
IOA 2	230 w
CPU 2	578 w
IOC 1	266 w
MEM 1	125 w
IOC 2	266 w
Power Conditioner	600 w
Door Converters	556 w
+5v Converter	75 w
Fans/Fan Inverters	778 w
P/TP	33 w
Total	5.5 kw

5065-48

FIGURE 3. AN/UYK-43 AIR COOLED "B" ENCLOSURE COOLING AIR FLOW

Total Cooling Air Flow Rate = 84 #/min



5065-49

FIGURE 4.
"A" ENCLOSURE

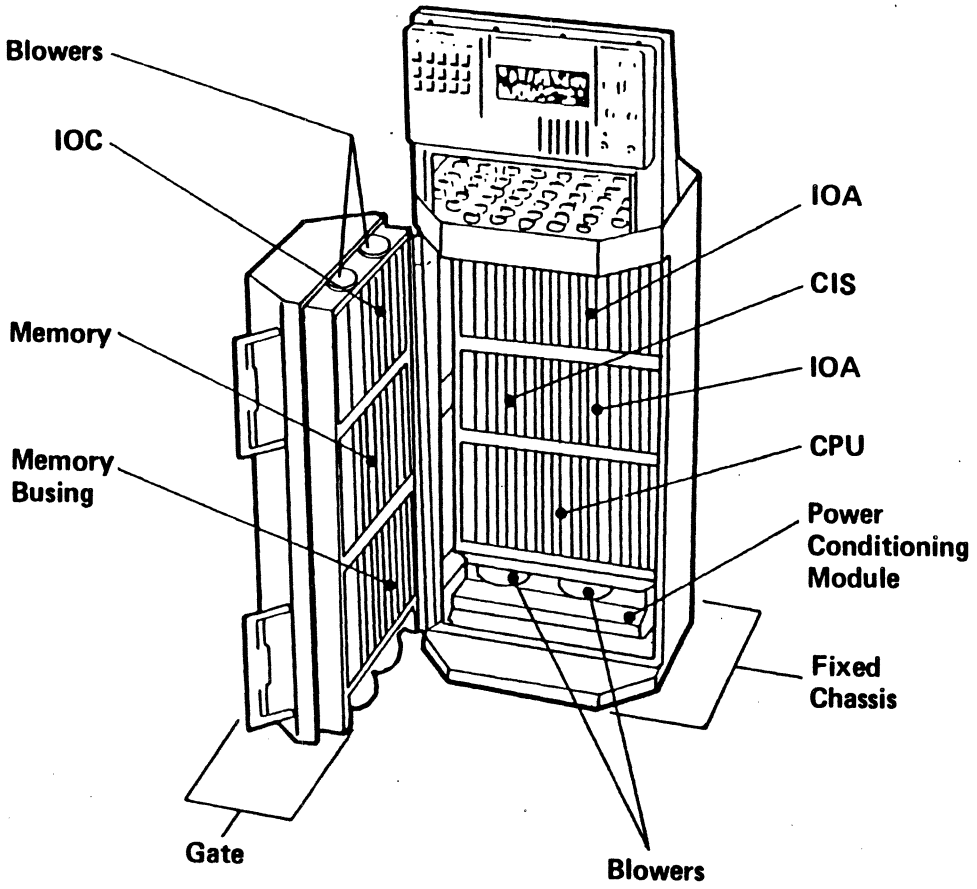
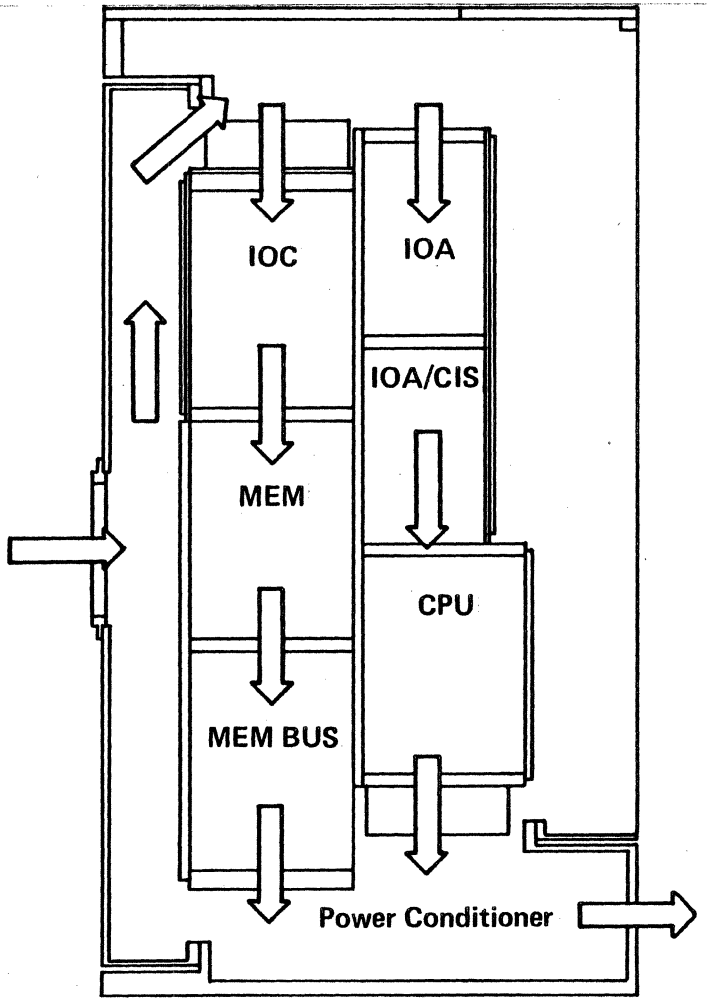


FIGURE 5.
AN/UYK-43 AIR COOLED "A" ENCLOSURE COOLING CIRCUIT AND POWER SUMMARY

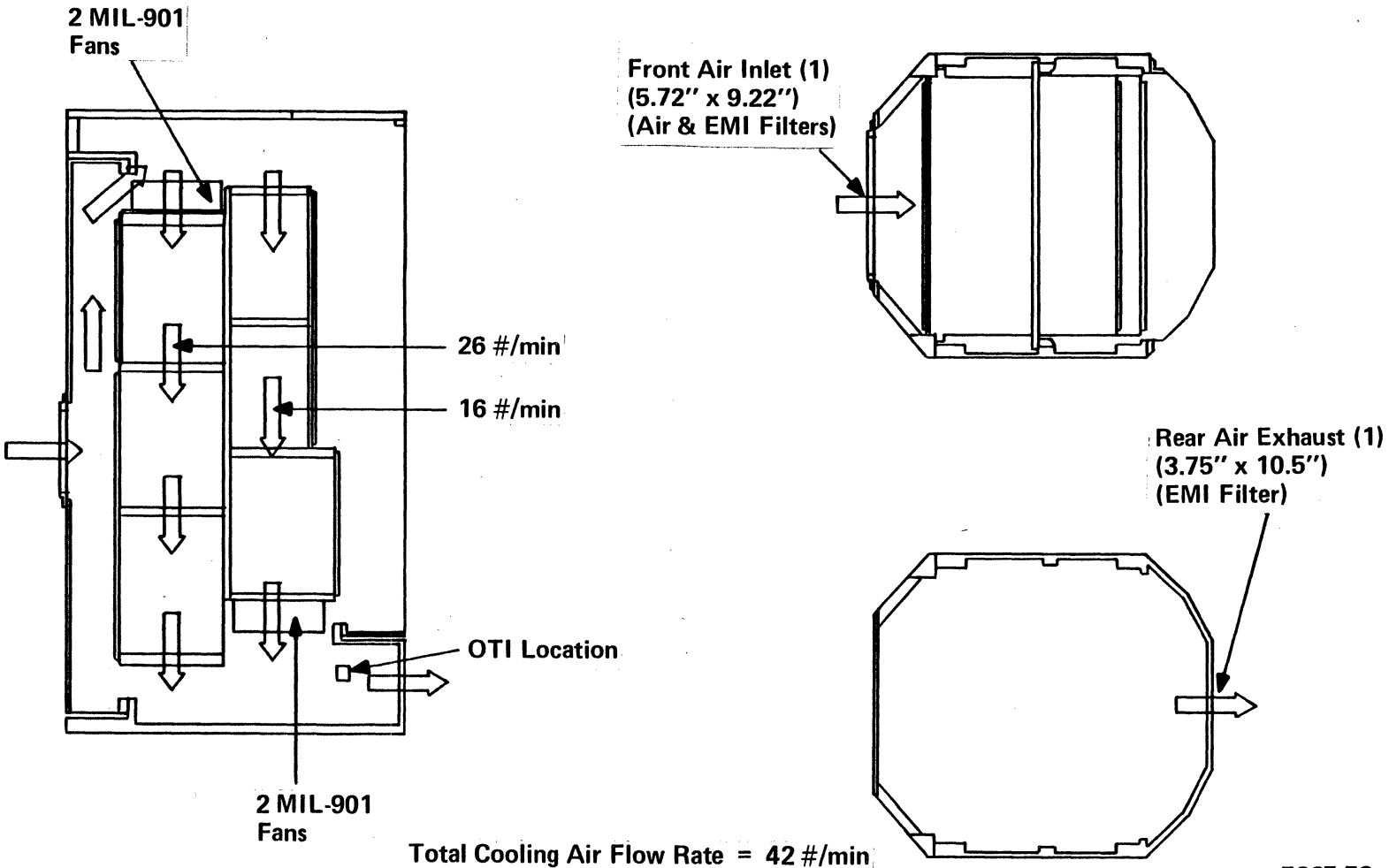


IOC	406 w
MEM	190 w
MEM BUS	383 w
IOA	229 w
IOA/CIS	339 w
CPU	578 w
Power Conditioner	180 w
Fans/Fan Inverters	333 w
P/TP	33 w
Total	2.7 kw

IBM

5065-51

FIGURE 6. AN/UYK-43 AIR COOLED "A" ENCLOSURE COOLING AIR FLOW



THERMAL DESIGN APPROACH LIQUID

- Method 2 Prefereable to Method 1 for IBM Electronics
  - Volume
  - Structureborne Noise
  - Acoustics Margin

- Conduction (Method 2)
- LRU Characterization (Conduction)
  - Material A1 vs Cu
  - Bonding
  - Component location
  - Power modules
  - Non-power modules
- LRU Mounting Interface
  - Power modules
  - Non-power modules
- θ j-c
- LRU Guidelines

IBM

System

- (A $\approx$ 1/2 B)
- Concept Finalized
- No Further Development Tests Planned (25 Years Conduction Experience)

Results:

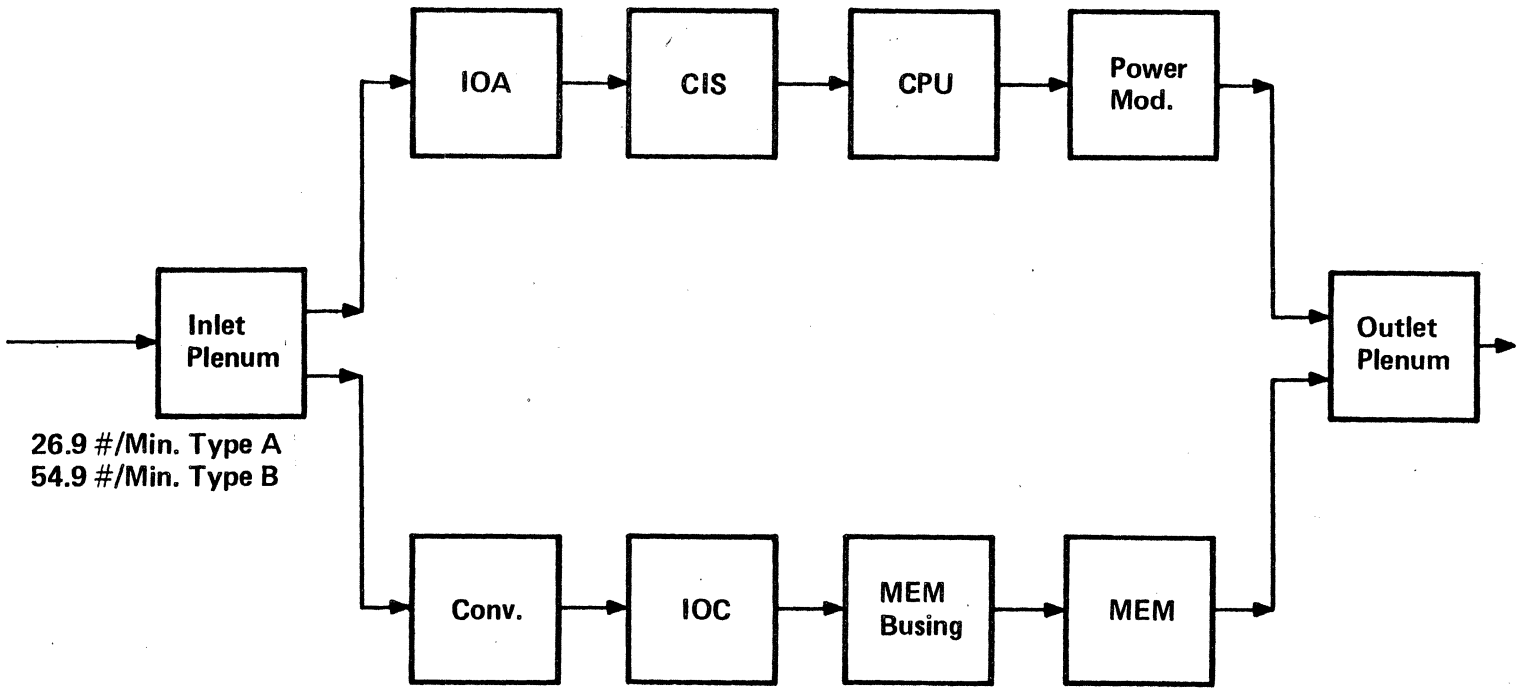
- High Confidence Level
- LRU Design Guides Issued

5065-53

COMPUTER THERMAL DESIGN DESCRIPTION

		Water Cooled	
		B	A
Illustration		Fig. 7	Fig. 7
Coolant/concept		Water/indirect (Fig. 8 & 9)	Water/indirect (Fig. 8 & 9)
Dissipation		4.7 kw (Fig. 10)	2.3 kw (Fig. 11)
Water inlet temp.		40°C	40°C
Water outlet temp		43°C	43°C
		ΔT = 3°C	ΔT = 3°C
Water flow (1.4 gal/min-kw)		54.9 #/min	26.9 #/min
OTI protect		yes (structure)	yes (structure)
		Min / Max / Avg / Allow	Min / Max / Avg / Allow
Projected temp T_j (°C)	Micro	53 / 79 / 61 / 80	53 / 79 / 61 / 80
	Power	56 / 98 / 77 / 120	56 / 98 / 77 / 120

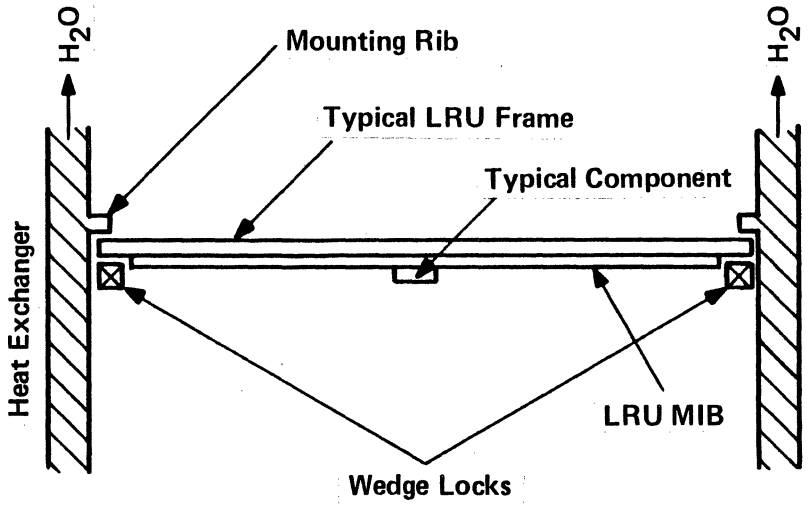
FIGURE 7.
WATER COOLED CABINET FLOW SCHEMATIC

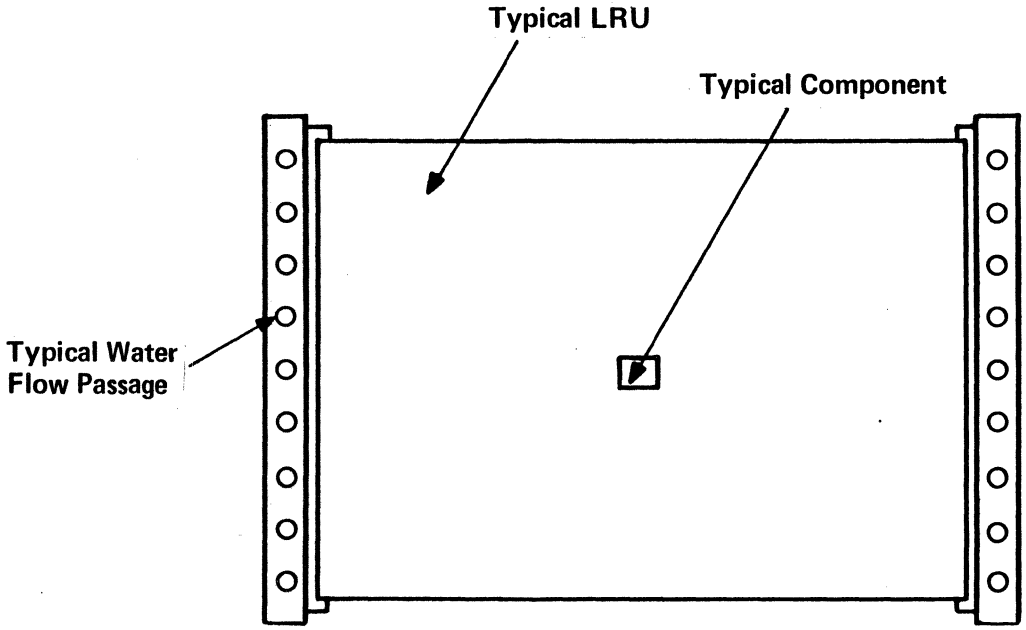


IBM

5065-55

FIGURE 8.
W/C HEAT EXCHANGER AND TYPICAL MOUNTING CONFIGURATION

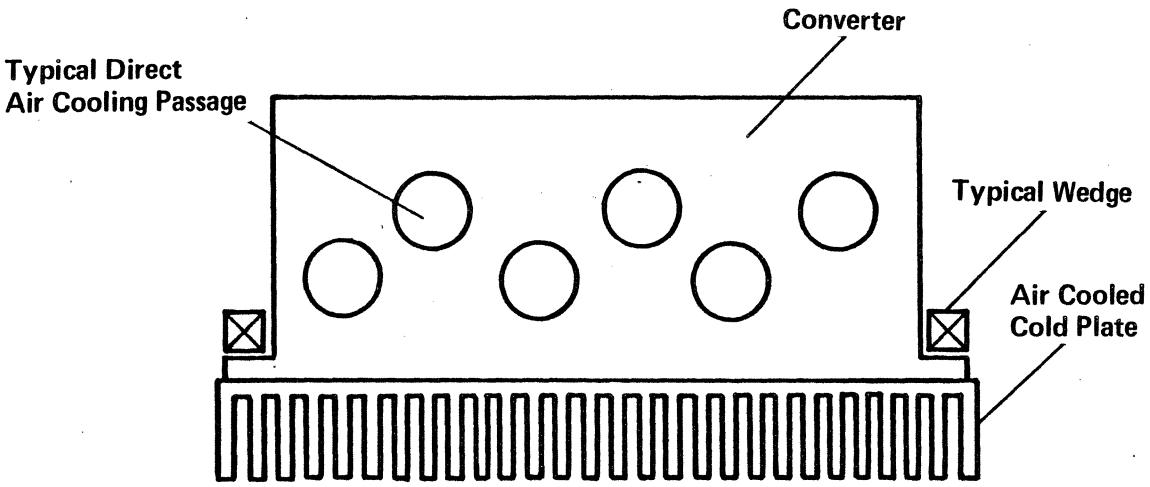




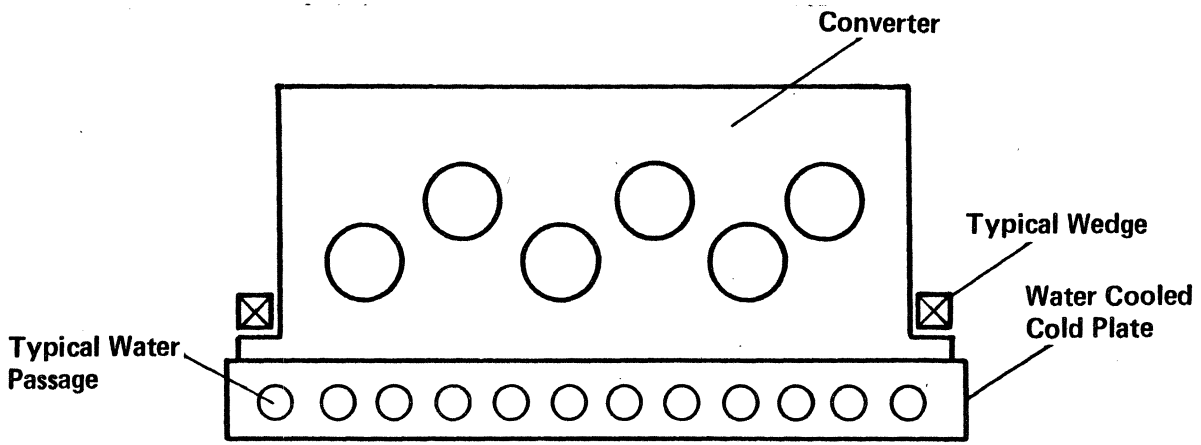
IBM

5065-56

FIGURE 9.
CONVERTER COOLING CONCEPT FOR AIR COOLED ENCLOSURES



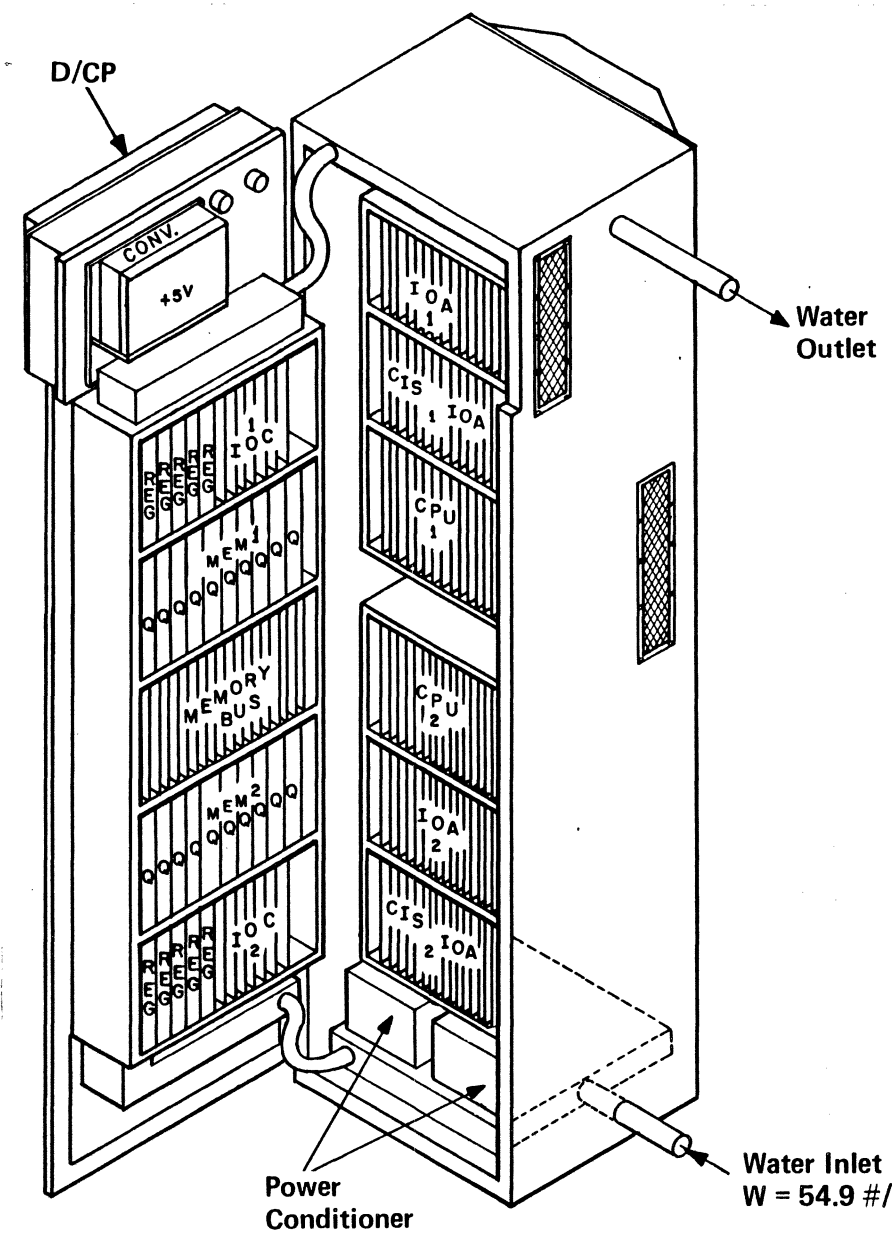
CONVERTER COOLING CONCEPT FOR WATER COOLED ENCLOSURES



IBM

5065-57

FIGURE 10.
AN/UYK-43 WATER COOLED "B" ENCLOSURE COOLING AND POWER SUMMARY

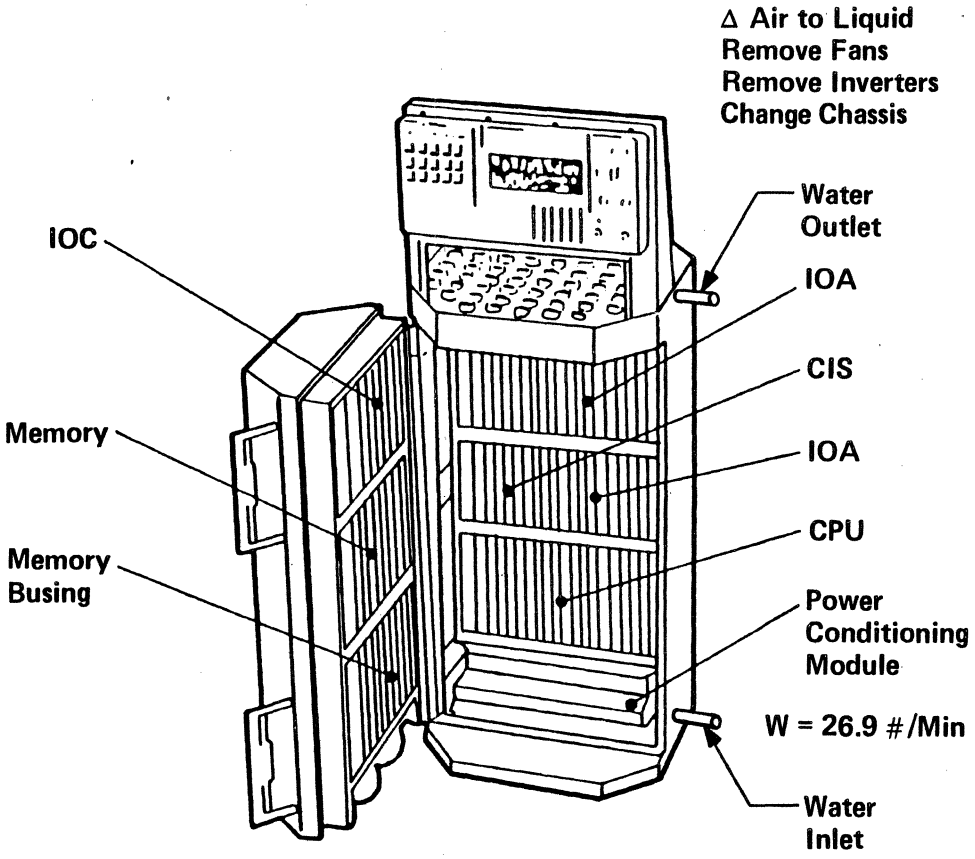


Power Summary	
IOA 1	244 w
IOA/CIS 1	357 w
CPU 1	578 w
IOA/CIS 2	273 w
IOA 2	230 w
CPU 2	578 w
IOC 1	266 w
MEM 1	125 w
MEM-BUS	385 w
MEM 2	125 w
IOC 2	266 w
Power Conditioner	600 w
Door Converters	556 w
+5 v Conv	75 w
P/TP	33 w
Total	4.7 kw

5065-58

FIGURE 11.

AN/UYK-43 WATER COOLED "A" ENCLOSURE COOLING AND POWER SUMMARY



Power Summary	
IOC	406 w
MEM	190 w
MEM BUS	383 w
IOA	229 w
IOA/CIS	339 w
CPU	578 w
Power Conditioner	180 w
P/TP	33 w
Total	2.3 kw

IBM

5065-59

CONCLUSION:

Thermal Design Meets Specification Requirements

WORST CASE ANALYSIS

WORST CASE ANALYSIS

- Methodology

  Component Circuit Analysis - Design evaluation

  Breadboard of Typical Component Application

  Test of Performance – Each circuit type thoroughly characterized for Worst Case performance

  - Function
  - Parametric
    - AC, delays, rise/fall time, etc.
    - DC, voltages, loading, etc.
  - Thermal environment
  - Voltage variation

  Design Automation Rules Established

  Physical Characterization

  Vendor Capability Evaluation

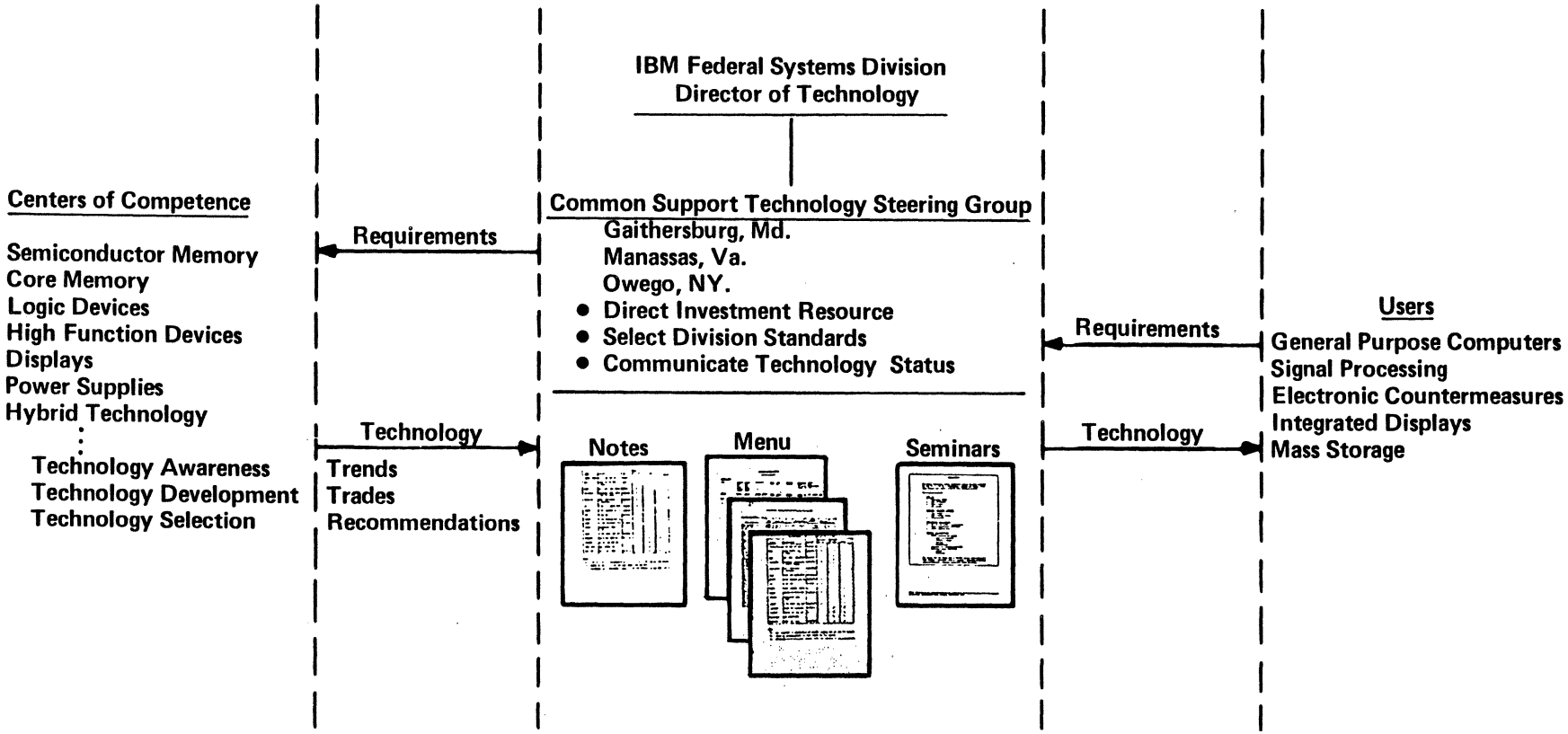
  Procurement Tests Specified

  Design Ground Rules – Derating, delay budgets, wiring

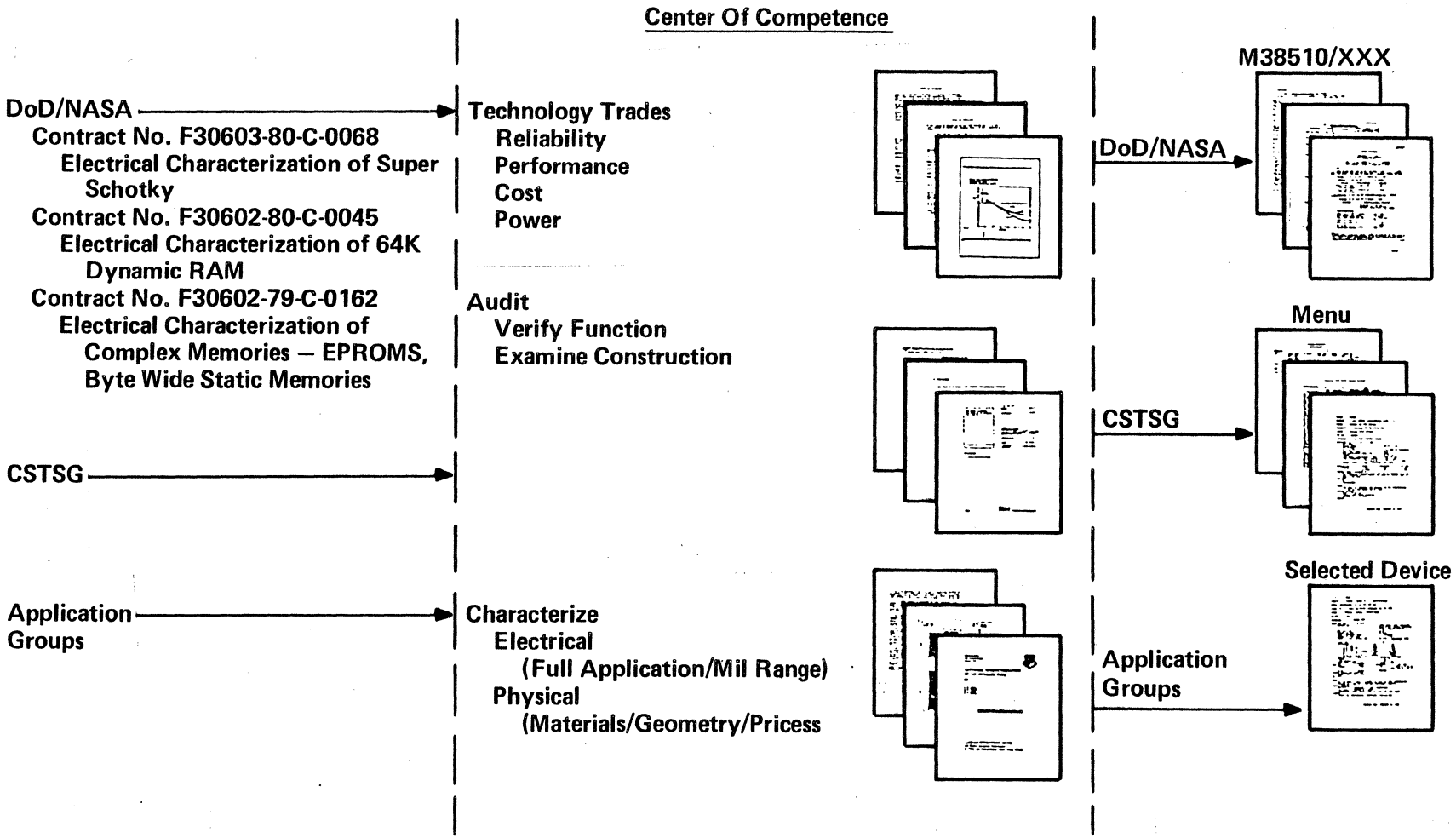
  Critical Path Timing Analysis

  Test of Critical Path

COMMON SUPPORT TECHNOLOGY STEERING GROUP



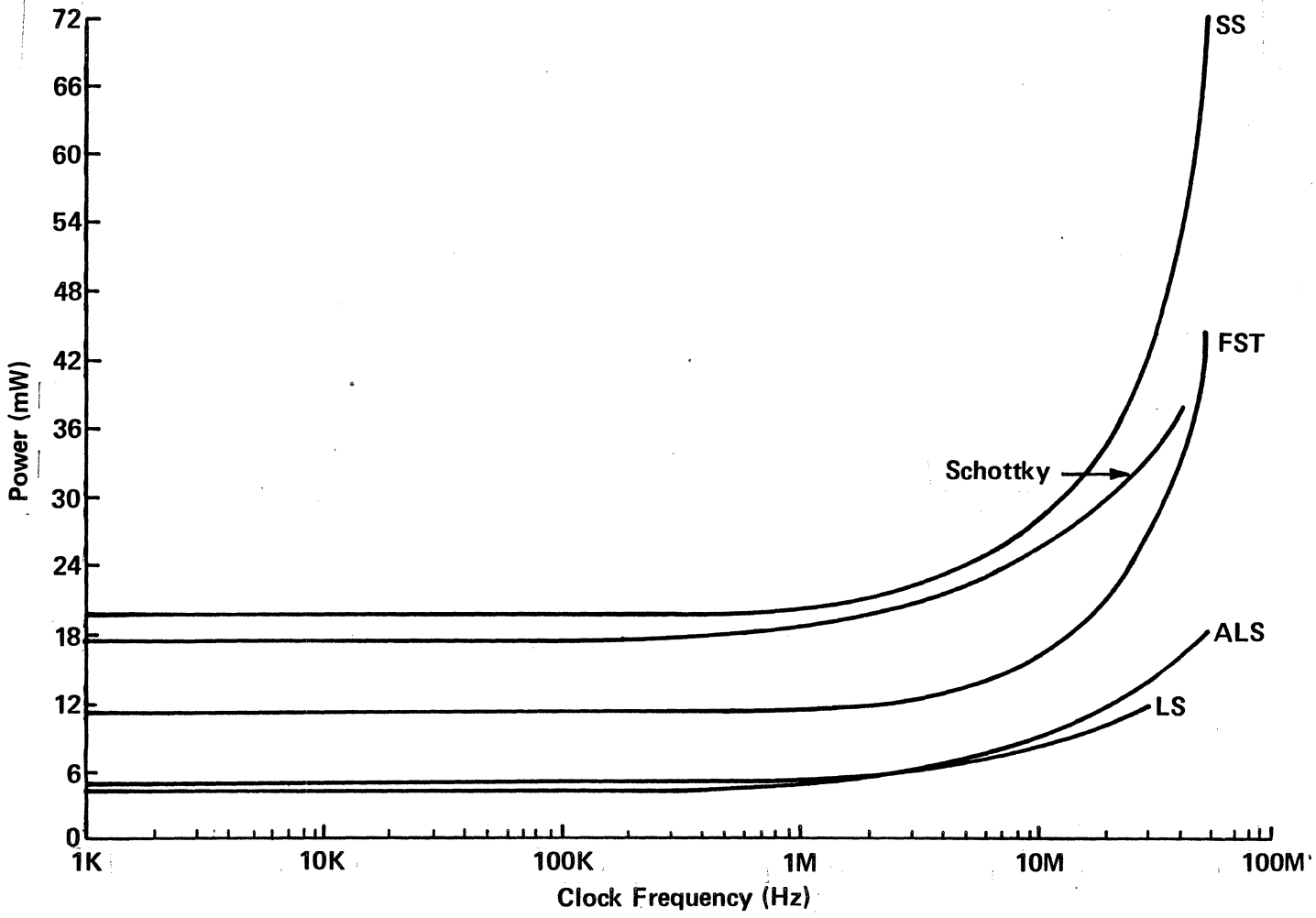
SELECTION METHODOLOGY



CHARACTERIZATION

- Intensive Technology Study
- Power vs Frequency
- All AC Paths
- Various Loading
  - Transmission line
  - CL
  - 3-State
- Input/Output DC Characteristics/Noise Immunity
- ICC Current Transitions (Decoupling)
- Pattern Sensitivity
- Shmoo Corners
- Instruction Sequence Sensitivity

CLOCK FREQUENCY vs POWER "74" D-FF



ELECTRICAL CHARACTERIZATION

AC Characterization

- Natural Circuit Thresholds Determined
- Combinatorial Circuits
  - TPD1, TPD0, TRISE, TFALL
    @ -55°C_J, 125°C_J, 25°C Amb.
    @V_{CC} = 4.5V, 5.0V, 5.5V
    @C_L = 50, 150, 250PF – Lumped Capacitive loads*
- Sequential Circuits
  - Propagation delays same conditions as above
  - Minimum pulse widths (clock, clear, preset)
  - Set-up's and hold times
  - FMAX
- Data Reduction and Analysis
  - Averages, maximum, minimum, ranges computed and tabulated
  - Histograms, plots, can be obtained
  - Composite plots comparing several vendors can be obtained
  - Average of slowest vendor used to determine production test limits.

*On Fast and ALS loads are C = 50 PF and 30Ω unterminated coax. line.

ELECTRICAL CHARACTERIZATION (CONT)

D C CHARACTERIZATION

- Static Parameters Evaluated by X-Y Plots of Impedance and Transfer Characteristics. @-55°C_J, 125°C_J and 25°C Ambient a V_{CC} = 4.5 or 5.5V.
  - I_{IN} vs V_{IN}
  - I_{OUT} vs V_{OUT}
  - I_{CC} vs V_{CC}
  - V_{OUT} vs V_{IN}
- Other Test Capability
  - $BI_{IN}(1)$ – Input breakdown
  - V_{CLAMP} – Schottky clamp voltage
  - BI_{OUT} – Output breakdown
  - BOZL – Tri-state leakage (0)
  - BOZH – Tri-state leakage (1)

FAST THRESHOLD SUMMARY

		-55°C	25°C	125°C
54F00	TR	2.0V	2.0V	1.7V
	TF	1.5V	1.2V	0.8V
54F02	TR	2.1V	2.0V	1.8V
	TF	1.5V	1.4V	1.0V
54F32	TR	1.9V	1.6V	1.3V
	TF	1.7V	1.4V	1.0V
Threshold	TR	1.5V	1.5V	1.5V
Chosen	TF	1.5V	1.5V	1.5V

CIRCUIT TYPE FAIRCHILD 54F04

Delay Path — Load 50 PF — 5.0 Volts

	Minimum			Average			Maximum		
	-55°C	25°C	125°C	-55°C	25°C	125°C	-55°C	25°C	125°C
1A-1Y TPD0(50PF)	3.4	3.1	2.8	3.5	3.2	2.8	3.6	3.3	2.9
1A-1Y TPD1(50PF)	3.2	3.4	3.9	3.4	3.6	4.2	3.6	3.7	4.4
3A-3Y TPD0(150PF)	5.6	5.0	4.6	6.0	5.2	4.8	6.4	5.4	4.9
3A-3Y TPD1(150PF)	5.3	5.4	5.9	6.0	6.2	6.7	7.8	7.5	8.0
6A-6Y TPD0(250PF)	8.2	7.7	6.9	8.7	7.9	7.3	9.3	8.3	7.5
6A-6Y TPD1(250PF)	7.6	7.7	8.5	8.8	9.2	9.6	10.5	10.4	11.1
TFALL-1Y(90./.-TH)	2.0	1.9	2.0	2.1	2.0	2.1	2.3	2.2	2.1
TRISE-1Y(.3-TH)	1.7	1.6	1.7	1.8	1.8	1.9	2.0	1.9	2.1

REVISIONS

CHK	ENGRG NOTICE	LTR	DESCRIPTION	DATE	APPROVED
..	66298LH	-	RELEASE PRELIMINARY 576	12-12-80	J.A. Simicek

BLKR	BHC	PKG-PINS= FP-20 PEUR = 0HZ TYPE NO.	PART NO.	PKG-PINS = PEUR = TYPE NO.	PART NO.	MFR.
DTM3						FAIRCHILD
	L					
	S					
	F	54F521	6134557			

1. PERCENT TESTABLE _____

2. NON-STANDARD ABBREVIATIONS AND SYMBOLS:
   A) ZERO = Ø, AND ONE = 1
   B) BLKR = BLOCK RULE, BHC = BLOCK HARDWARE CODE, BRC = BLOCK REPRESENTATION CODE, PEUR = PHYSICAL ELEMENTARY UNIT RULE, FP = FLATPACK, DIP = DUAL-IN-LINE PKG, TBA = TO BE ASSIGNED.

3. LINE TWO (2) OF THE LOGIC BLOCK REPRESENTATION CONTAINS: BLKR (4 CHARACTERS), BHC (1 CHARACTER), AND BRC (1 CHARACTER).

   BHC CODES: BLANK = STANDARD SPEED
   L = LOW POWER SCHOTTKY
   S = SCHOTTKY
   F = FAIRCHILD FAST
   H = HIGH SPEED
   P = LOW POWER

–				
4	5	6	7	8
REV	–	–	–	
SH	1	2	3	

REV STATUS OF SHEETS

CONTR NO
PREPARED BY P. SAWYER 12/80
DSGN CHK
DWG CHK
DSGN APPROVAL
OTHER APPROVAL (PLEASE ACTIVITY)

IBM FEDERAL SYSTEMS DIVISION
☐ GAITHERSBURG, MD ☒ OWEGO, N Y ☐ HUNTSVILLE, AL ☐ MANASSAS, VA

TITLE
8-BIT IDENTITY COMPARATOR

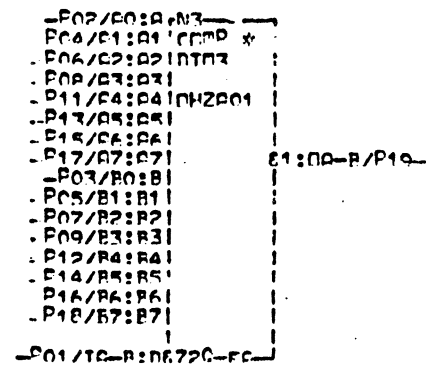
SIZE	CODE IDENT NO	DWG NO
A	03640	6189940

NEXT ASSY NONE | WT | SHEET 1 OF 4

NOTES CONTINUED FROM SHEET 1

4. P20 - VCC P10 - GND

SIZE	FSCM NO.	DWG NO.
A	03640	6189940
SCALE NONE	REV -	SHEET 2



LOADING DATA FOR DTM3 DRIVE/LOAD IS IN MILLIAMPS

PEUR OHZ - FP		BHC _				
DOT FUNC	LOGPIN	LOAD	LOAD	LOAD	LOAD	
	A0	0.6				
	A1	0.6				
	A2	0.6				
	A3	0.6				
	A4	0.6				
	A5	0.6				
	A6	0.6				
	A7	0.6				
	B0	0.6				
	B1	0.6				
	B2	0.6				
	B3	0.6				
	B4	0.6				
	B5	0.6				
	B6	0.6				
	B7	0.6				
	D0	0.6				
	10	20.0				

SIZE A	FSCM NO. 03640	DWG NO. 6189940
SCALE NONE	REV -	SHEET 4

HM200CT40__+L UPLEVEL HMB-2

DRIVERS	BTR/HC	MA	TOTAL	LOADS	BTR/HC	MA	TOTAL
HM200CT40	DQA4/F	20.00		HM252EBK0	DRV0/F	0.60	
				HM252EBJ0	DRV0/F	0.60	
				HM252EBI0	DRV0/F	0.60	
				HM252EBH0	DRV0/F	0.60	
				HM252EAK0	DRV0/F	0.60	
				HM252EAJ0	DRV0/F	0.60	
				HM252EAI0	DRV0/F	0.60	
				HM252EAH0	DRV0/F	0.60	
				HM232BDB0	DRN6/F	0.60	
				HM232BCB0	DRN6/F	0.60	
				HM216DCB0	DRN6/F	0.60	
				HM216DBB0	DRN6/F	0.60	
				HM215BBB0	DRN6/F	0.60	
				HM210DBB0	DRN6/F	0.60	
				HM210DAB0	DRN6/F	0.60	
				HM210BBB0	DRN6/F	0.60	
				HM210BAB0	DRN6/F	0.60	
				HM203ABB0	DRN6/F	0.60	
				HM203AAB0	DRN6/F	0.60	
		20.0		HM202EBB0	DRN6/F	0.60	12.0

HM200CW40__+L UPLEVEL HMB-3

DRIVERS	BTR/HC	MA	TOTAL	LOADS	BTR/HC	MA	TOTAL
HM200CW40	DQA4/F	20.00		HM252ECB0	DRN6/F	0.60	
				HM232BDC0	DRN6/F	0.60	
				HM232BCC0	DRN6/F	0.60	
				HM230BAC0	DRN6/F	0.60	
				HM222BAB0	DRN6/F	0.60	
				HM221CBE0	DRN6/F	0.60	
				HM221CAE0	DRN6/F	0.60	
				HM210BBC0	DRN6/F	0.60	
				HM210BAC0	DRN6/F	0.60	
				HM204ABA0	DSQ1/L	0.40	
				HM204AAA0	DSQ1/L	0.40	
				HM203DNB0	DRN6/F	0.60	
				HM203DBB0	DRN6/F	0.60	
				HM203BBC0	DRN6/F	0.60	
				HM203ABC0	DRN6/F	0.60	
		20.0		HM203AAC0	DRN6/F	0.60	9.2

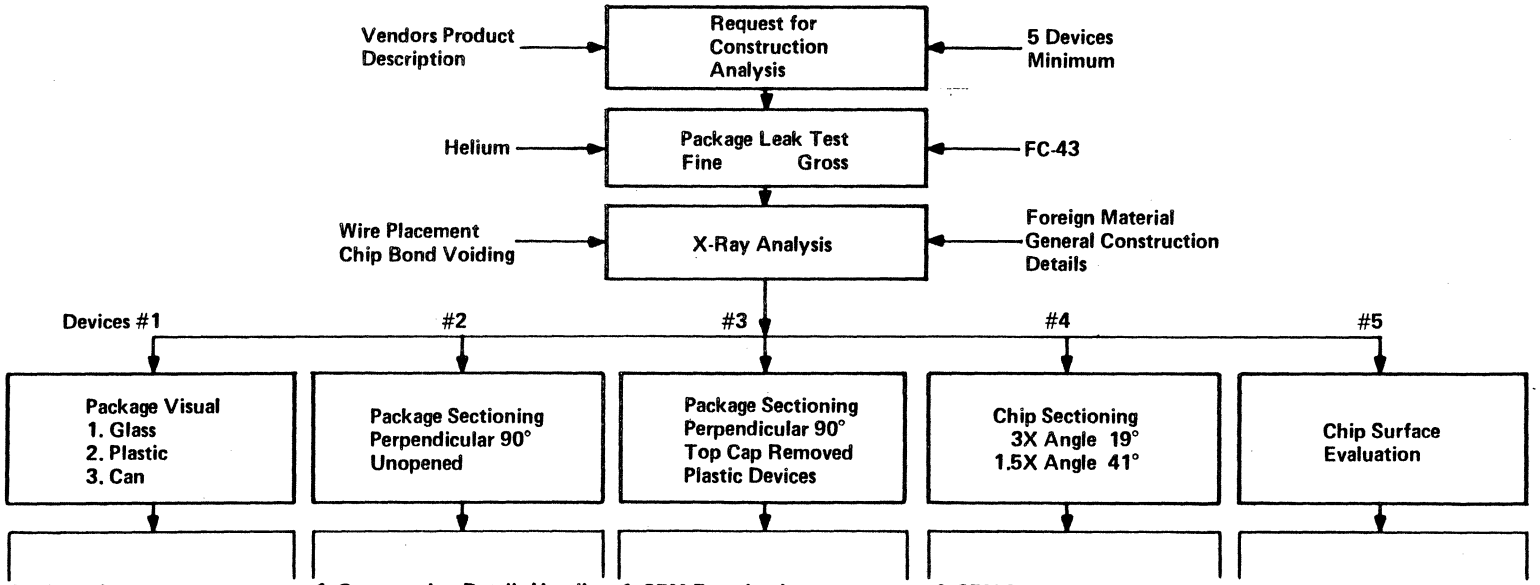
WHAT IS PHYSICAL CHARACTERIZATION

- Destructive Disassembly To Define
- Physical Structure and Processes
  - Horizontal
  - Vertical
  - Package
  - Materials
  - Bonding

PURPOSES OF PHYSICAL CHARACTERIZATION

- Expose Potential Problems
  - Design
  - Process
  - Producibility
  - Quality
  - Reliability
- Establish Construction Baseline
  - Monitor of vendor changes
  - Vendor comparisons

GENERAL CONSTRUCTION ANALYSIS OUTLINE



1. Dimensions
   Lead-Package
   Width-Height
   Length, etc.
2. Identification
   Paint Integrity
   Proper Identification
3. Plating Uniformity
4. Electrical - Curve Tracer of BV_{EBO}, BV_{CEO}, VF_{EBO}, VF_{CEO} Retain Sample
5. Photographs

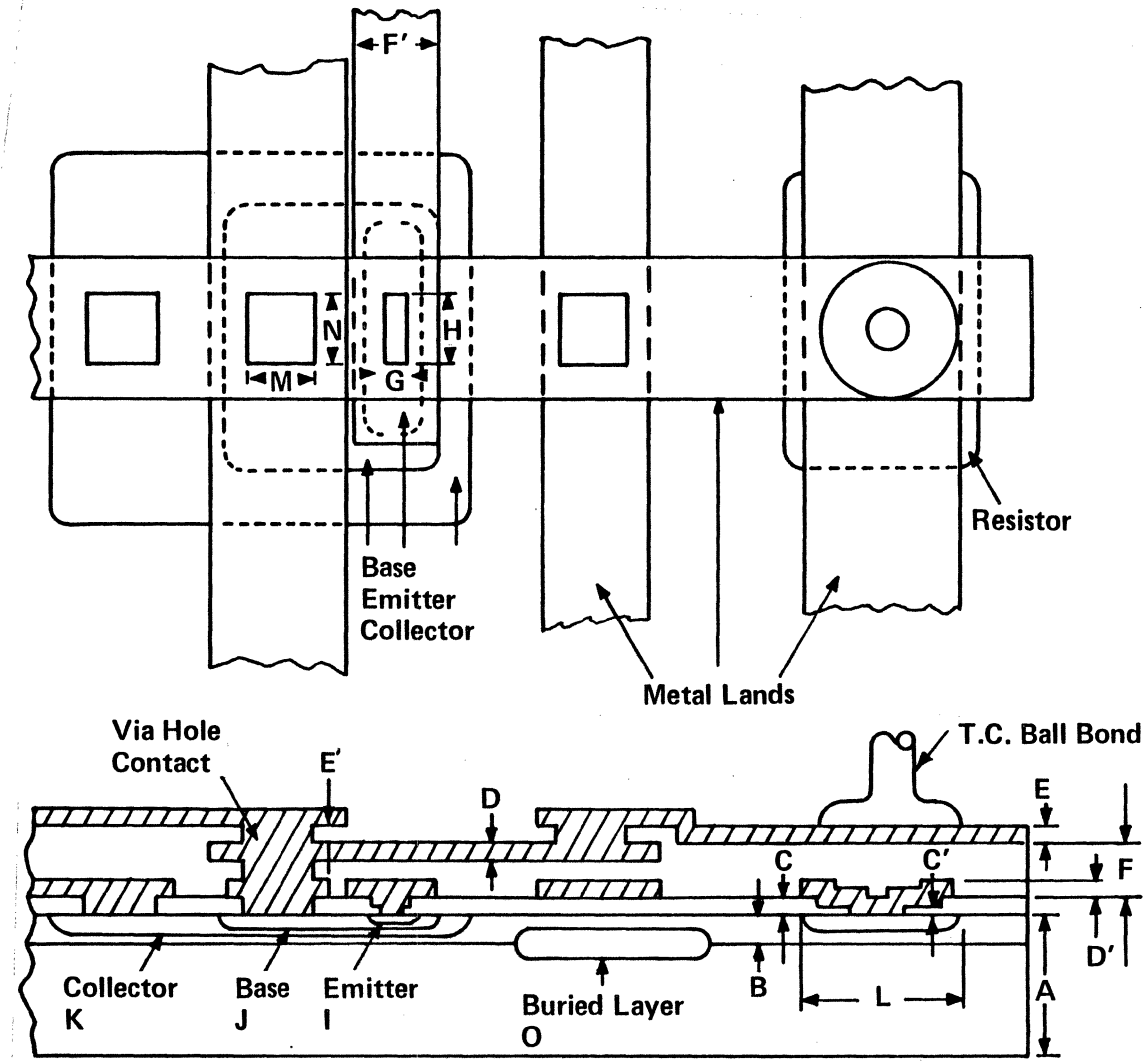
1. Construction Details-Usually Mid-Way in Package Photograph Anomalies
2. Microprobe
   Materials Identification
3. Measurements:
   Chip Height
   Chip Bond to Header
   Wire Bond Diameter
   Wire Diameter
   Glass to Metal
   Die Bond Voiding
4. Photographs

1. SEM Examination
   Chip-Contact Areas
   Chip to Header Bond
   Wire Bond
2. Photograph Cavity
   Chip
   Bond
   Anomalies
3. Pull Test-Optional
   Wire Bond Integrity
   Photograph
4. Encapsulated
   Die Bond Voiding
5. Photographs

1. SEM Examination
   Chip-Contact Areas
   Chip to Header Bond
   Wire Bond
2. Pull Test
   Wire Bond Integrity
   Photograph Anomalies
   Leave 1 or 2 Wires Unpulled
3. Chip Removal - Hot Plate
4. Encapsulated
   Overlay
   Stripe Metal
   Passivation
   Junctions
5. Photographs

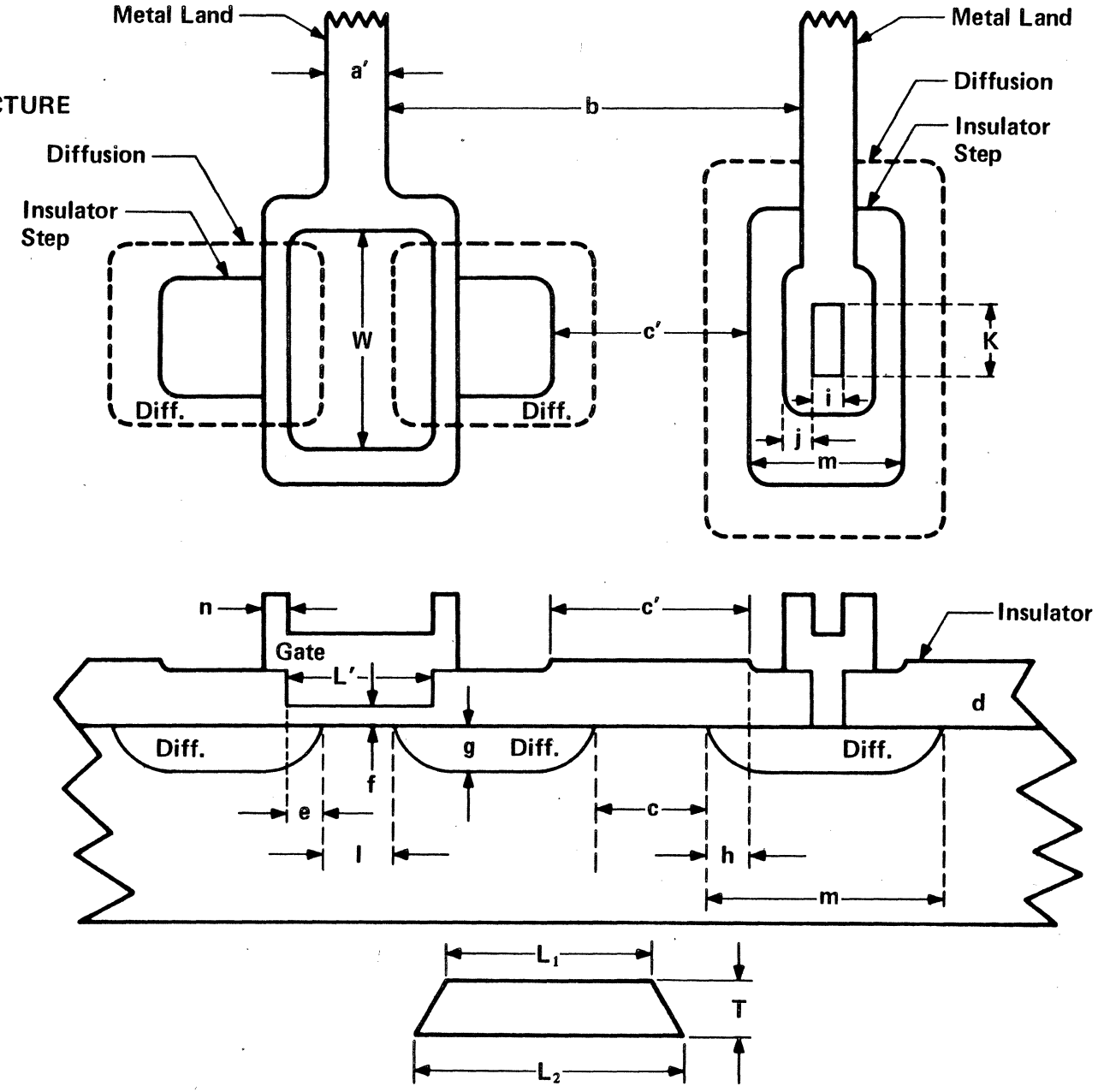
1. Pull Test
   Wire Bond Integrity
2. Grain Size
3. Overlay Removal
4. Aluminum Removal
5. Pin Hole Test
   and/or
   Passivation Removal for Junction Top Staining of all Diffusions
6. Photograph

MULTILAYER METALIZATION STRUCTURE
SKETCH-1



5065-60-19

TYPICAL MOS STRUCTURE



WIRING RULES FOR FAST CIRCUITS

- All Wiring Including Connections to Test Points Shall be Point to Point (Daisy Chain). The Distribution of Clock Signals to Pages Along the Back Panel is the Exception.

- These Rules Apply for $-55°C \leq T_J \leq 125°C$, $V_{CC} = 5V \pm 0.25$ V and Z0 of Page MIB Signal Lines = Z0 of Back Panel MIB Signal Lines. Z0 of These Signal Lines $\geq 30\ \Omega$.

WIRING RULES FOR FAST CIRCUITS (CONT)

- Noise Sensitive Circuits
  - If the output of a 54FXX circuit cannot be allowed to cross the threshold more than once during a change of state, that circuit must be located within six inches from the end of the signal line driven by a single fast circuit.
  - Fast circuits which can tolerate multiple threshold crossings during changes of state can be located anywhere along a signal line driven by a single fast circuit.
- All Random Logic
  - On any wiring net driven by a single fast circuit. The fast circuit nearest the driver will be the last to switch at -55°C. There will be some higher temperature (varies depending on driver sink) above which the fast circuit closest to the driver will be the first to switch for falling inputs. At some different higher temperature, this circuit could also be the first to switch for a rising input.
  - To ensure that the fast circuit closest to the driver always is the first to switch and to eliminate all restrictions on the placement of the fast circuits along the net, use two paralleled 54F244 circuits in the same package or four paralleled 54FXX gate circuits in the same package (54F00, 54F02, 54F04, 54F08, or 54F32) as the net driver. These common package circuits should be wired in parallel with the shortest wires possible.

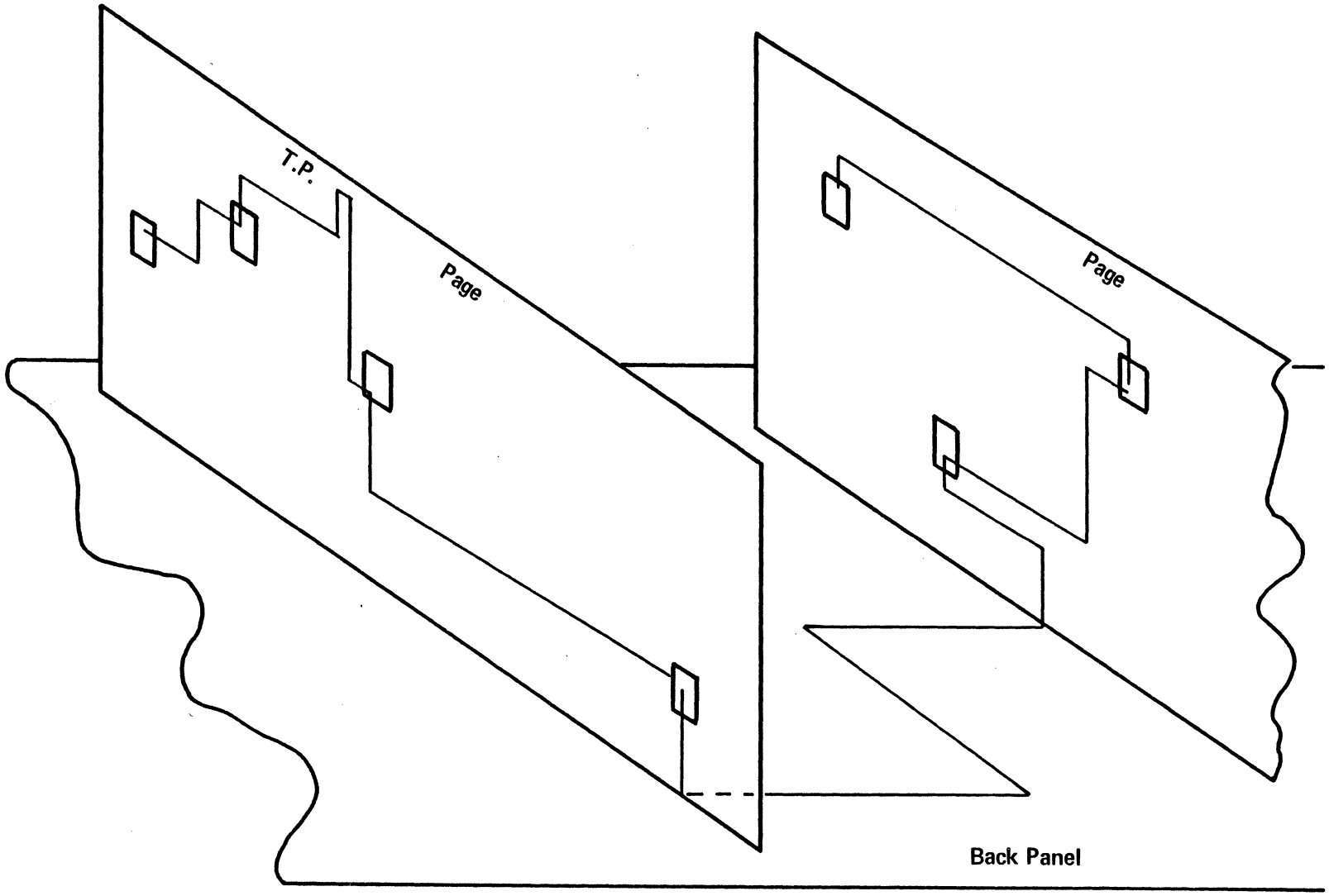
WIRING RULES FOR FAST CIRCUITS (CONT)

- Clock Signals
  - Clock signals can be distributed to as many pages along the back panel as desired.
  - If the page containing a clock signal buffer is located at the end of the back panel, there is no restriction on the location of the buffer on the page. The buffer can also drive fast circuits located on the same page MIB as the buffer.
  - If the page containing a clock signal buffer is not located at the end of the back panel. The buffer must be placed in the bottom row of circuits and wired to a connector pin with the shortest wire possible.
  - The clock signal buffer shall consist of two of the circuits in a 54F244 packaged wired in parallel with the shortest nets possible if it is on a page located at the end of the back panel. Four circuits in a 54FXX gate package (54F00, 54F02, 54F04, 54F08, or 54F32) can be substituted for two circuits in a 54F244 package.
  - The clock signal buffer shall consist of four of the circuits in a 54F244 package wired in parallel with the shortest nets possible if it is on a page located anywhere but at the end of the back panel.

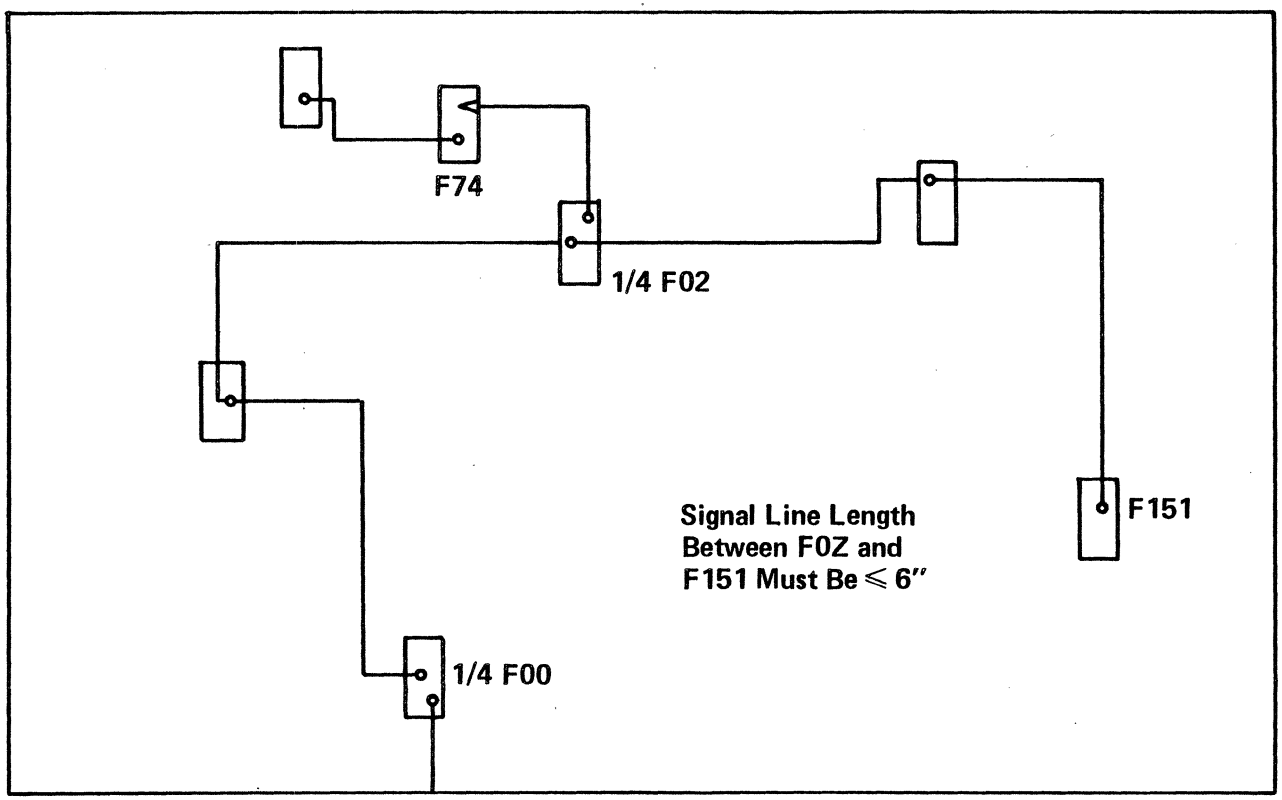
WIRING RULES FOR FAST CIRCUITS (CONT)

- Clock Signals (Continued)
  - Clock signal receivers shall be located in the bottom rows of circuits on the pages and wired to the connector pins with the shortest wires possible.
  - If a clock signal receiver drives only clock inputs of clocked circuits (54F74, 54F161, 54F175, 54F194 and 54F374) the following rules apply:
    - The receiver can be any appropriate fast gate (i.e. inverting or non-inverting) and can drive any number of clocked circuits within its fan out limit. No clocked circuit can be located more than two feet from the end of the signal line. The clocked circuit closest to the receiver will be the last to switch at -55°C. It could be the first to switch to some higher temperature.
    - The receiver shall consist of two circuits in a 54F244 package wired in parallel or four circuits in any 54FXX gate package (54F00, 54F02, 54F04, 54F08 or 54F32) wired in parallel if it is desired that the clocked circuit closest to the receiver switch first and not be restricted to being placed within two feet from the end of the signal line. The paralleled circuits must be wired with the shortest nets possible.
  - If a clock signal receiver drives a gate used to invert the clock signal, that gate must be located within six inches from the end of the signal line.
  - The clock pulse width in nsec must be $\geq$ ten times the length in feet of the signal line from the clock signal buffer to the furthest receiver.

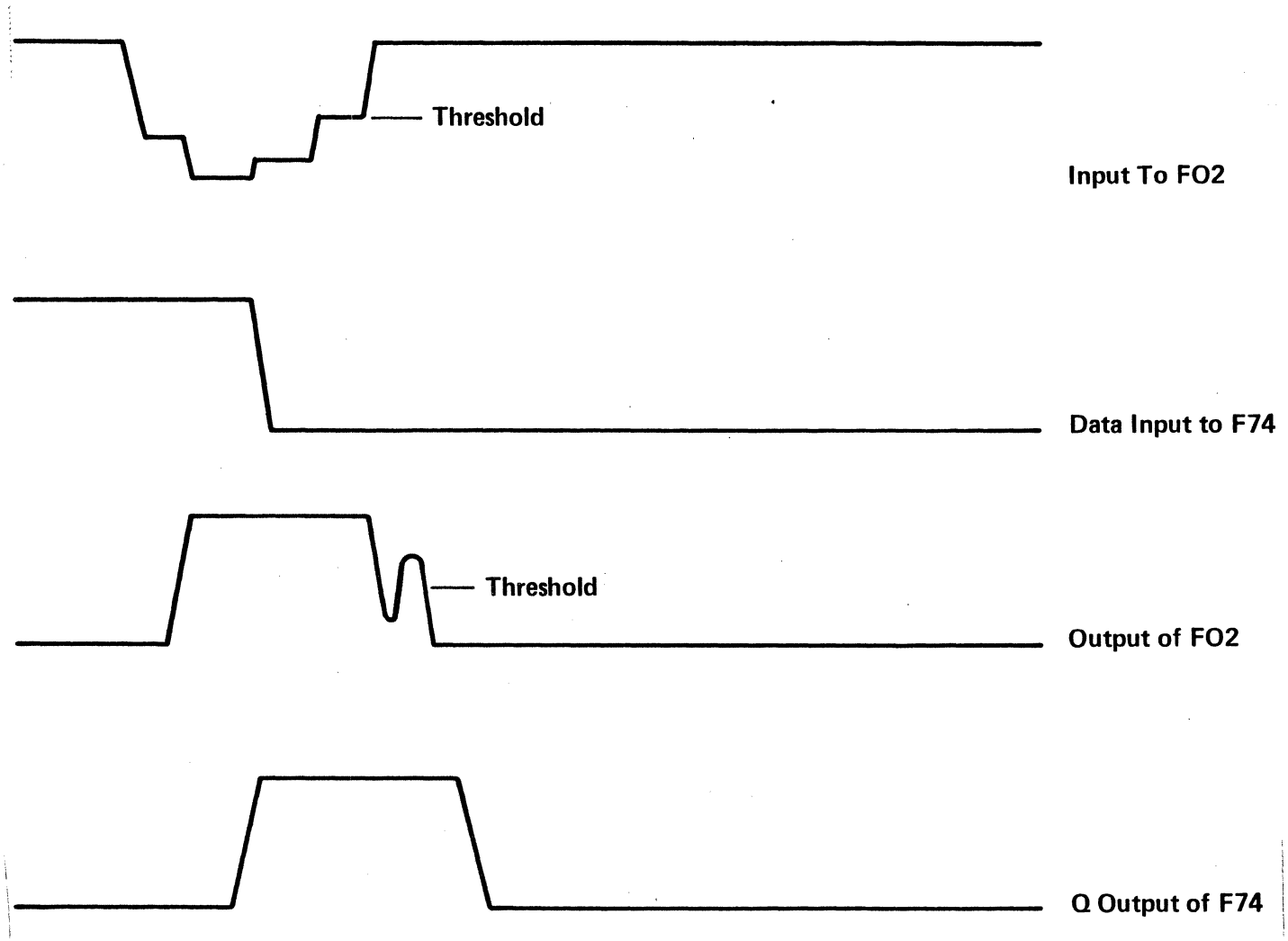
POINT TO POINT (DAISY CHAIN) WIRING

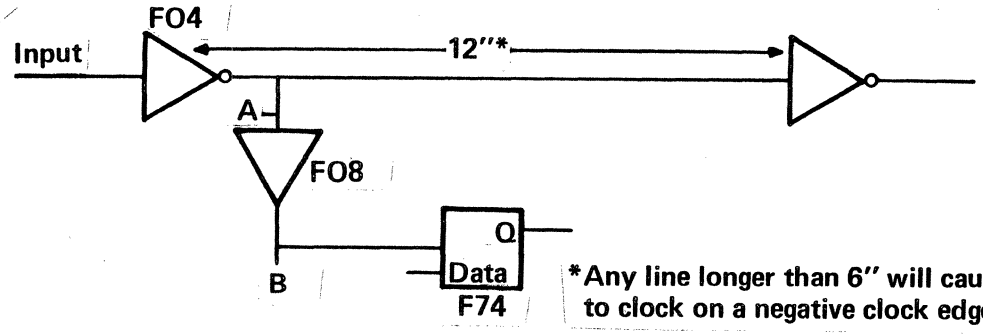


NOISE SENSITIVE FAST CIRCUIT LOCATION

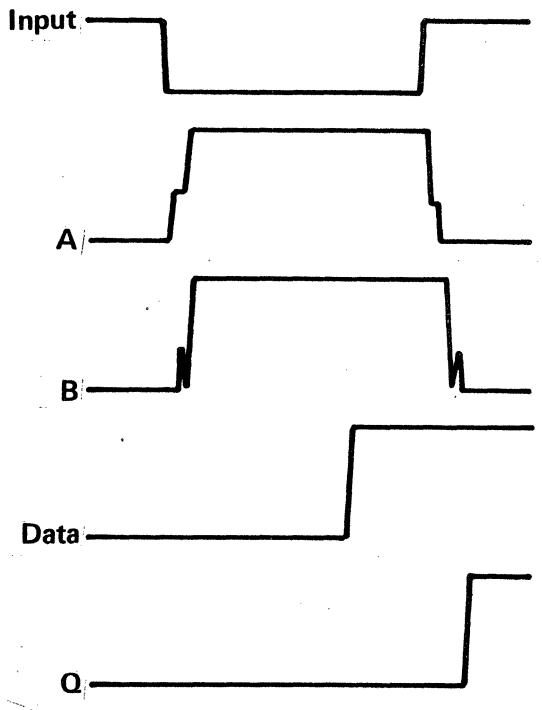


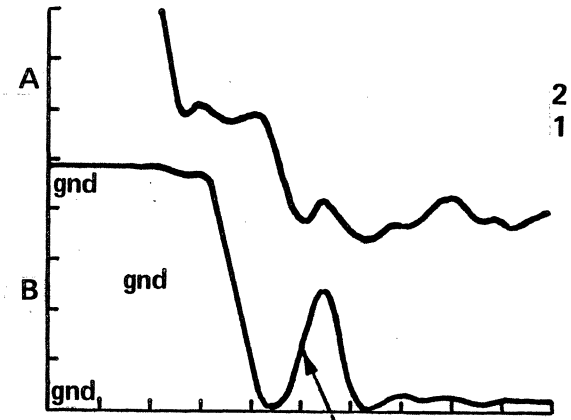
FALSE CLOCKING OF F74 IF 6" RULE IS VIOLATED





*Any line longer than 6" will cause the flip flop to clock on a negative clock edge.

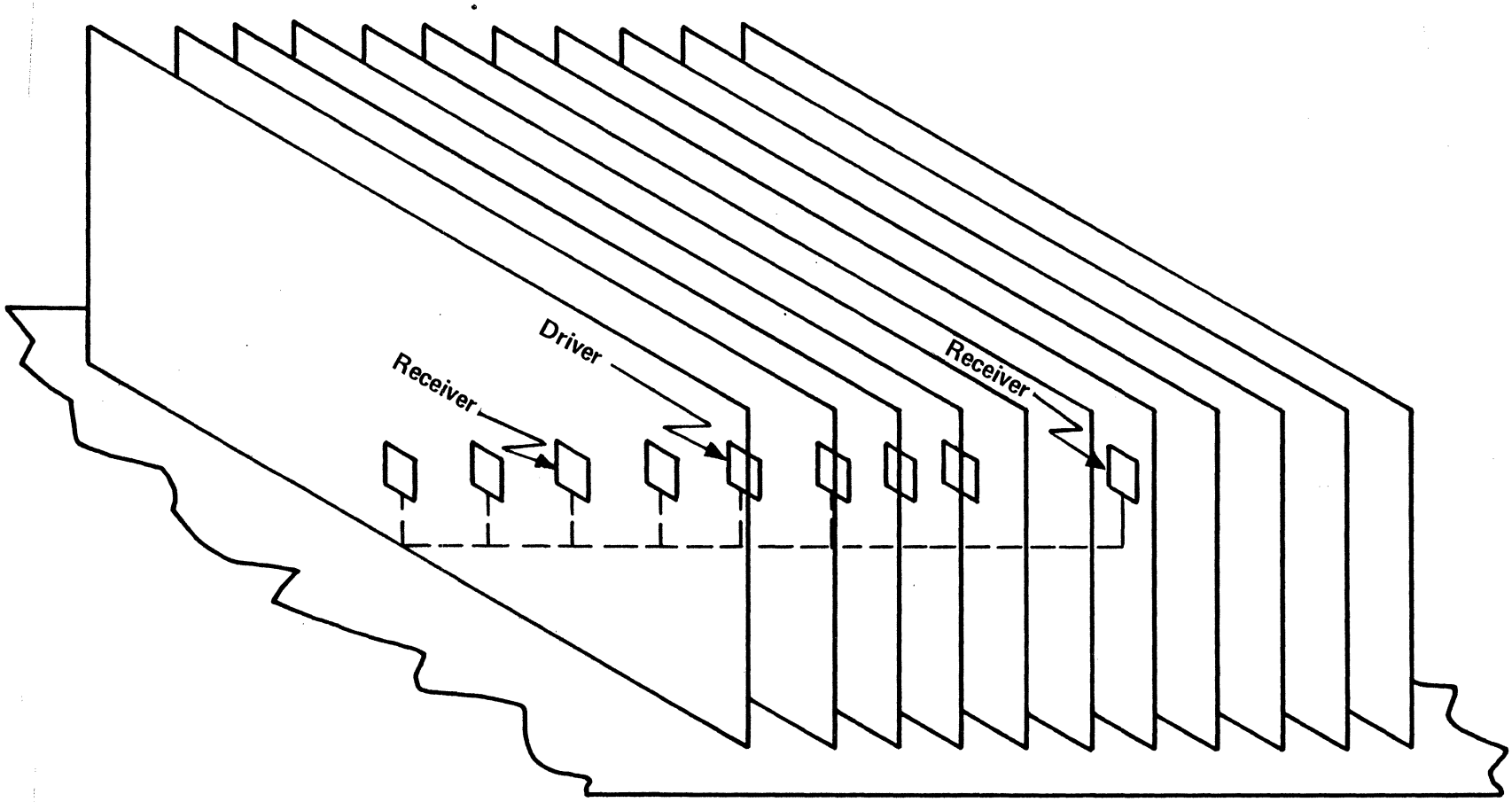




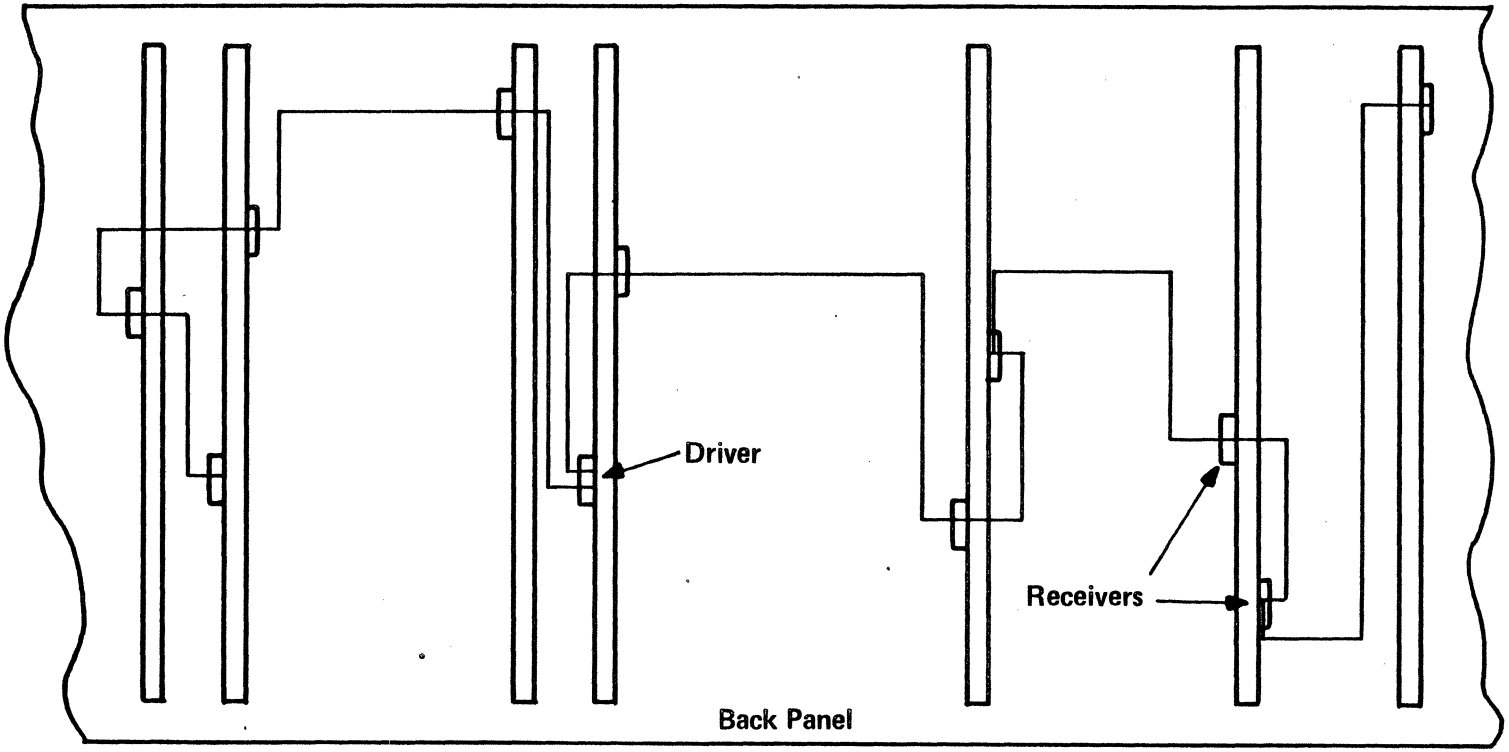
2 ns/cm
1 V/cm

This will cause the flip flop to clock

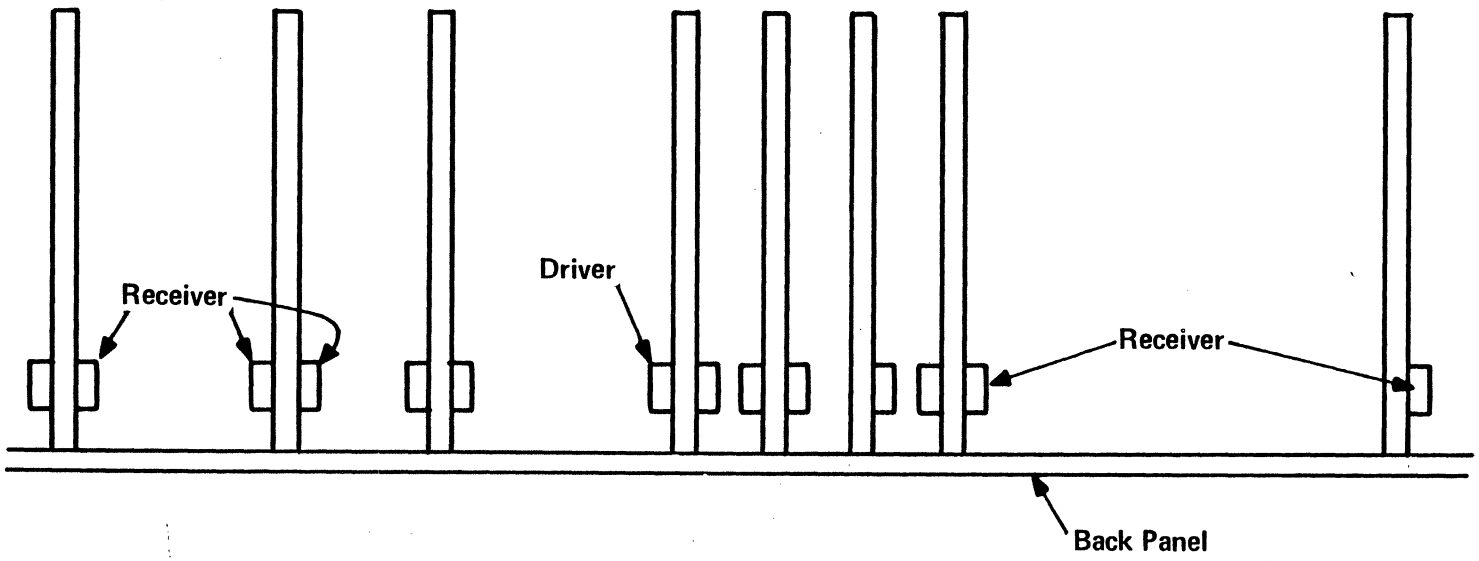
CLOCK SIGNAL DISTRIBUTION ALONG BACK PANEL



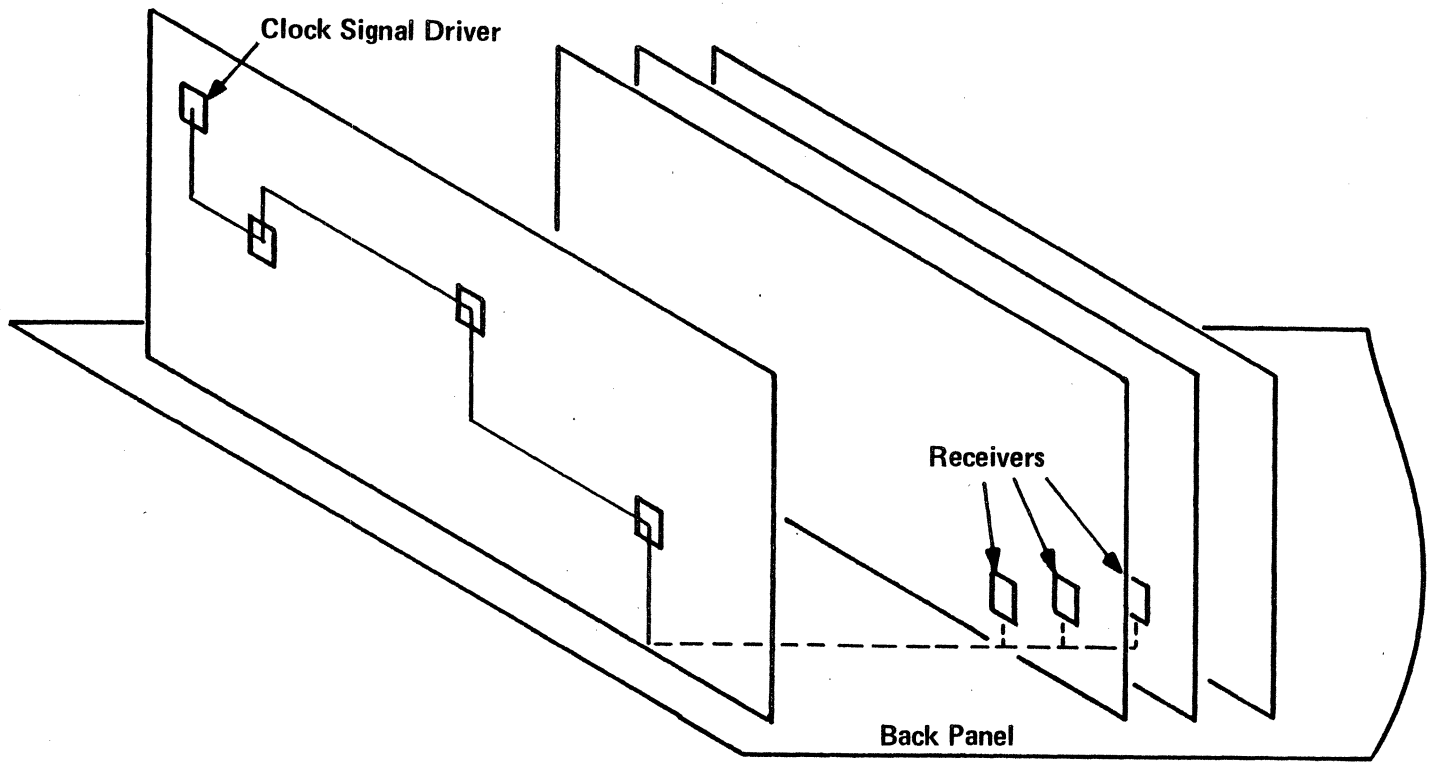
CLOCK SIGNAL DISTRIBUTION TOP VIEW



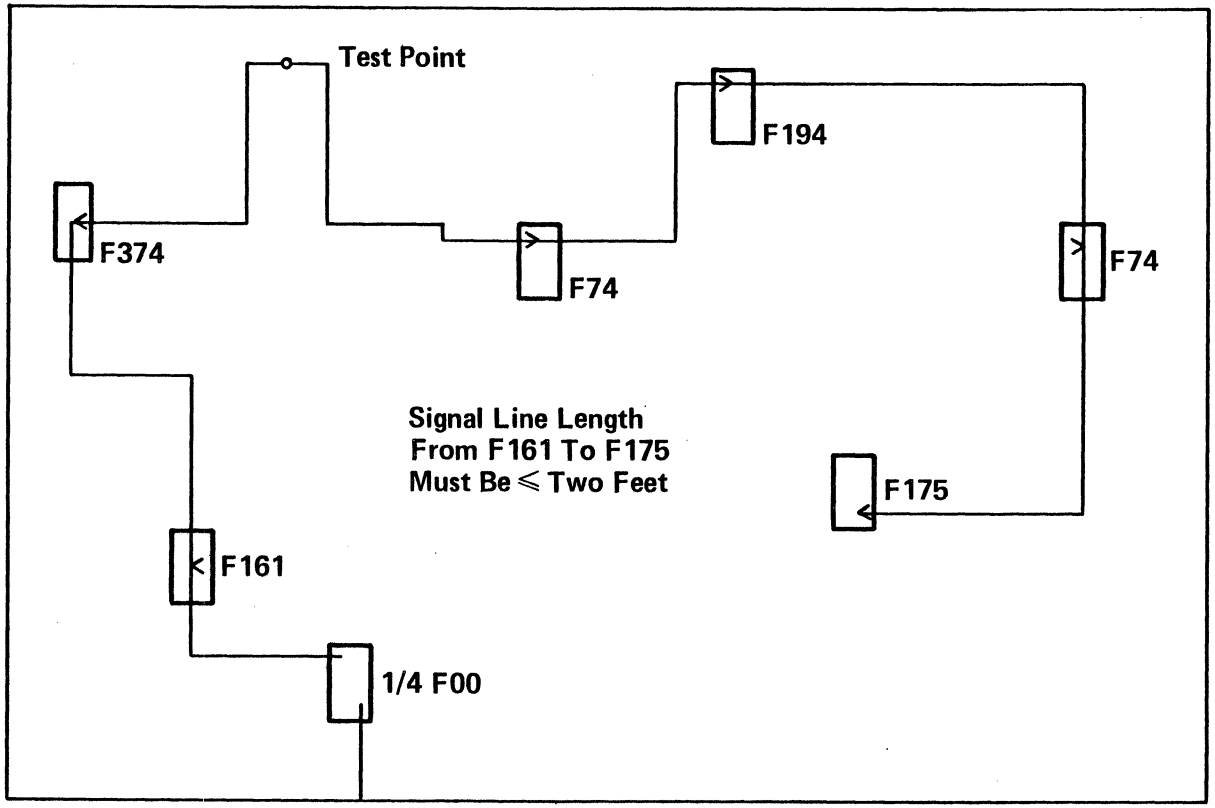
CLOCK SIGNAL DISTRIBUTION SIDE VIEW



CLOCK SIGNAL DISTRIBUTION FROM END OF BACK PANEL

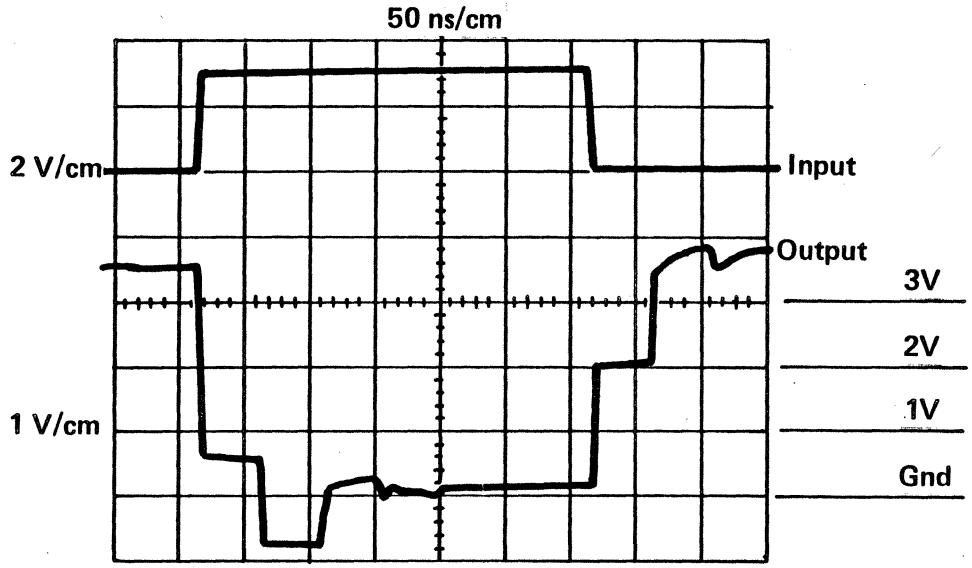


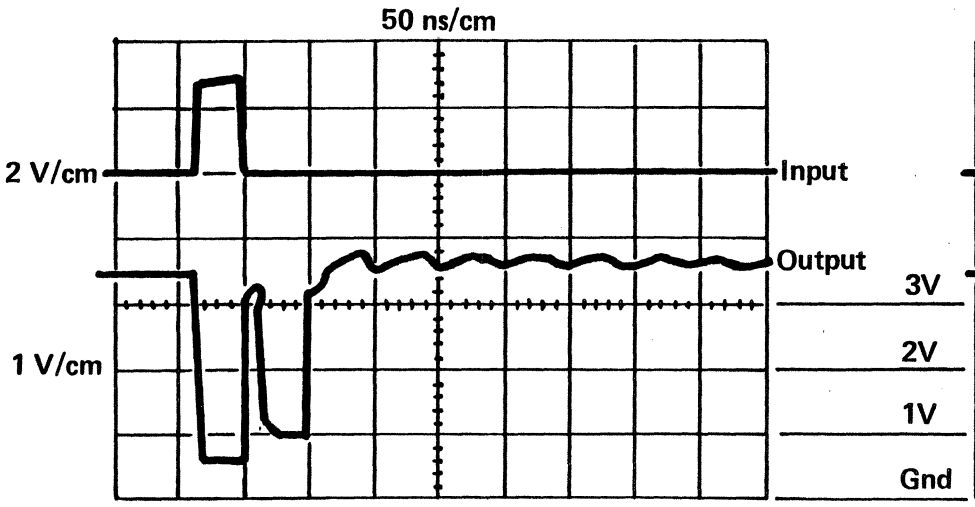
CLOCK SIGNAL DISTRIBUTION ON PAGE

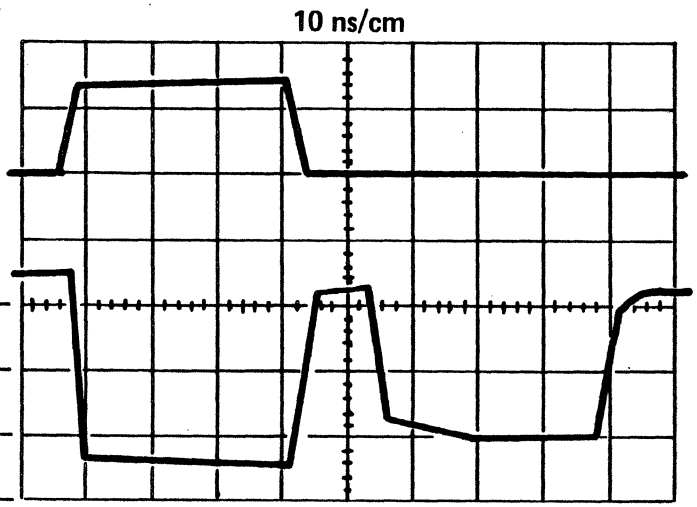


IBM

5065-60-33


50 ns/cm
2 V/cm
1 V/cm
Input
Output
3V
2V
1V
Gnd


50 ns/cm
2 V/cm
1 V/cm
Input
Output
3V
2V
1V
Gnd


10 ns/cm

ANALOG DESIGN CRITERIA ON IOA'S

- Design to Derating Guidelines for Discrete and Micro Circuits.
- 80°C Junction Temperatures.
- Design of Monolithic I.C.'s and Hybrids.
  - All circuits are analyzed and breadboarded to insure circuit performance. The breadboards, which utilize equivalent components, are temperature tested. The power supplies are varied over the limits during the temperature testing.

    The prototypes, I.C.'s are retested over power supply and temperature requirements.

NOISE

- Limit Coupling Path of Signals in Pages and Backpanels to Minimize Crosstalk.
- Voltage and Ground Distributed on Backpanel Connectors and Preassigned Signal I/O to Minimize Crosstalk.
- Tightly Coupled Ground and Voltage Planes in Backpanels to Provide High Frequency Decoupling.
- Localized Power Supply Decoupling on Pages.
- Signals on Pages and Backpanels are Shielded from Chassis.
- The Impedance on Pages, Backpanels, and Cabling are Matched, to Provide a Uniform Transmission Line Which Minimizes Ringing on Signals.
- Inter-Backpanel Transmission Lines Used to Minimize Crosstalk and Reflections.

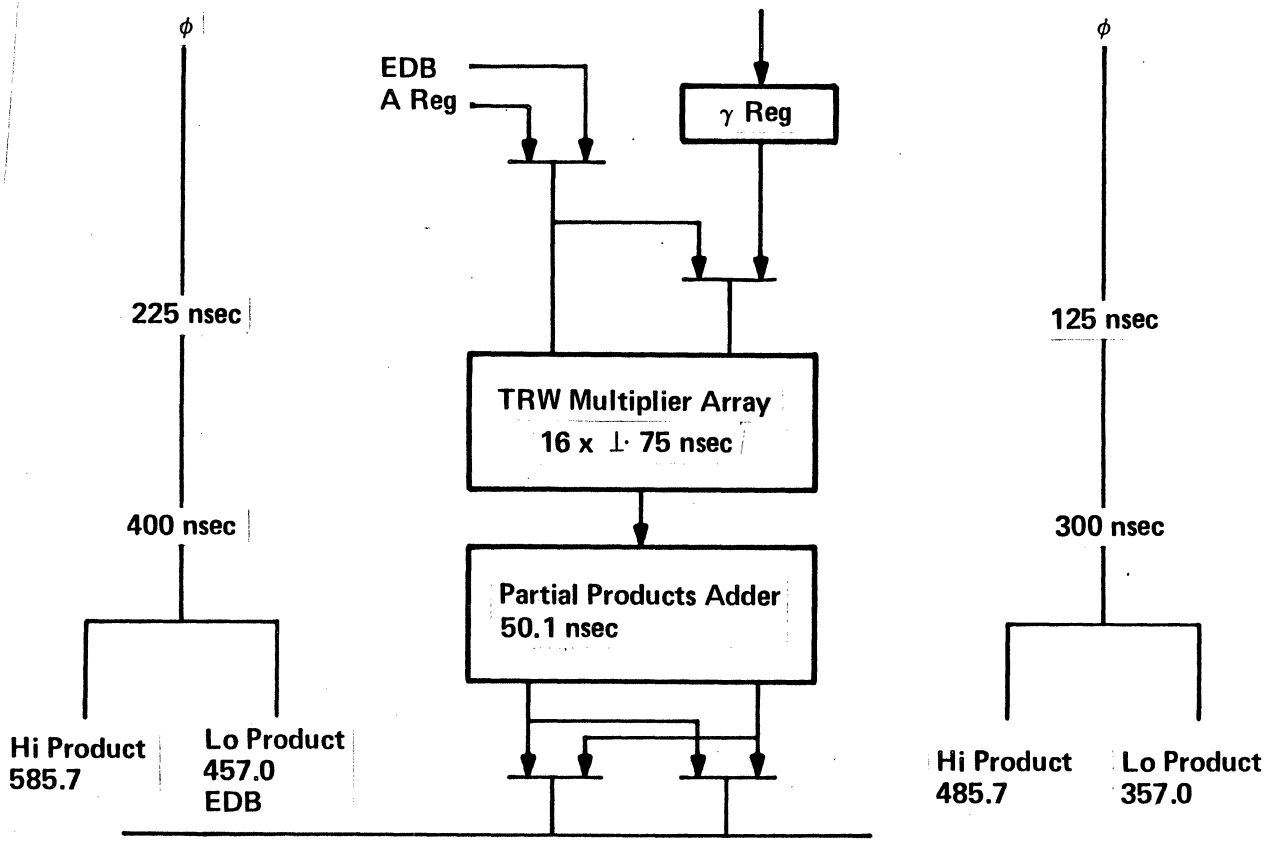
POWER SUPPLY LRU DESIGNS

- Substantial Portions of Converter, Regulator and Inverter Circuits are Identical to Hardware Presently in Production for Other Programs (eg. B52D, B52G/H, Cutty Sark, E3A/Nato).
- Over 90 Percent of Part Types Used in Power Supply LRUs are Identical to Current Production Parts.
- Modified Component Designs (eg. Converter Transformers are Verified by Testing Prototype Vendor Parts in Laboratory Breadboards).
- New Vendor-Designed Components (eg. IC Reference Circuit) are Fully Characterized for Performance to the IBM Drawing Requirements.
- All New Circuit Designs or Substantially Modified Circuit Functions have been Breadboarded and Evaluated Under Worst Case Functional Conditions.
- Circuit Analysis Results are Compared with Observed Test Results of Performance and Stress Levels.

POWER CONDITIONING/SWITCHING DESIGNS

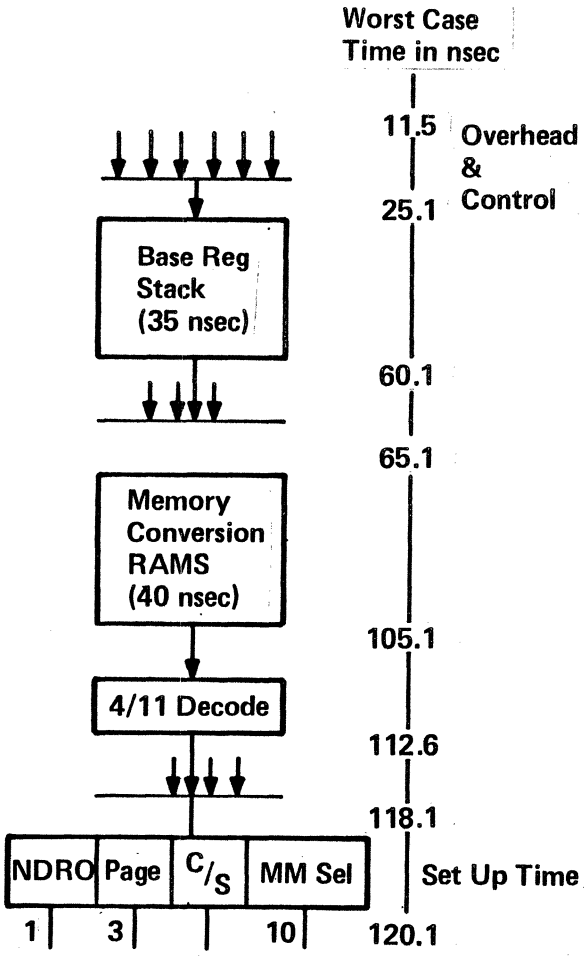
- Power Switch Gear Selected in Accordance with Part Derating Requirements.
- Prototype Power Magnetics for Conditioners Procured and Evaluated for Harmonic Distortion Performance, Efficiency and Temperature Rise.
- Breadboard EMI Filters Evaluated in Conjunction with Actual Power Conditioner Configurations and Power Converter Loads to Verify Narrow and Breadboard Performance.
- Power System Analysis and Test to Verify Compliance with EMP, Voltage Spike and Leakage Current Requirements.

MULTIPLIER TIMING ANALYSIS



Worst Case Lo Product = 4 x 125 nsec cycles = 500 Δ 43 nsec
Hi Product = ⊥ stretch cycle 162.5 Δ 76.8 nsec

I-UNIT TIMING ANALYSIS MEMORY TRANSLATION PATH

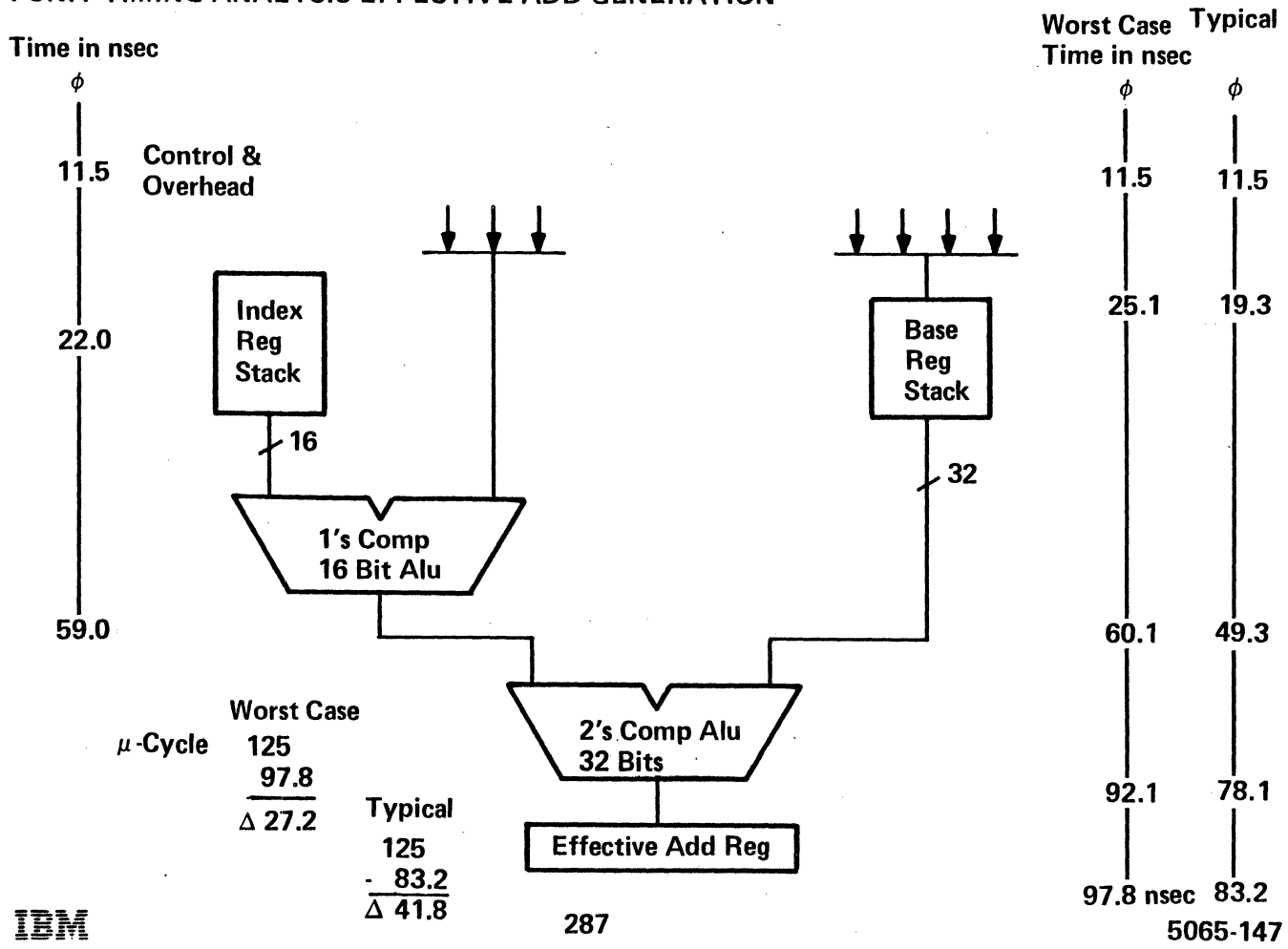


	Worst Case Time in nsec	Typical Time in nsec
	11.5	11.5
Overhead & Control	25.1	19.3
	60.1	49.3
	65.1	54.4
	105.1	89.4
	112.6	94.9
	118.1	100.2
Set Up Time	120.1	104.2

μ cycle = 125 − 120.1 = Δ 4.9

125 − 104.2 = Δ 20.8

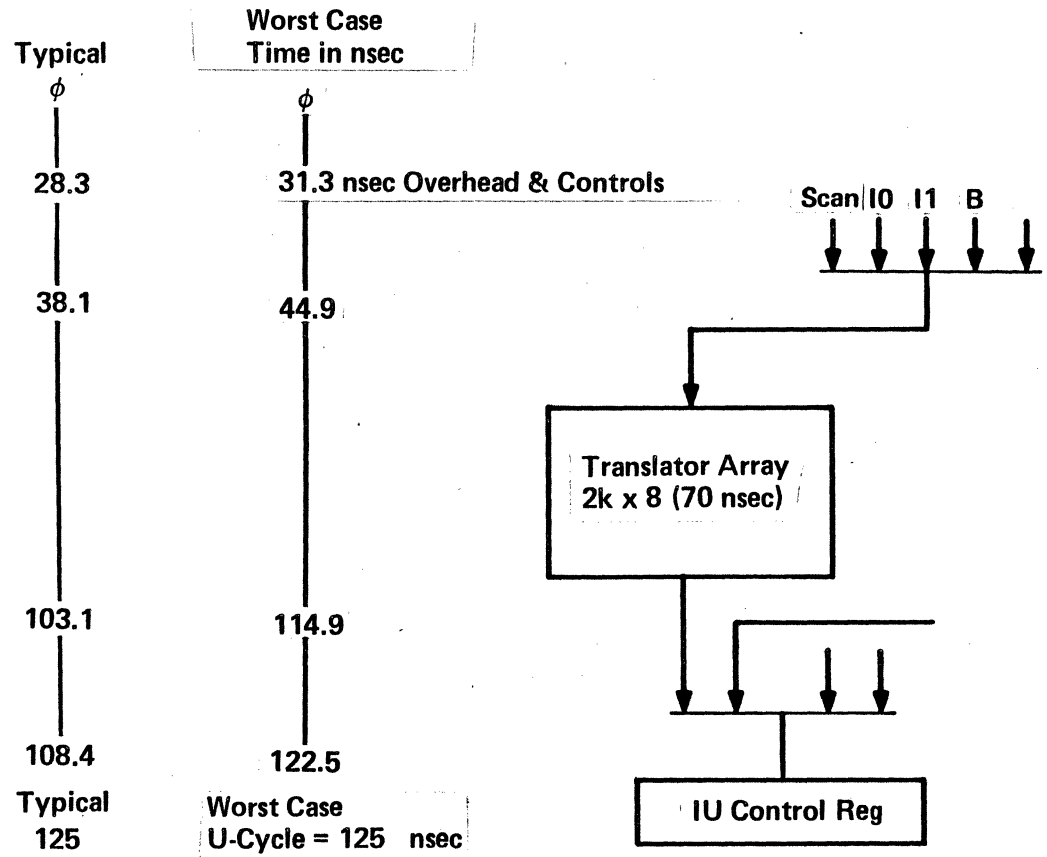
I-UNIT TIMING ANALYSIS EFFECTIVE ADD GENERATION



IBM

5065-147

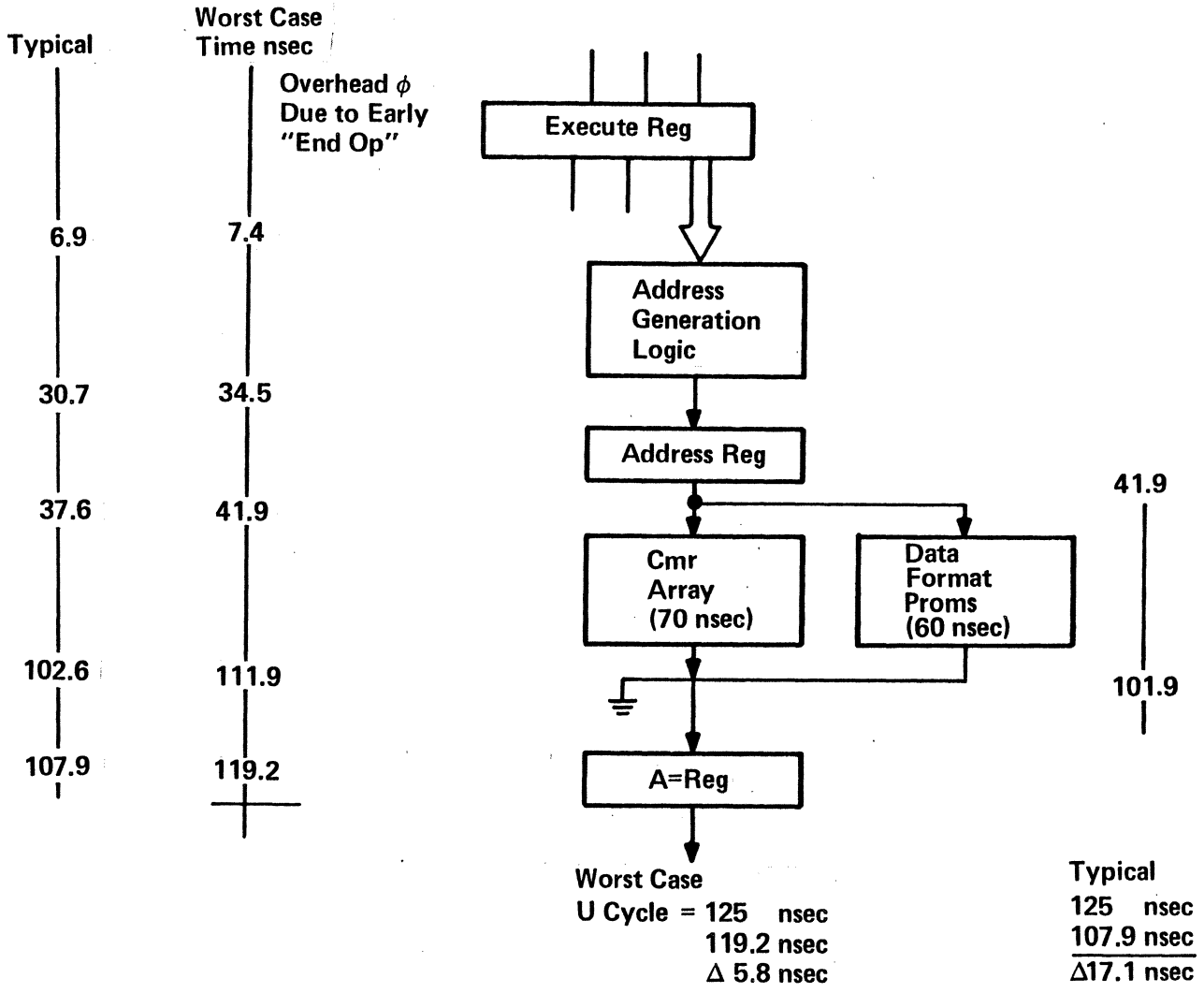
I-UNIT TIMING ANALYSIS TRANSLATOR PATH



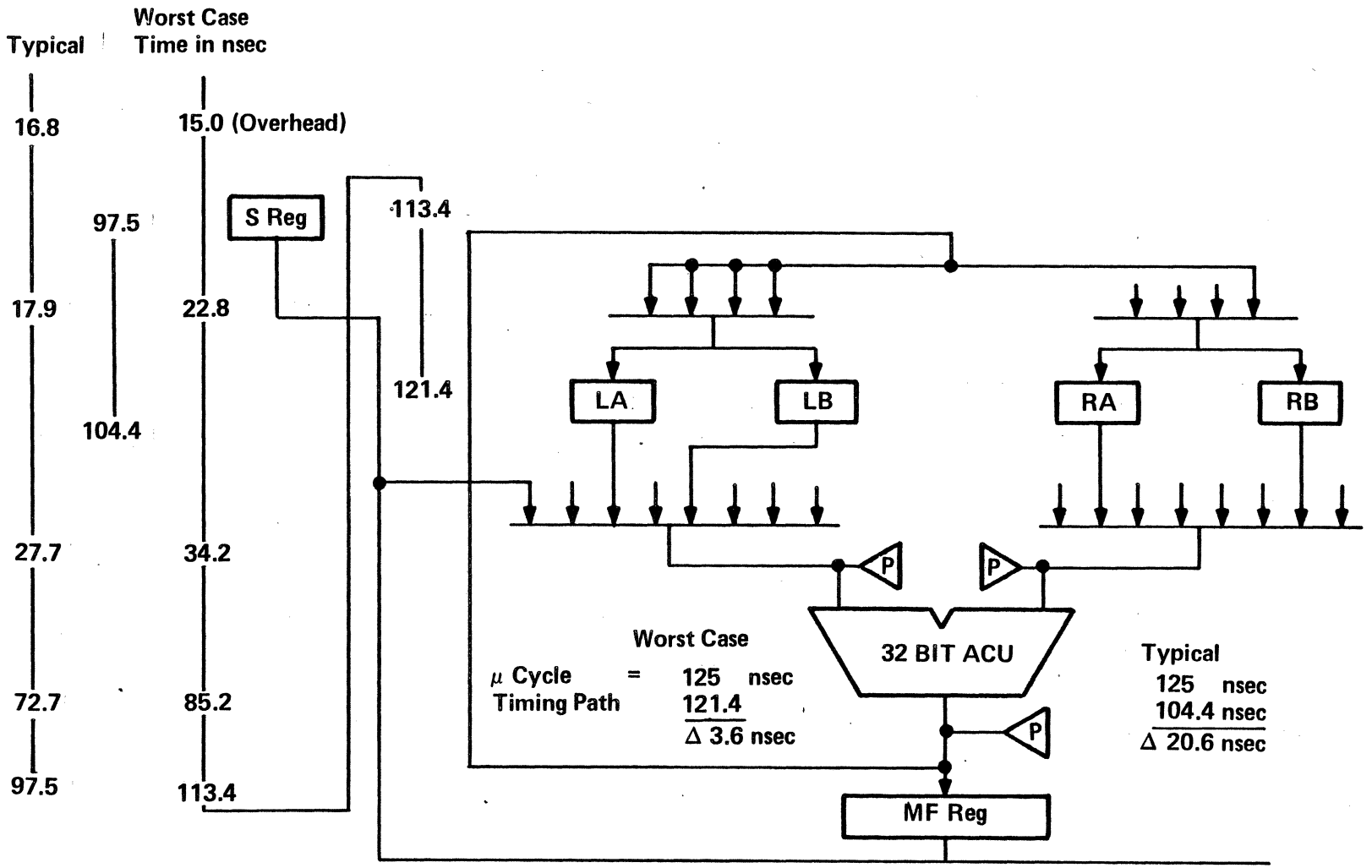
IBM

5065-148

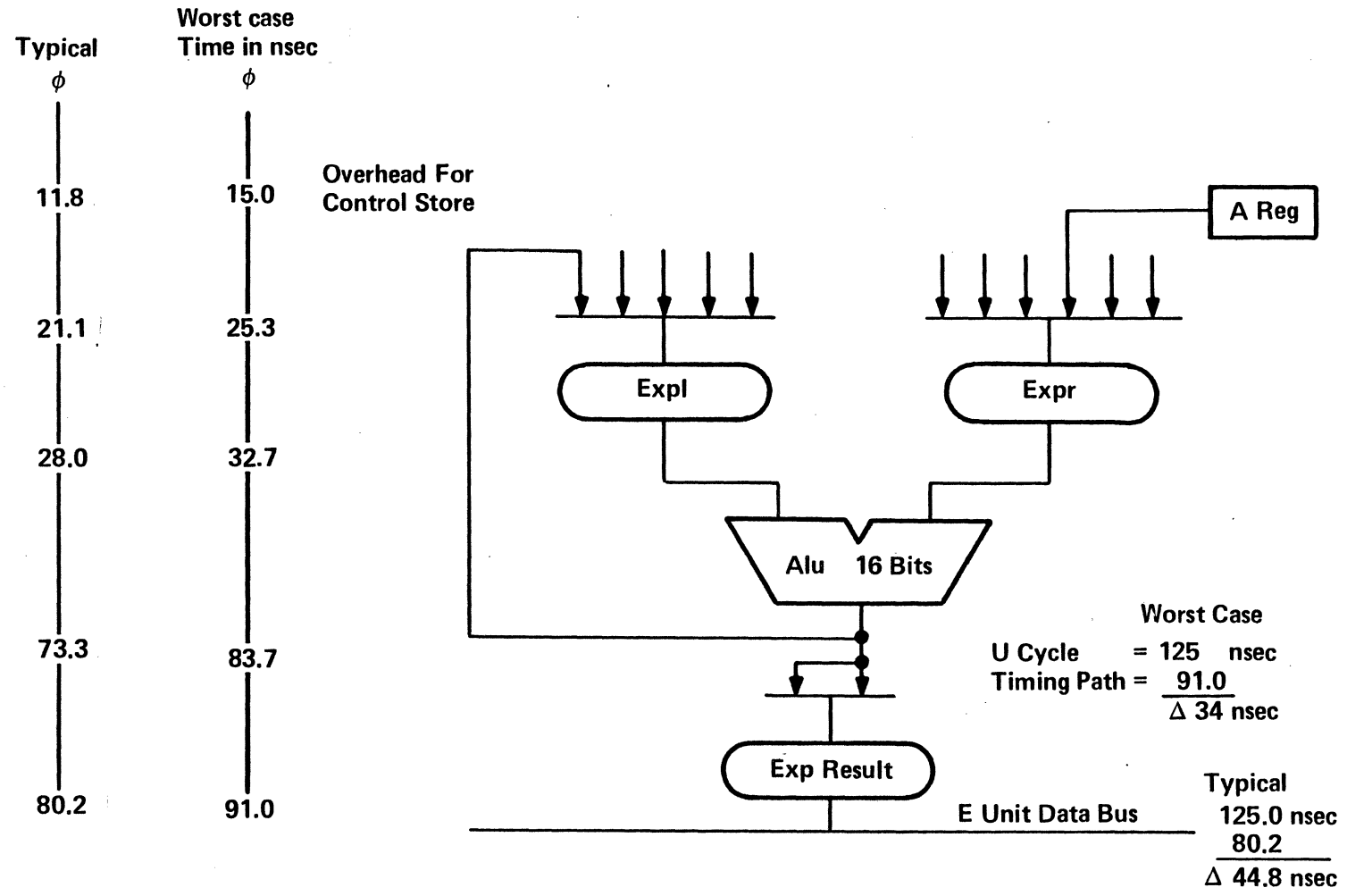
E-UNIT TIMING ANALYSIS CMR ACCESS



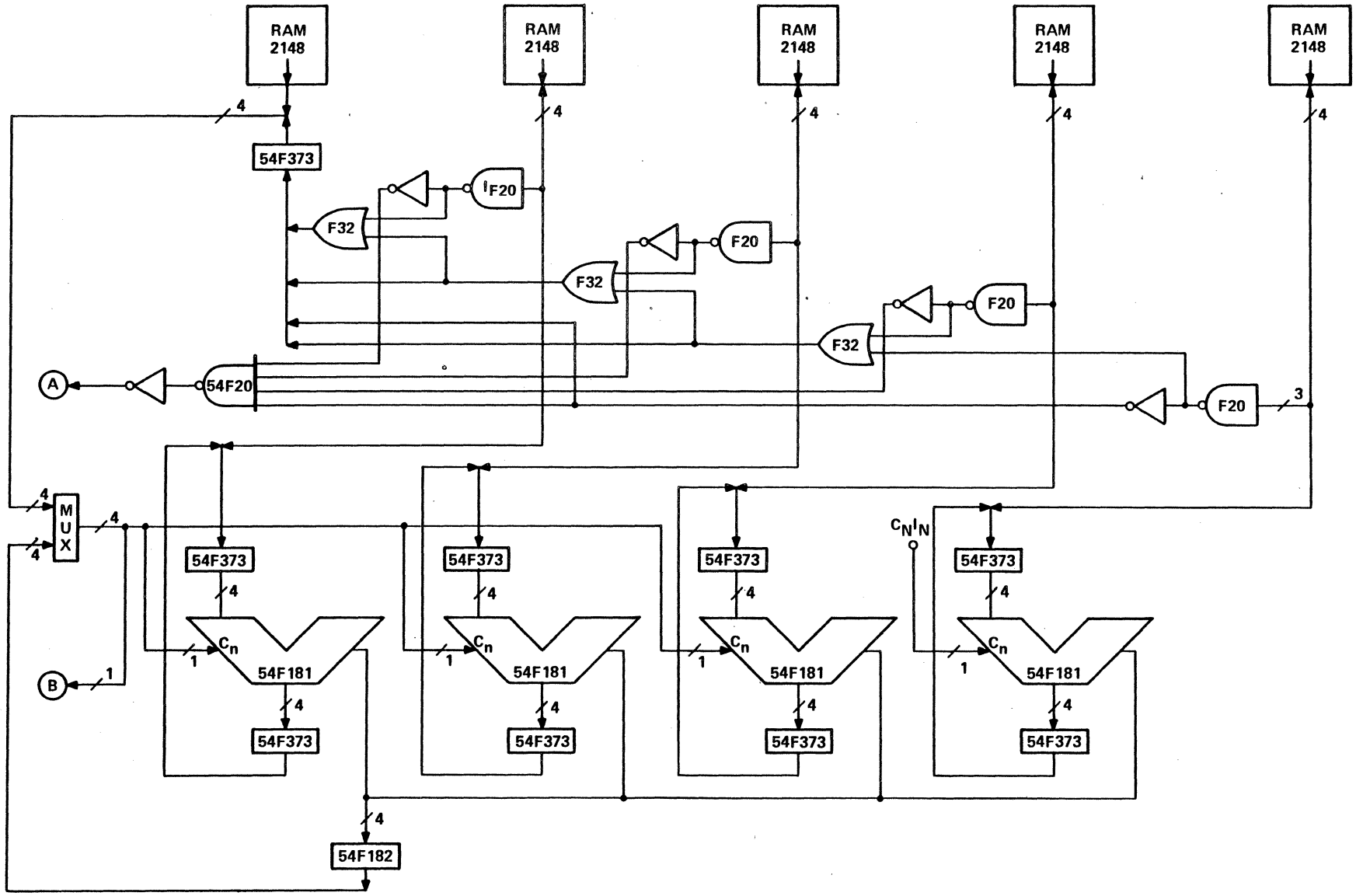
E-UNIT TIMING ANALYSIS MAIN DATA FLOW (S REG TO RANK REG)



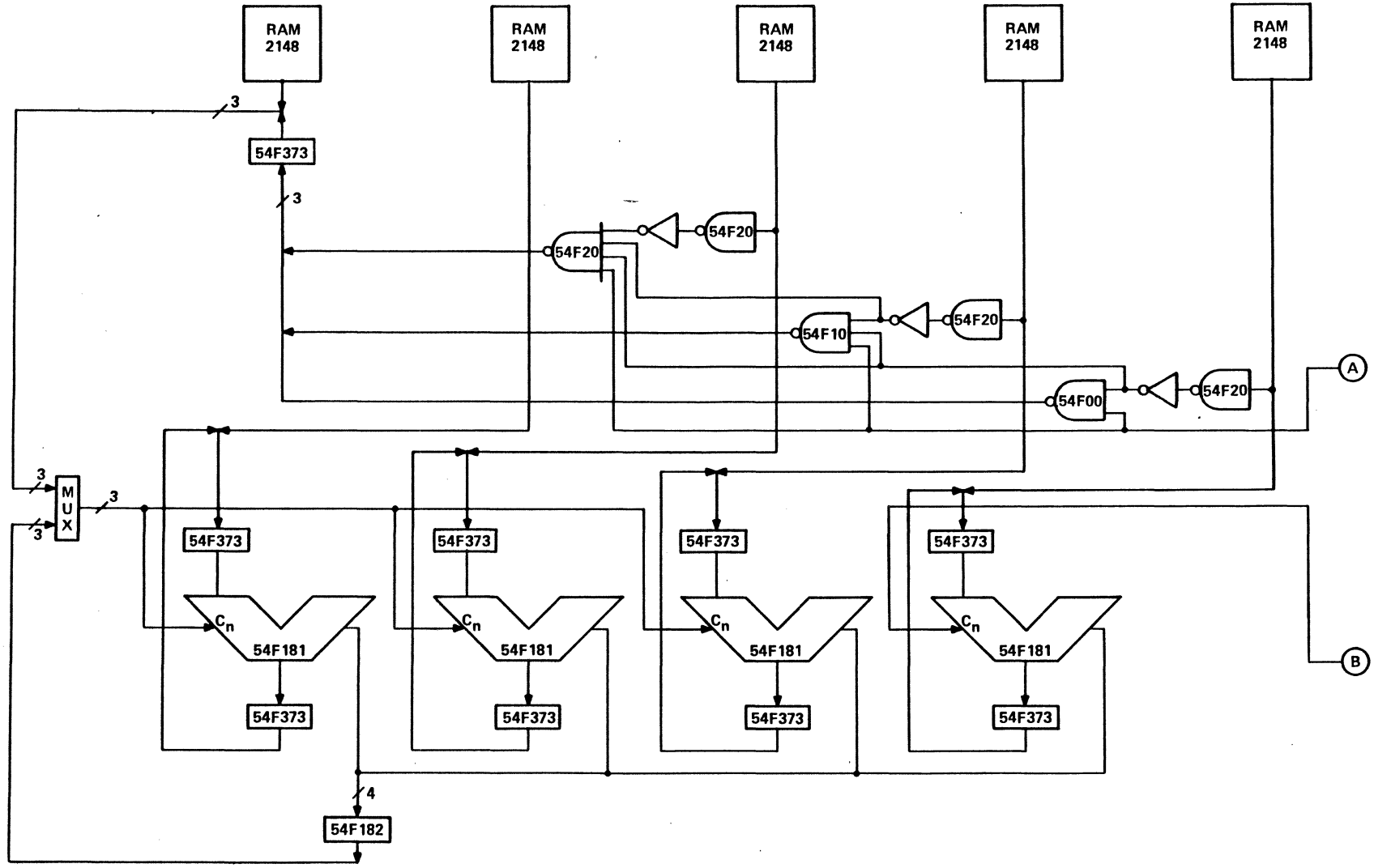
E-UNIT TIMING ANALYSIS EXPONENT DATA FLOW



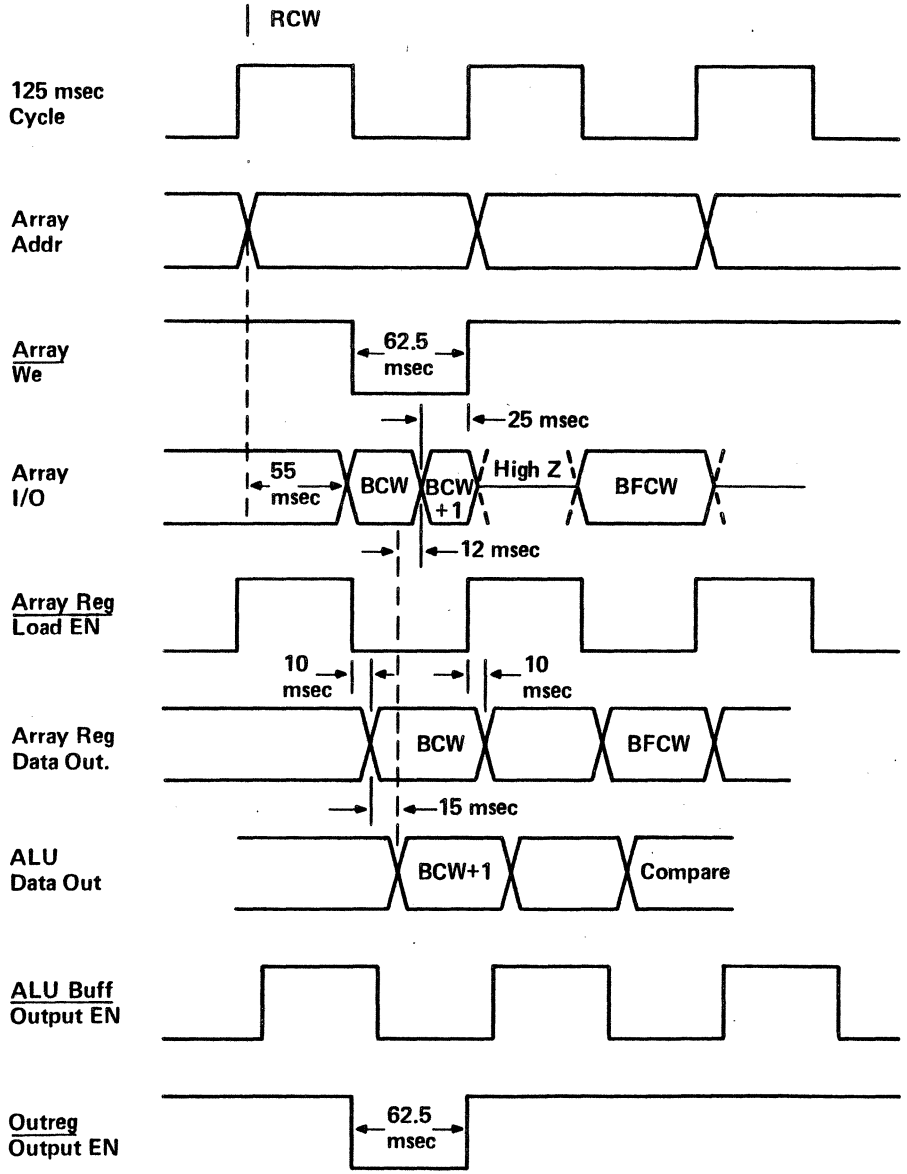
PROCESSOR DETAIL ($\phi\phi$ - 15)



PROCESSOR DETAIL (16-31)

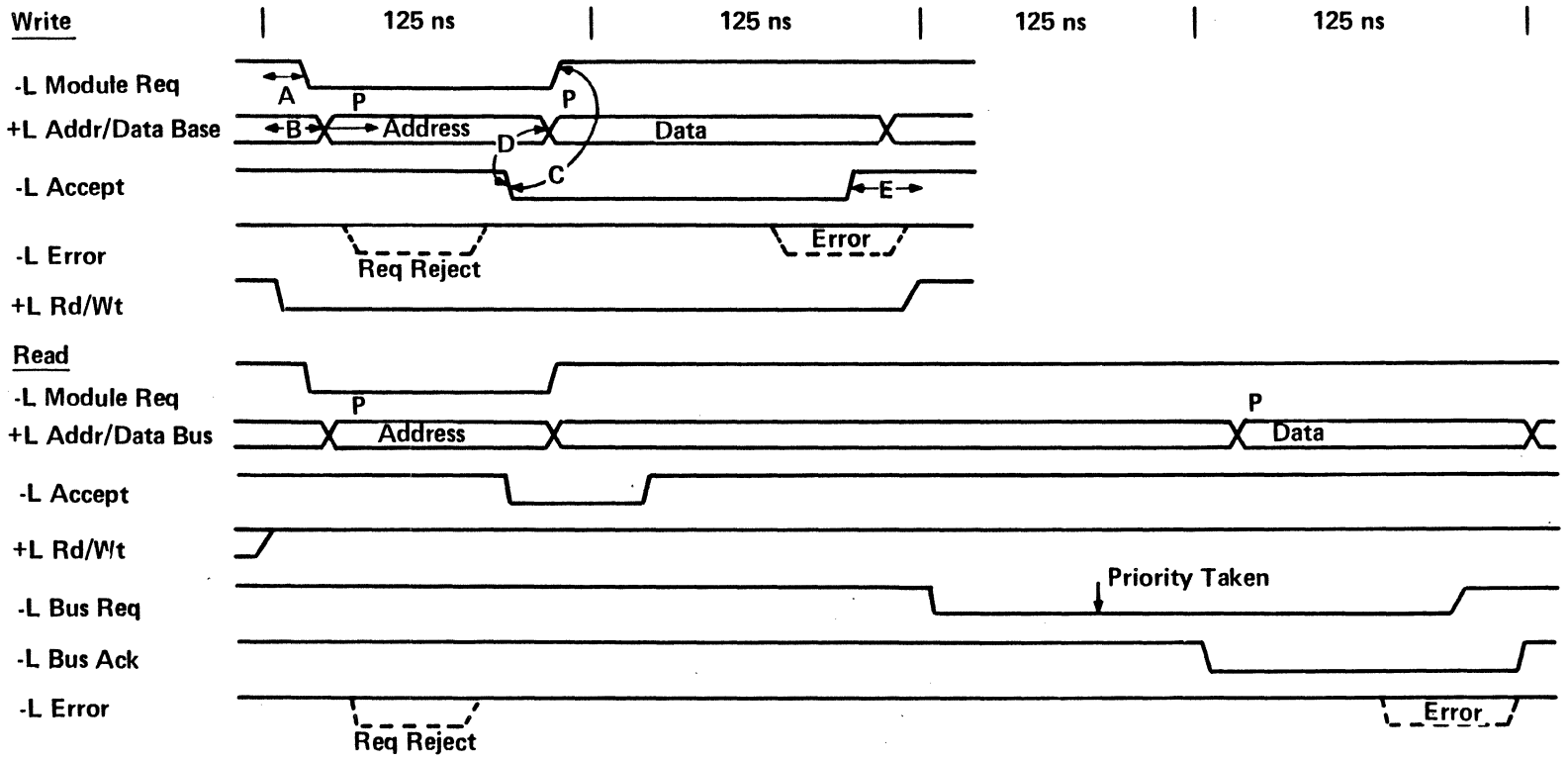


IOC PROCESSOR TIMING

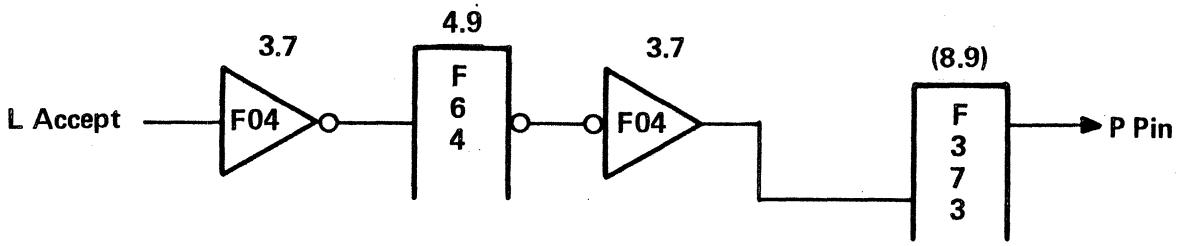


5065-151-3

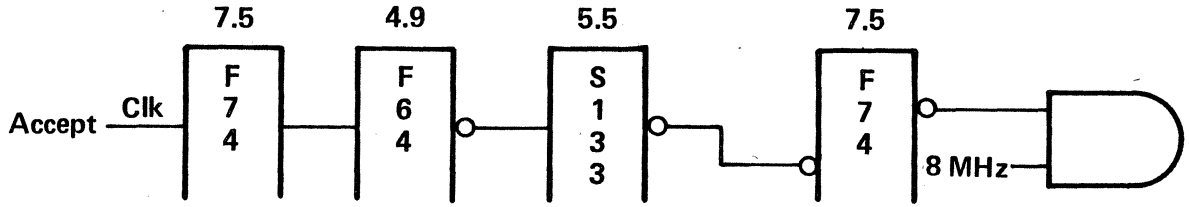
IOC MEMORY TIMING



D Accept ↓ To Data + Parity Good = 21.2 ns

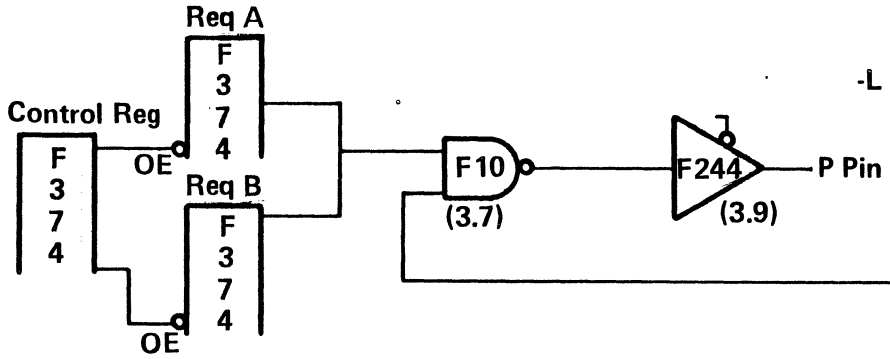


E Accept ↑ To End of Cycle = 25.4 ns

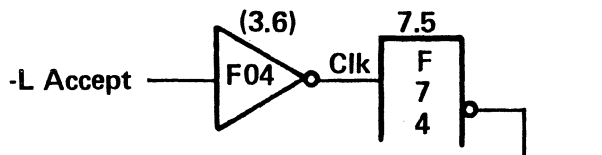


CRITICAL DATA PATHS

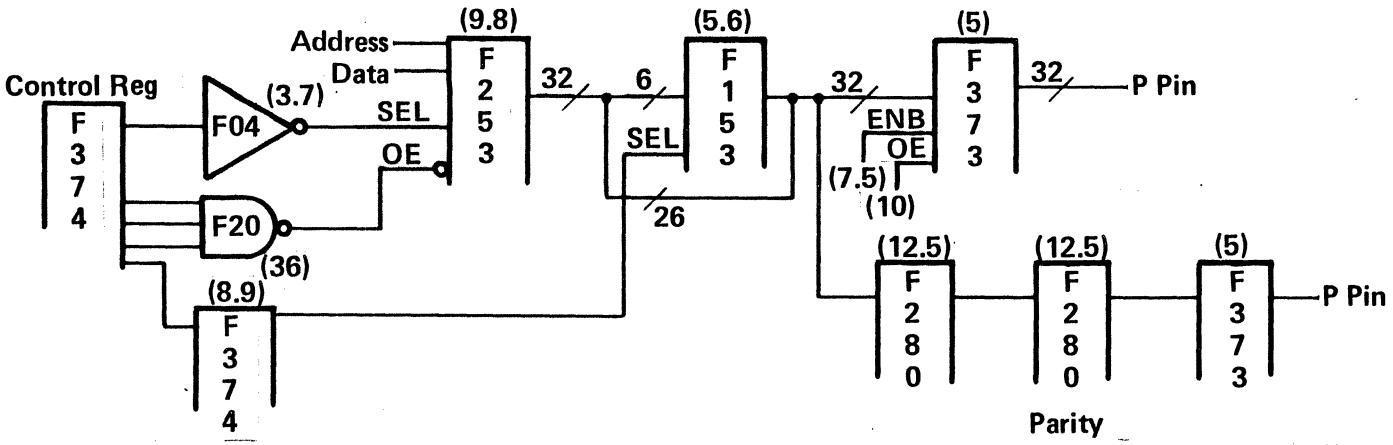
A Cycle Start To Request Down = 15.6 ns



C Accept ↓ To Req ↑ = 18.7 ns



B Cycle Start To Address Good = 24.2 ns



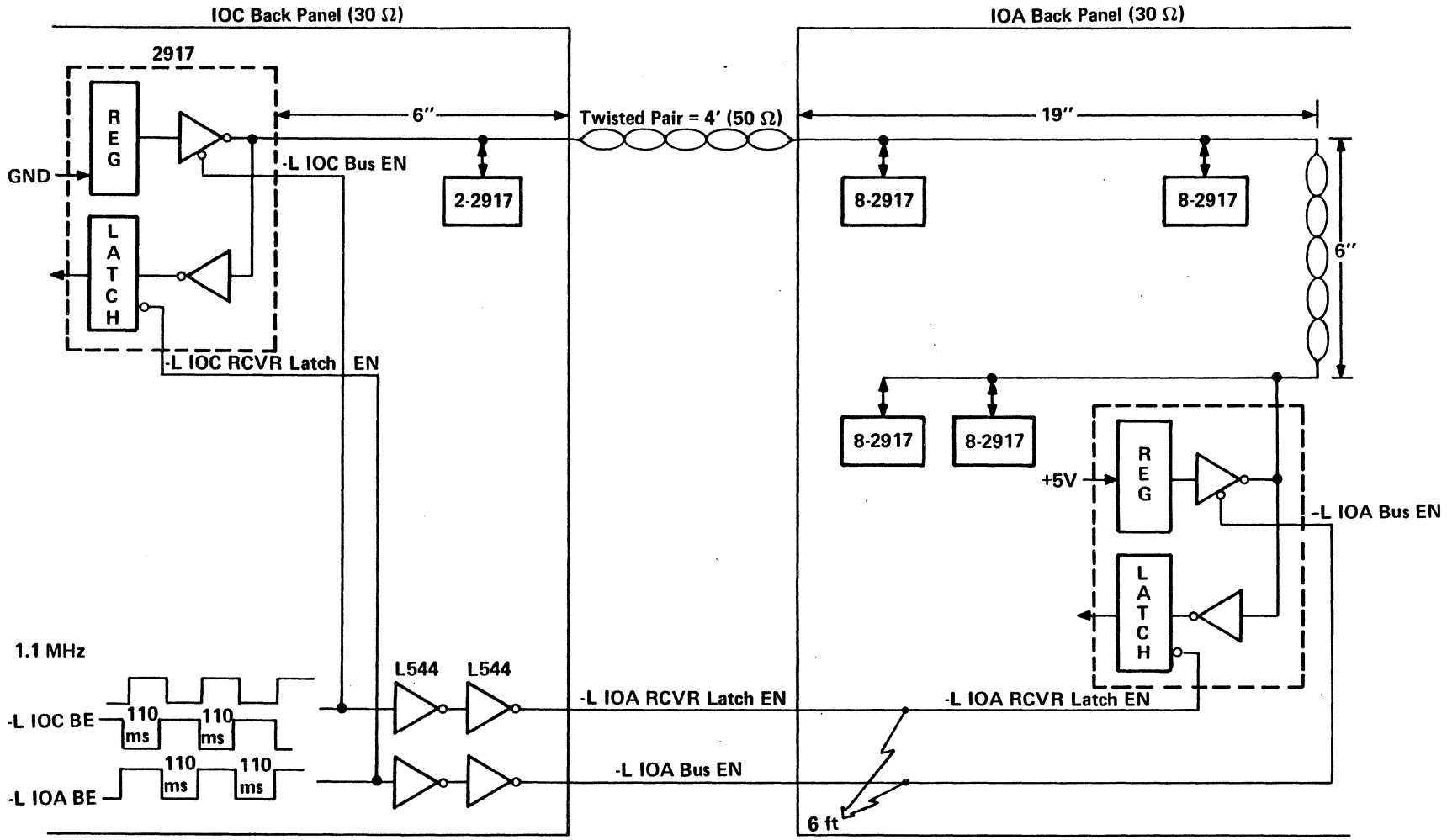
Cycle Start To Parity Good = 49.1 ns

IOC/IOA BUS LOADING

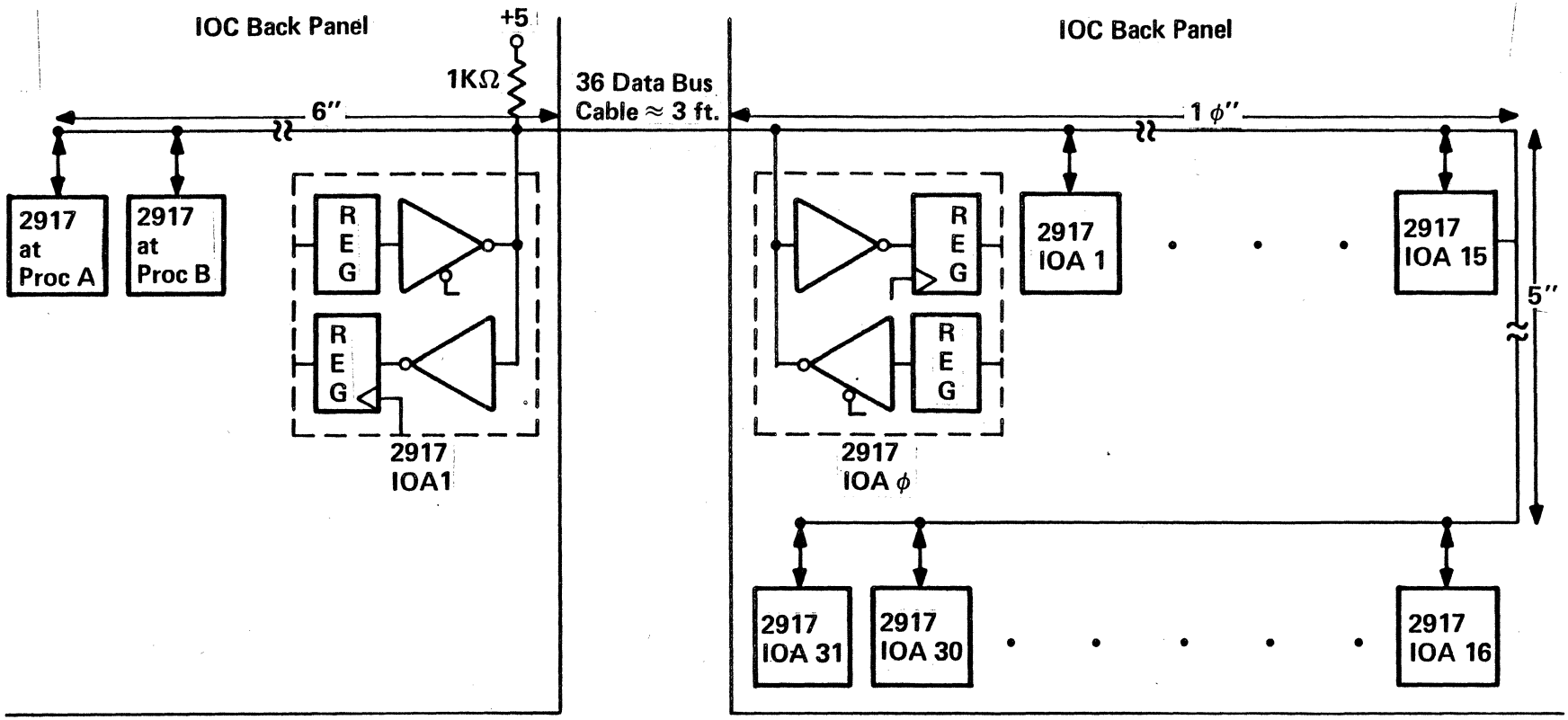
	Logic 0 (≤0.5V)	Logic 1 (≥2.4V)
Load Per Sink	200 μA	50 μA
Total Load (34 sinks)	11.8 mA*	1.7 mA
Source Drive	48 mA	15 mA
% Load	~25%	~12%

*Includes 5 mA in pullup resistor

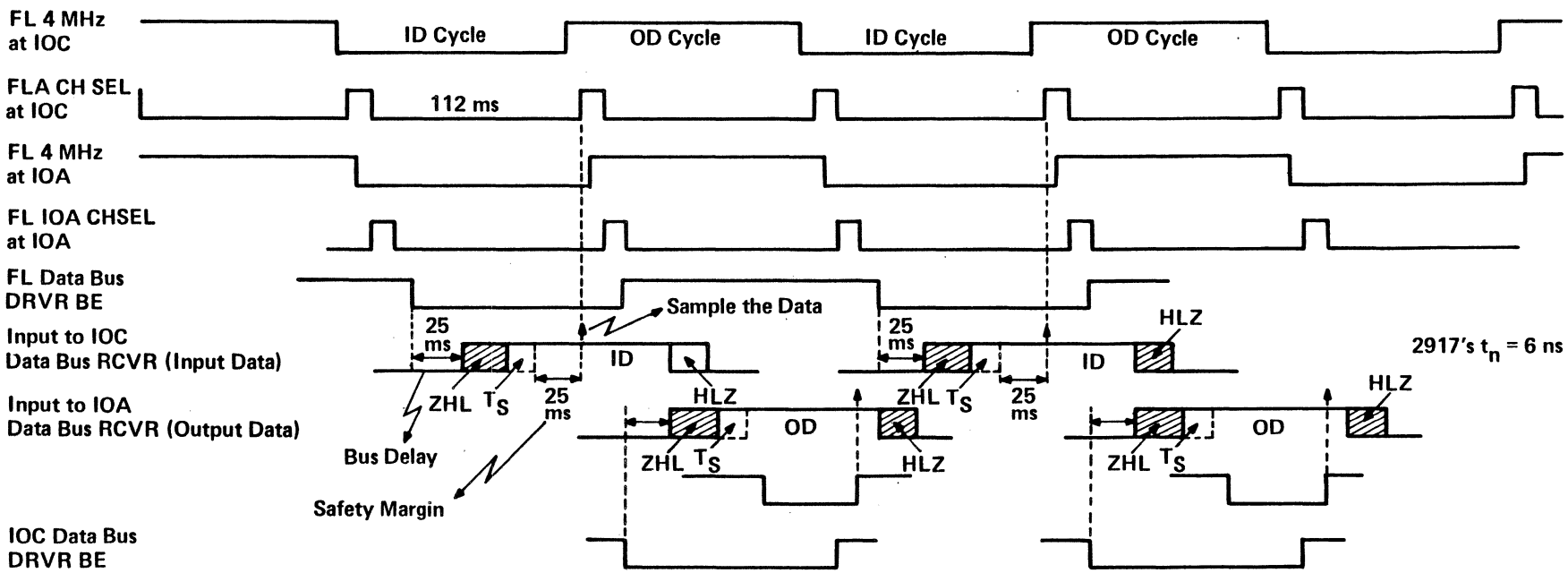
IOC/IOA INTERF LAB SIMULATION



IOC/IOA INTERF DATA BUS

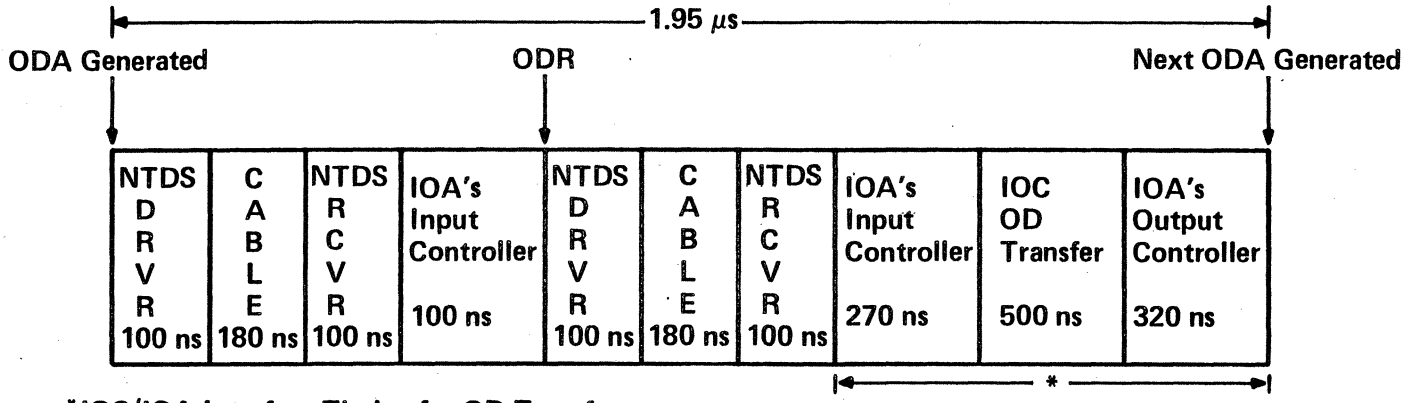


IOC/IOA INTERF TIMING

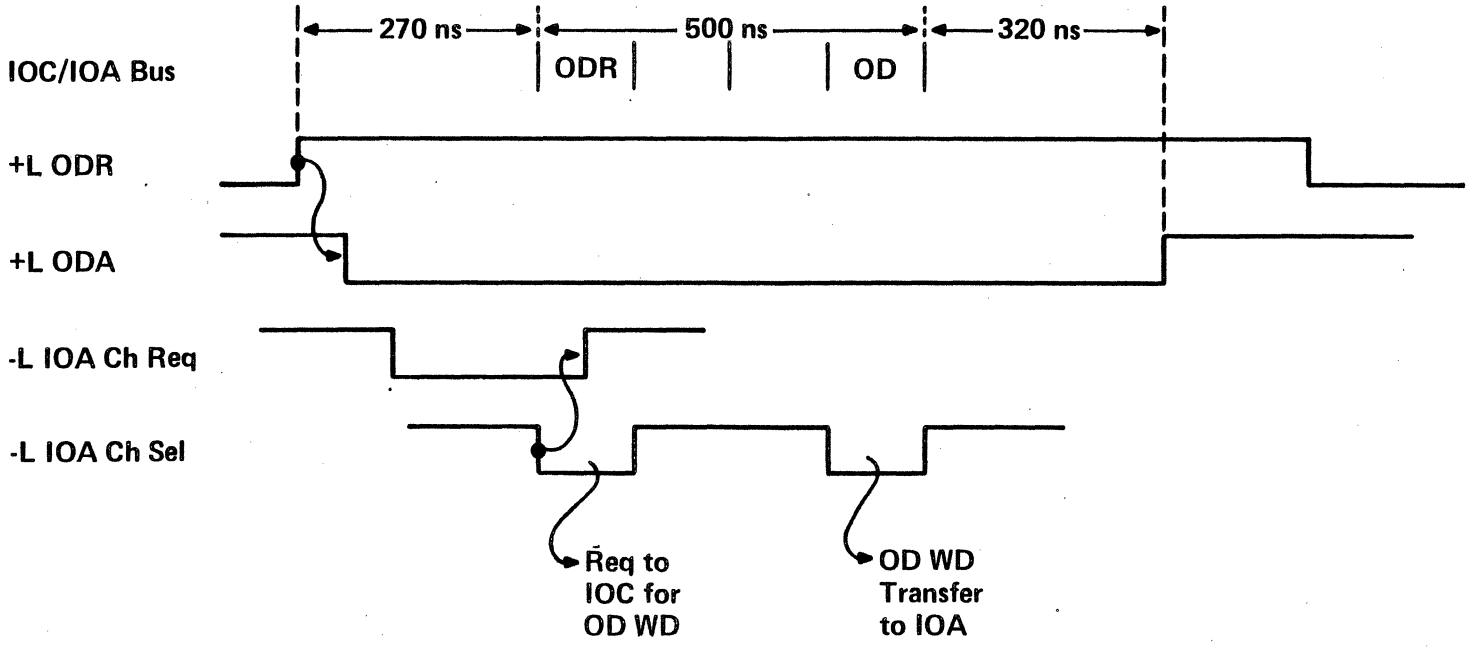


Max Theoretical Bus Delay = 18 ns

NTDS TYPE H PARALLEL CHANNEL THROUGHPUT RATE ANALYSIS



*IOC/IOA Interface Timing for OD Transfer:



5065-151-11

FTRM

FTRM

- Introduction
  - Mission
  - List of functions
- Definition
  - Operating system assumptions
  - Data base requirements
- Interfaces
  - Illustration
  - FTRM to operating system
  - FTRM to application
  - FTRM to OLSD
  - FTRM to SASD
  - FTRM to BCU software
- Function Flow
  - Overall
  - Initialization
  - Class I & II interrupt handler
  - FHM isolation
  - Configuration and resource management
  - Diagnostic interface
  - Application interface
  - Operator interface
- Storage Estimate
- Schedule

INTRODUCTION

Mission

- Implement all fault tolerant computer design features for the AN/UYK-43 Computer System
- Perform System Resource Monitoring Functions
- Maintain a Continuous Account of all Available Computer Resources
- Support Application Controlled Reconfiguration and Reload
- Provide Online Access to all System Diagnostic Capabilities and Recovery Services

Functions

- Initialization
- Class I & II Interrupt Handler
- FHM Isolation
- Configuration and Resource Management
- Diagnostic Interface
- Application Interface
- Operator Interface

DEFINITION

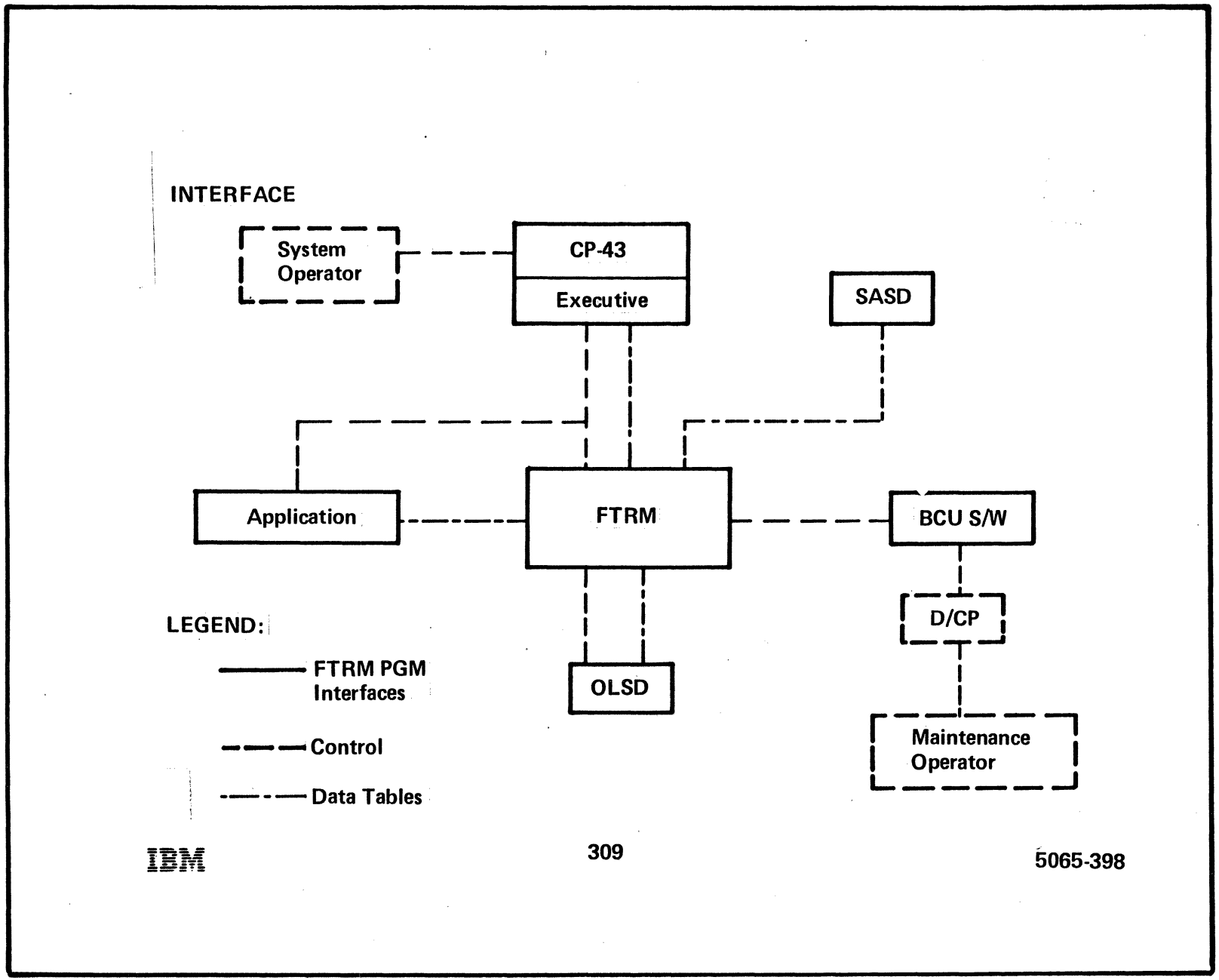
Operating System Assumptions

- Demonstrated Using AN/UYK-7 Common Program and SDEX/7.
- Can be Modified to use any Operating System with Equivalent or Greater Services.
- FTRM Requires From Operating System:
  - Executive services
  - I/O services
  - Access facility
- FTRM adds:
  - Automatic casualty reaction.
  - Software fault detection
  - Support of online maintenance.

Data Base Requirements

Main Storage Tables Shall be Used by FTRM to:

- Store System Status Information.
- Module Interface
- Application Control of Recovery Actions and Execution Modes.
- FTRM Tables:
  - System resource table
  - Casualty error data table
- Application Tables:
  - Software state mapping table
  - Application option table
- Operating System Tables:
  - Memory mapping table
  - I/O mapping table


INTERFACE
System Operator
CP-43
Executive
SASD
Application
FTRM
BCU S/W
D/CP
OLSD
Maintenance Operator
LEGEND:
FTRM PGM Interfaces
Control
Data Tables

FTRM To Operating System

- Control
  - Task scheduling
  - Interrupt handling
  - Program segment load
  - Message processing
  - Common data updata and fetch
  - Interface to system peripheral devices
- Data
  - Memory mappling table
  - I/O mapping table

FTRM To Application

- Control
  - Request messages from application
  - Response messages to application
- Data
  - System resource table
  - Software state mapping table
  - Application option table

FTRM To OLSD

- Control
  - Initiated as subroutine to FTRM
  - FTRM assures required H/W is available
- Data
  - Casualty error data table
  - System resource table
  - Application option table

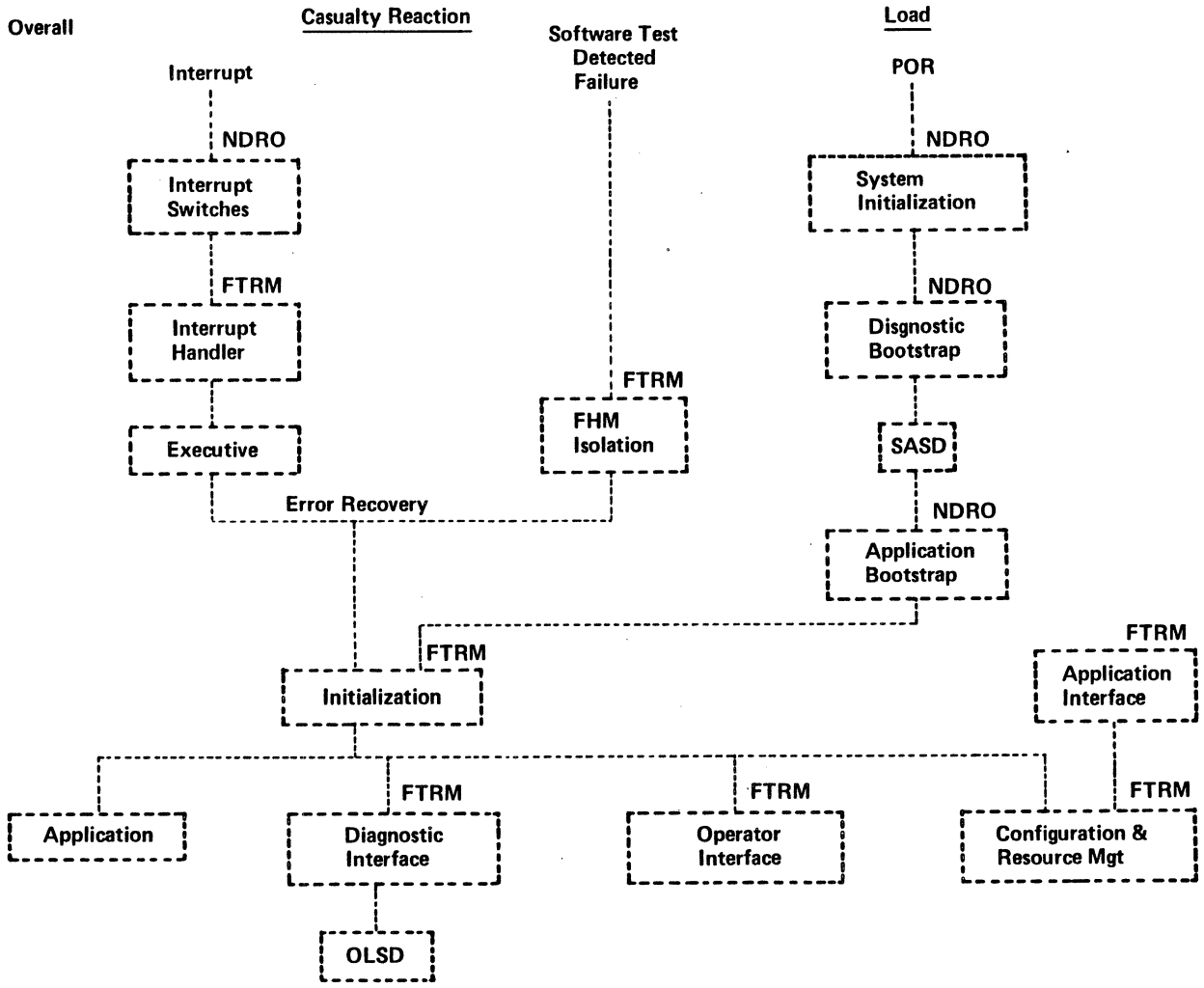
FTRM To SASD

- Data
  - System resource table

FTRM To BCU Software

- Control
  - — Privileged bus command to read BCU storage word for data from D/CP.
    - -- Execute test
    - -- Bypass test
    - -- Mode 600
  - — Privileged bus command to send data to D/CP via BCU.
    - -- Resource status data
    - -- Test menus & results

FUNCTION FLOW



NOTE: For simplicity paths required for some functions (e.g. AN/UYK-7 IPL, Warm Start) are omitted.

IBM

5065-404

Initialization

```
proc Initialization
   [ start/restart the Application ]

   use  Casualty_Error_Data_Table
   use  System_Resource_Table
   use  Software_State_Mapping_Table

   Poll BCU Store to determine cold start/warm start
   if
      proceeding from IPL (cold start)
   then
      [ load the Application based on current resources ]
      run  Configuration_and_Resource_Management
   else
      if
         reload required
      then
         [ reload appropriate RCM's ]
         run  Configuration_and_Resource_Management
      fi
   fi

   for
      all active Application Modules
   do[Indicated in the Mapping Table ]
      cause Application Module to go through initialization
   od

   perform FTRM Task initialization
   request Operator Interface output the status and error log

corp
```

Class I & II Interrupt Handler

```
proc Interrupt_Handler(in Class I & II Interrupts out CEDT)

   if
      FHM can not be determined from ISC data
   then
      run additional tests to isolate FHM
   else
      isolate FHM from ISC data
   fi

   Build Casualty Error Data Table (CDET) entry
   Reconfigure H/W to remove faulty FHM from system
   Invoke the Executive to initiate normal Interrupt processing
   [  control will pass from Executive to FTRM Initialization  ]

corp
```

FHM Isolation

```
proc FHM_Isolation (in Error_Data out CEDT)

   if
      Error data not sufficient to isolate FHM
   then
      run additional tests to isolate faulty FHM
   else
      Isolate FHM from error data
   fi

   Build Casualty Error Data Table (CEDT) entry
   Initiate FTRM Initialization function

corp
```

Configuration And Resource Management

```
proc Configuration_and_Resource_Management (in Request out Response)
    use  System_Resource_Table
    use  Software_State_Mapping_Table
    use  Application_Option_Table
    if
       Request is valid
    then
       case
          Request_Type
       part (Reload_Request)
          determine active resources from System Resource Table
          load/reload as specified in Mapping Table
       part (Table_update_request)
          perform requested update
       part (status_request)
          Response := Requested status
       else continue
       esac
    else
       Response := Request_Denied
    fi
corp
```

Diagnostic Interface

```
proc Diagnostic_Interface (in Request out Response)

   use  Casualty_Error_Data_Table
   use  System_Resource_Table
   use  Application_Option_Table

   if
      Request is valid
   then

      case
         request
      part  (LRU_Isolation)
         run OLSD (in FHM_ID out Result)
         Response  := Result
      part  (fault_detection_test)
         add/delete requested test to list of periodic tests
      else continue
      esac

   else
      Response  :=  Request_Denied
   fi

   pass Response to requestor

corp
```

Application Interface

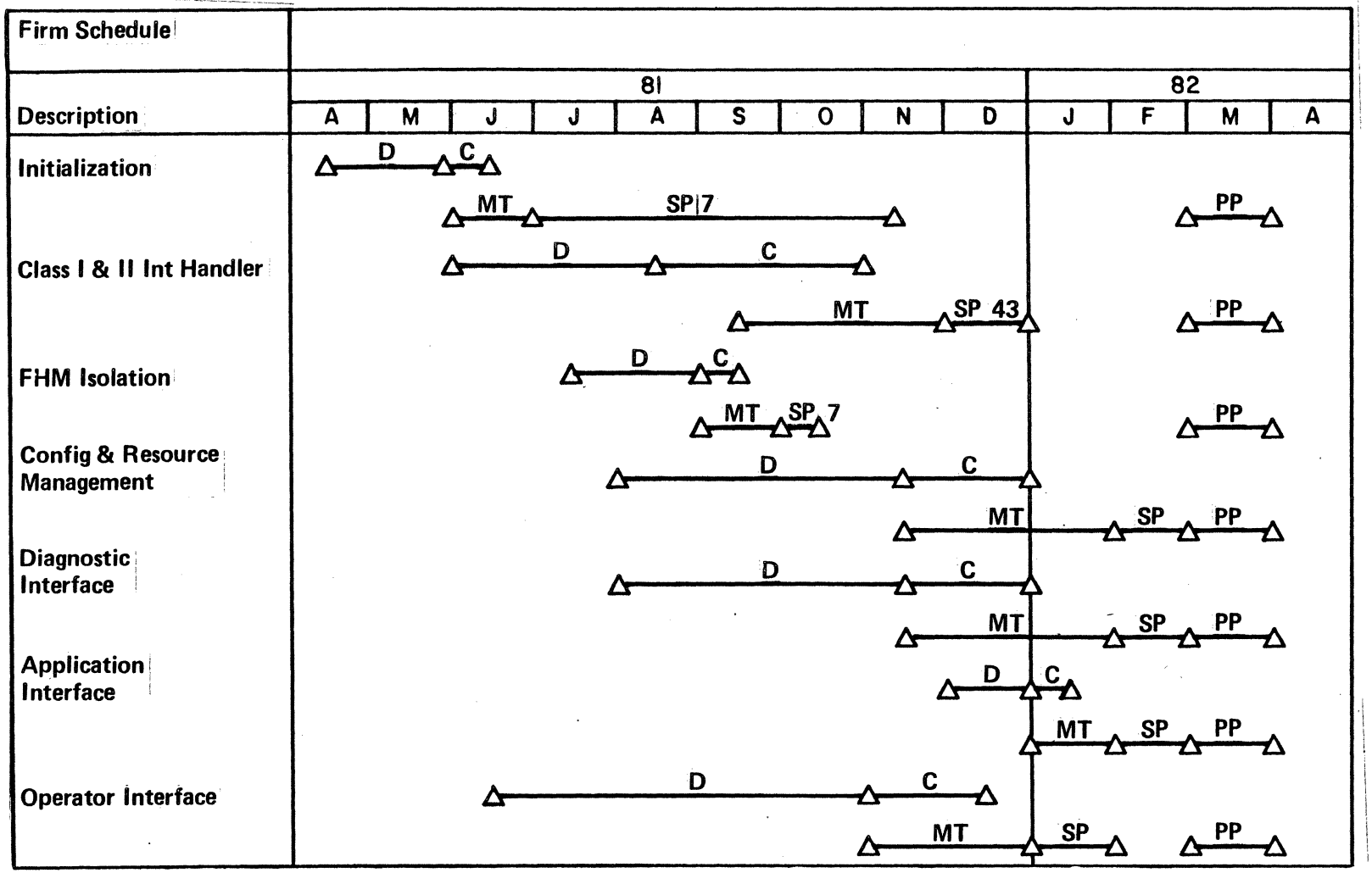
```
proc Application_Interface (in Request out Response)
  use Application_Option_Table
  if
    Request is valid
  then
    if
      request for Diagnostic service
    then
      run  Diagnostic_Interface (in request out Response)
      pass result back to Application
    else
      if
       request for reconfiguration
      then
       run Configuration_and_Resource_Management (in request out Response)
       pass result back to Application
      fi
    fi
  else
    Response := Request_Denied
  fi
```

Operator Interface

```
proc Operator_Interface (in message out message, BCU_cmd)

  var message : message
  type message = rec
                   destination : ID of destination function
                   source : ID of sender
                   content : data
                 cer

  Validity check the message
  if
    source = FTRM
  then
    send message to op sys module for transfer
      to System Operator
    format and send BCU cmd to pass data to D/CP
  else
    send message to appropriate FTRM function
  fi

  Poll BCU store for D/CP input
  Process any D/CP data

corp
```

STORAGE ESTIMATES

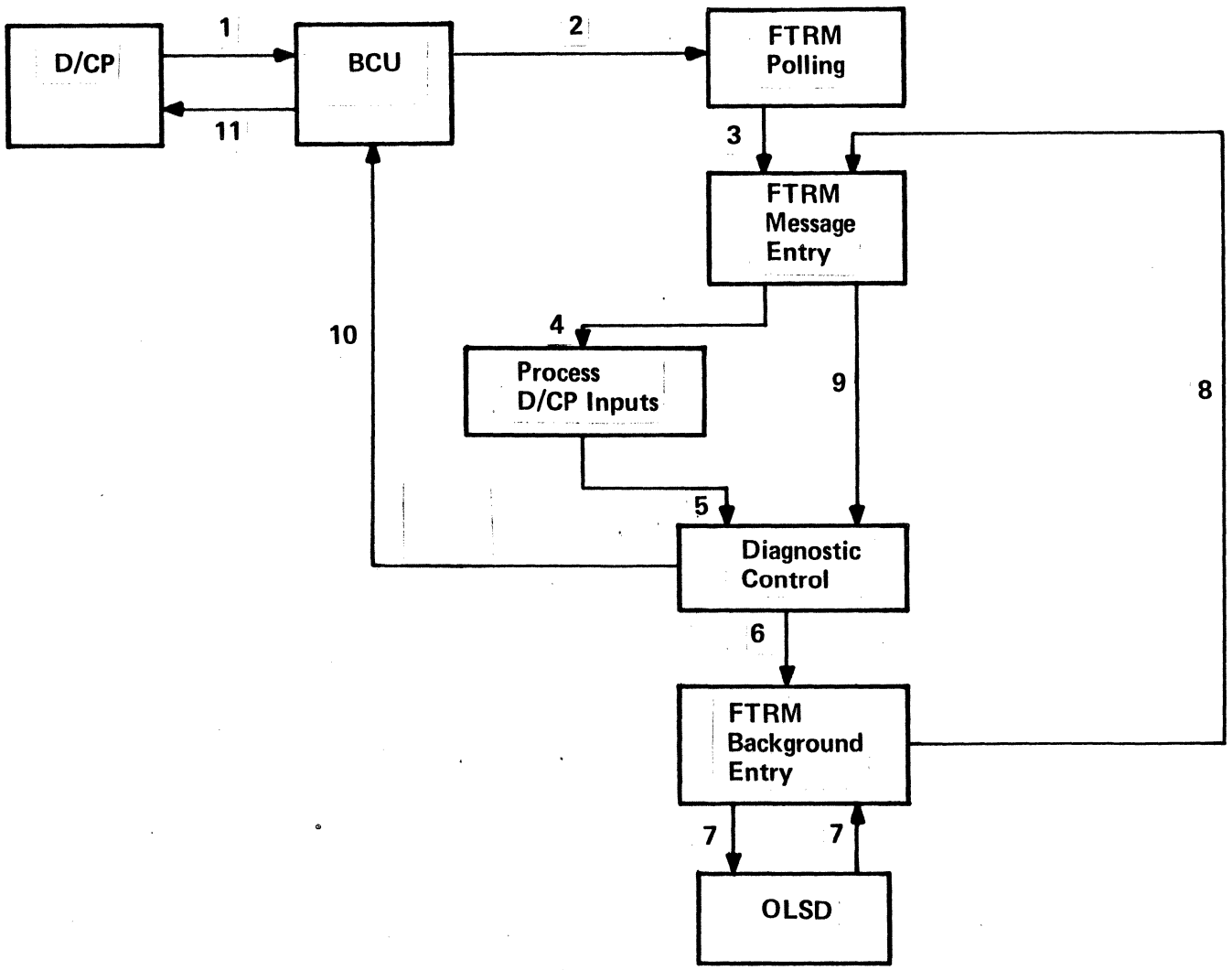
FUNCTION	SLOCS
Initialization	1000
Class I & II interrupt handler	2500
FHM isolation	1000
Configuration and resource management	2500
Diagnostic interface	2500
Application interface	500
Operator interface	3000
Total	13000


Firm Schedule
81
82
Description
A
M
J
J
A
S
O
N
D
J
F
M
A
Initialization
D
C
MT
SP 7
PP
Class I & II Int Handler
D
C
MT
SP 43
PP
FHM Isolation
D
C
MT
SP 7
PP
Config & Resource Management
D
C
MT
SP
PP
Diagnostic Interface
D
C
MT
SP
PP
Application Interface
D
C
MT
SP
PP
Operator Interface
D
C
MT
SP
PP

IBM

5065-413

AUTOMATED MAINTENANCE FACILITY
PROGRAM EXECUTION SEQUENCE



IBM

5065-413-1

FTRM AUTOMATED MAINTENANCE

1. Operator depresses "EXEC TEST"
2. FTRM polls BCU Storage word
3. Message sent to FTRM Message entry
4. Message passed to D/CP input module
5. Message passed to Diagnostic Control
6. Background task initiated
7. OLSD isolates LRUs
8. Message sent to FTRM Message entry
9. Message passed to Diagnostic Control
10. LRU callout formatted and passed to BCU
11. Callout displayed on D/CP

FTRM POLLING

```
Proc FTRMPERX – Periodic Task Entrance.
   ''------------------------------------------''
   '' Scheduled by FTRM During Initialization.  ''
   ''     Execute the Jobs That FTRM Must Do On a Periodic Basis  ''
   ''------------------------------------------''
   Case
      Entry Type
   Part (Initialization Message from DMR or FTRM).
      Initialize Self Per Warm Start or Cold Start.
      Schedule the Periodic Entry with the Executive.
   Part (Periodic).
      Poll D/CP for Operator Requests.
      If
         Polling Data Found,
      Then
         Build a D/CP Operator Message Packet with the Data.
         Run FTRMMSG – To Send the Message to FTRM.
      FI
      Update FHM Statistical Data with Any FHM Transient Error Counter
         Data.
      Poll Bus Status Reg for FHM Run Status and System Changes Such as
         Battle Short.
      If
         Any System Status Being Polled Has Changed.
      Then
         Build a System Status Change Message.
         RUNX FTRMMSG – To Send the Message to FTRM.
      FI
   ESAC
Corp
```

AUTOMATED MAINTENANCE

FTRM MESSAGE ENTRY

```
Proc FTRMMSG - FTRM MSG Task Entrance.
    Case
        Message Type
    Part (Initialize Message from DMR after Boot or Error Packet from
          the Executive).
        Run FTRMINIT - Initialize FTRM (Cold Start, or Warm Start).
    Part (Request from System Operator Console).
        Run OPERSYS - Process System Operator Requests.
    Part (Request from the D/CP Operator, FTRMPERX).
        Run OPERDCP - Process Requests from the D/CP Operator.
    Part (System Change Notification from the Periodic Task (FTRMPERX)).
        Run SYSCHNG - To do what is necessary.
    Part (Request from a Regional Control Module).
        Run RCMRQUST - Regional Control Module Message Control.
    Part (Request from On-line Diagnostic).
        Run DIAGCNTRL - On-line diagnostic control.
    ESAC
Corp
```

PROCESS D/CP INPUTS

```
Proc OPERDCP – Requests from D/CP Operator.
     Invoked by a Message from the D/CP Polling Task FTRMPERX
   Case
     Unique Code from D/CP
   Part (Exec Test, Bypass Test, Enter Maint Mode, Exit Maint Mode).
     Run DIAGCNTRL, Bypass Operator Request to Diagnostic Control
   Part (Mode 600).
     Case
       Mode 600 Code
     Part (Mode 600 Prompting Menu).
       Display the Mode 600 Prompting Menu at the D/CP.
     Part (Change System Configuration).
       Change the Status of the Specified FHM to the Specified Status. Configure to
         a New Software State, if the Change in FHM Status Requires it.
     Part (Change on Line Fault Detection Test Execution).
       Change the Table that Controls the Execution of Fault Detection
         Tests as Specified.
     Part (Display System Diagnostic (LOG).
       Display the System Diagnostic Log Contents at the D/CP.
     Part (Display Memory translation Table).
       Display the Memory Translation Configuration at the D/CP.
     Part (Display System Resource Statistics).
       Display the System Resource Statistics at the D/CP.
     Part (Display Unsolicited Casualty Reaction Events).
       Display all Casualty Reaction Events at the D/CP.
     ESAC
   Else
     Code is not Legal. Take no Action.
   ESAC
Corp
```

DIAGNOSTIC CONTROL

```
Proc DIAGCNTRL – On-line Diagnostic Control.
   ''–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––''
   '' Called to Control the Automated Maintenance Procedure. (AMP)    ''
   ''      Called By:  OPERDCP, FTRMMSG.                              ''
   ''      Schedules:  FTRMBACK to Interface to OLSD.                 ''
   ''–––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––––''
   Case
     Input Type
   Part (Exec Test).
     If
        Maint Mode,
     Then
        Run Diag Procedure to Execute Next Step in a Diagnostic Procedure
     FI
   Part (Bypass Test).
     If
        Main Mode,
     Then
        RUNX Diag Procedure to Cancel Active Procedure and Display Next Failing FHM,
           If One Exists.
     FI
   Part (Enter Maint Mode)
     Set Flag That Indicates Maint Mode.
     Refresh the D/CP from Display Buffer.
   Part (Exit Maint Mode)
     Clear Flag That Indicates Maint Mode.
   Part (Diagnostic Test Results)
     Build the Display Buffer with Test Results.
     If
        Maint Mode,
     Then
        Output the Display Buffer to the D/CP.
     FI
   ESAC
Corp
```

FTRM BACKGROUND ENTRY

```
Proc FTRMBACK – Background Task Entrance.

    Scheduled by FTRM's Diagnostic Controller (P/O MSG Entry).

    DO
      USEX System Resource Table to Determine Validity of Request.
      If
          Request is Valid,
      Then
          Call the Diagnostic Interface Subroutine to Run LRU Diagnostics on the FHM That
               Is at the Top of the Failed FHM List.
          When the Results are Returned, Build a Message Packet.
      Else
          Set Message Packet to Request Denied.
      FI
      Run FTRMMSG – Send Diagnostic Results to FTRM Diagnostic
          Controller.
      Return to Executive.
    OD

    Proc Diagnostic Interface Subroutine.
      For
          I = 1 to Number of Tests for Selected FHM or Until Test Fails.
      DO
          Test (I).
      OD
      Pass Results to Requestor.
    Corp
Corp
```

(This page is intentionally left blank)

OPERATIONAL TEST PROGRAMS
OTP

IBM

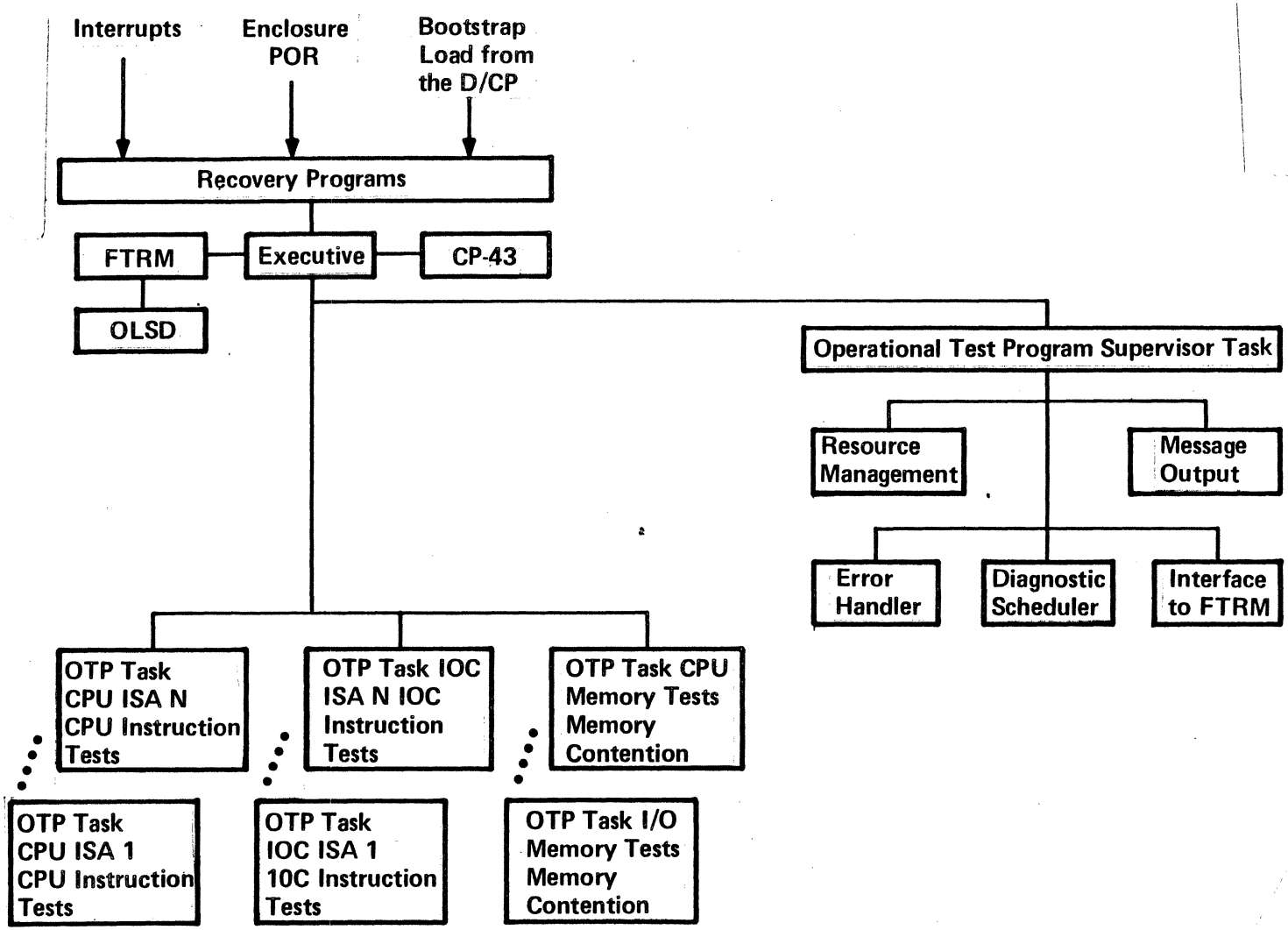
335/336

5065-413-8

OPERATIONAL TEST PROGRAM (OTP)

- OTP will demonstrate
  - Fault tolerance
  - System reconfiguration
  - System recovery and restart
  - Online fault detection and isolation
  - Online fault repair
- Task state modules will
  - Execute all non-privileged instructions
  - Exercise all memory locations
  - Cause I/O on all channel

OTP FUNCTIONAL ENVIRONMENT



OTP FUNCTIONAL SUMMARY

OTP SUPERVISOR

- Accepts operator input
- Controls testing

- Resource Management
  - Uses FTRM maintained resource status information
  - Controls reconfiguration of OTP test modules

- Diagnostic Scheduler
  - Controls scheduling of FTRM fault detection tests

OPT FUNCTIONAL SUMMARY — Continued

- Error Handler
  - — Logs errors detected by OTP test.
- Interface to FTRM
  - — Provides interface with FTRM for OTP functions
- Message Output
  - — Uses common peripheral services
  - — Prints messages from OTP functions

OTP FUNCTIONAL SUMMARY – Continued

Instruction Tests

– Exercise CPU instructions

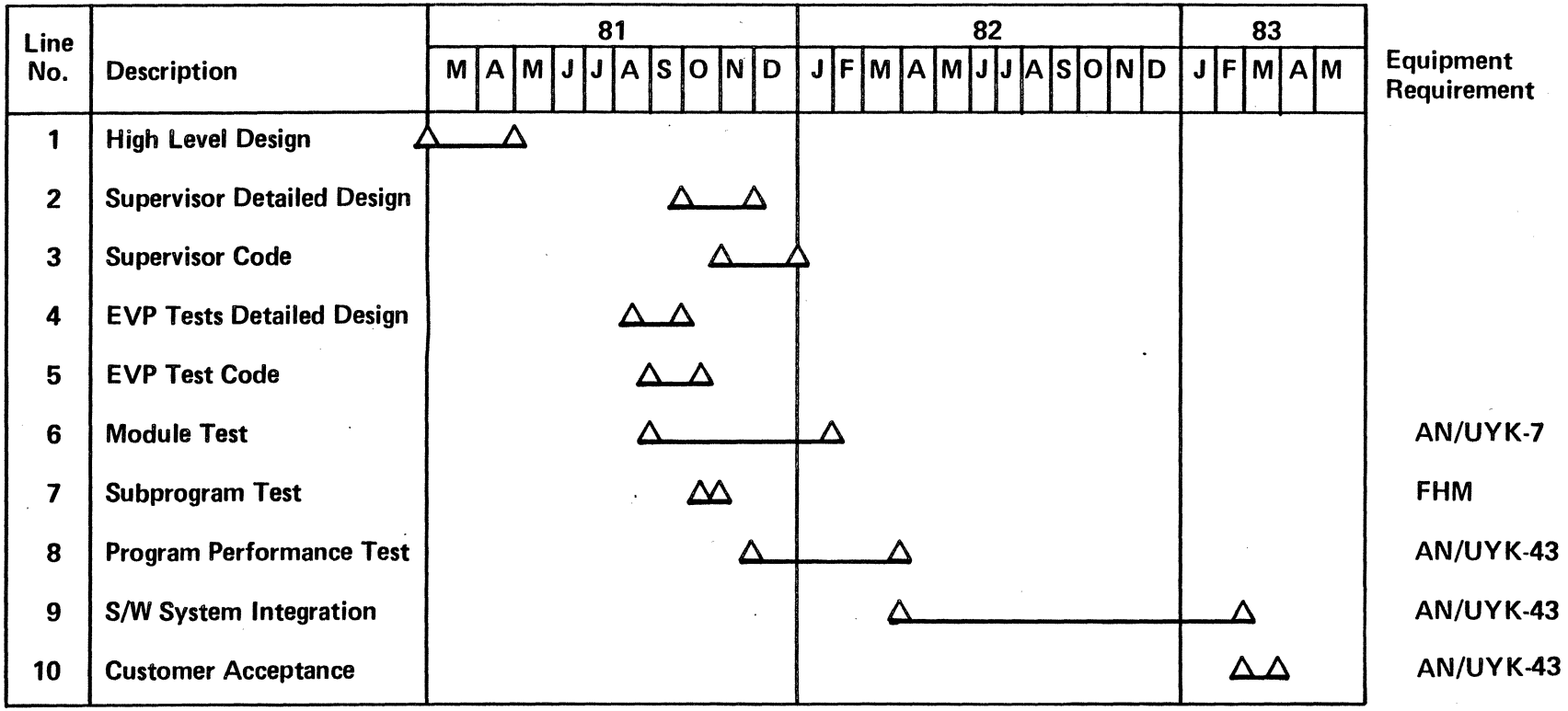
I/O Tests

– Exercise IOC instructions

Memory and Memory Contention Tests

– Exercise memory locations and check memory addressing

OTP PROGRAM DEVELOPMENT



STORAGE ROUGH ESTIMATE

- OTP Supervisor (Including Subprograms) – 2.5k
- CPU Instruction Tests – 32k each
  - Option: 1 or more copies
- I/O Instruction Tests – 16k each
  - Option: 1 or more copies
- Memory and Memory Contention Tests – 4k

AN/UYK-43
EMULATION VALIDATION PROGRAM
(EVP)

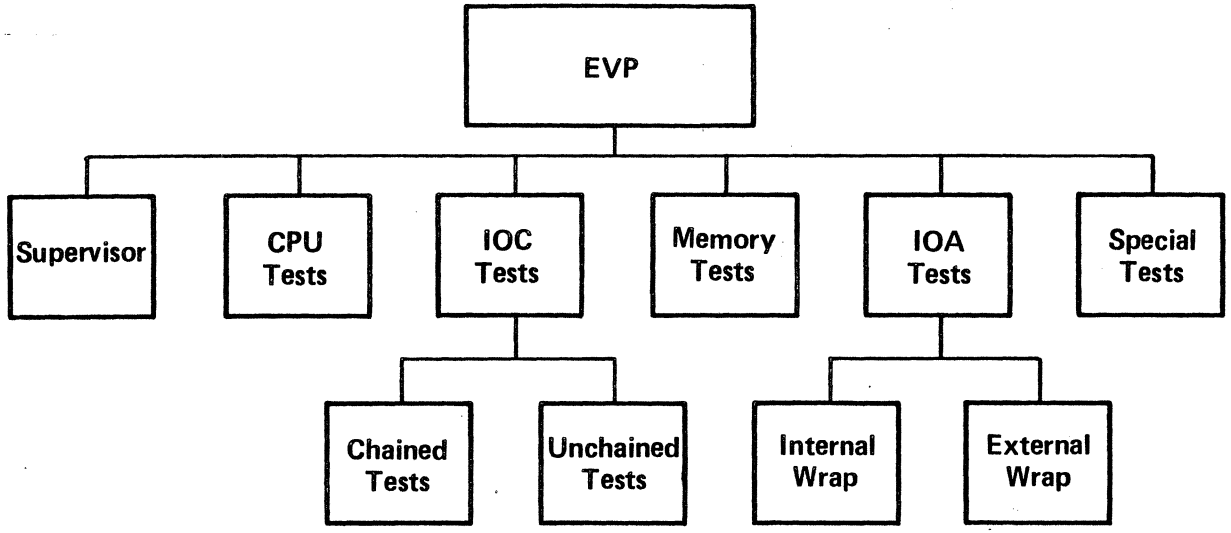
EMULATION VALIDATION PROGRAM

- Requirements
- Program Structure
  - Functional hierarchy
  - Functional flow
- Control Functions
  - Supervisor
  - OTP interface
- EVP Test Functions
  - CPU, IOC, IOA, Memory, Special
- Interfaces
  - Hardware
  - Operator
- Memory Allocation

REQUIREMENTS

- Validate All ISA Instructions for AN/UYK-43
- Execute Stand Alone or Under OTP Control
- Verify the Correct Functions of Hardware Resources Available to Operational Program Not Specified in the ISA

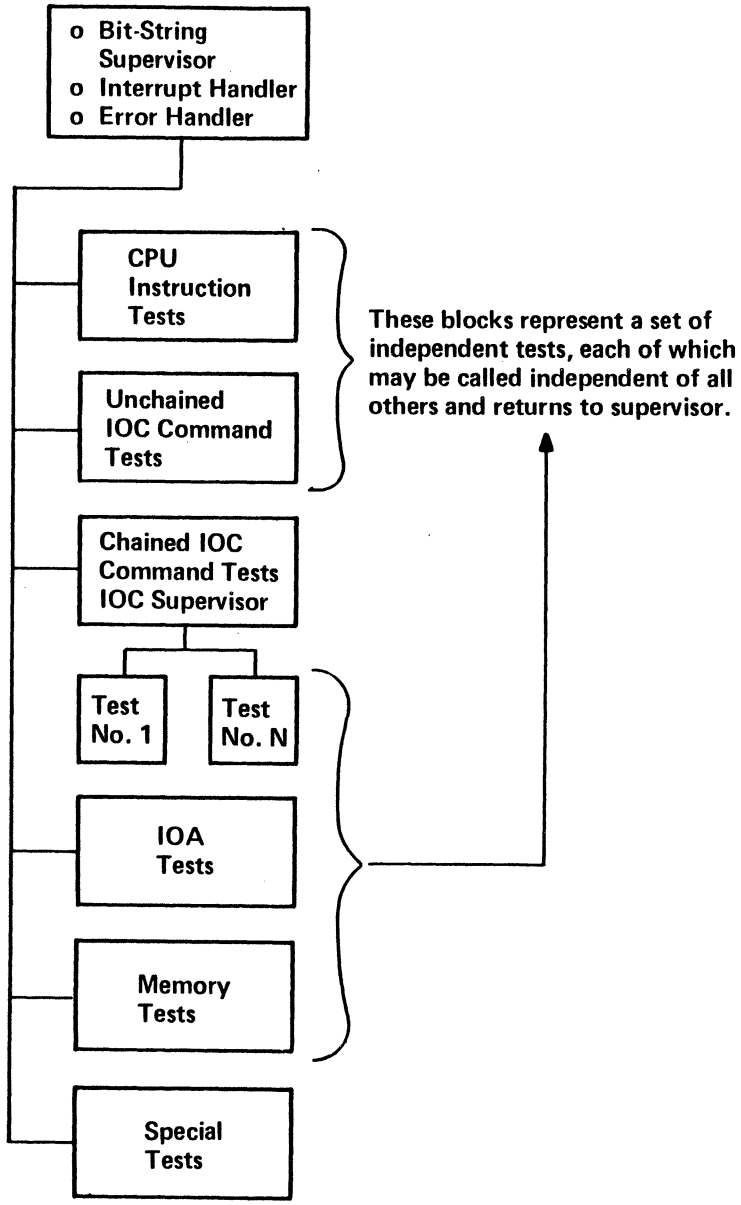
FUNCTIONAL HIERARCHY



IBM

5065-425

EVP FLOW DIAGRAM



SUPERVISOR CONTROL FUNCTIONS

- Provides Overall Control of EVP Functions
- Minimum Operations – Verifies Minimum Set of Instructions Used By All Functions.
- Initialization
- Bit String Test Selection – Allows Selected Subsets of Tests to Be Executed
- Error Log
- Interrupt Handlers

OTP CONTROL INTERFACE

- Operational Test Program Executes EVP as Operational Program
- EVP Supervisor Receives Control From OTP
- Conditions OTP For Test Interrupts
- Receives Test Interrupt Data From OTP
- Provides Go/No-Go Indicator and Error Information to OTP For Executing Diagnostics

CPU INSTRUCTION TEST FUNCTION

- Purpose – Verify All CPU Instructions Perform As Specified By AN/UYK-43 ISA
- Perform All Instructions In All Addressing Formats
- Verify All Operation Results and Condition Codes
- Generate All Exception Conditions (I.E. Overflow, Privileged Instruction) and Verify Results

IOC CHAINED COMMAND TEST FUNCTION

- Purpose – Verify All IOC Executed Commands Perform As Specified By AN/UYK-43 ISA
- Perform All IOC Executed Commands In All Addressing Formats
- Verify All Operation Results and Status
- Generate All Exception Conditions (I.E. Timeout, Illegal OPS) and Verify Results

IOC UNCHAINED COMMAND TEST FUNCTION

- Purpose:
  - Verify all CPU instructions for IOC control as specified by AN/UYK-43 ISA
  - Verify all IOC commands valid for unchained execution as specified by AN/UYK-43 ISA
- Perform All CPU Instructions For IOC Control In All Formats
- Perform IOC Commands Valid For Unchained Operation
- Verify All Operation Results and Status
- Generate All Exception Conditions (I.E. Timeout, Illegal OPS) and Verify Results

IOA TEST FUNCTION

- Purpose – Verify Correct Operation of IOA's By Internal and External Wraps
- Internal Wrap – Wrap Individual IOA's From Their Output Subchannel to Their Own Input Subchannel
- External Wrap – Wrap One Channel To Another Channel of Its Own Type Using Test Wrap Cable

MEMORY TEST FUNCTION

- Purpose – Verify Each Memory Word In the System
- Verify Addressability of Each Word
- Verify Data Integrity of Each Word
- Verify Refresh of Volatile Memory
- Verify Proper Execution of Cache Memory

SPECIAL TEST FUNCTION

- Purpose – Establish Contention Between Resources
- Execute CPU and IOC Functions Concurrently
- Verify Function Results and Order of Occurrence of Predicted Events
- Check For Interference Due to Simultaneous I/O and/or Interrupts

INTERFACES

- Hardware
  - Sequential load device
  - IOA to IOA wrap cables
  - CIS to CIS wrap cables

- Operator
  - Display/control panel
  - Test control inputs via maintenance functions
  - Test status indication output to D/CP

EVP MEMORY ALLOCATION

• Supervisor Function	2K
• CPU Test Function	32K
• IOC Chained Command Function	16K
• IOC Unchained Command Function	12K
• IOA Test Function	6K
• Memory Test Function	4K
• Special Test Function	8K
Total	80K Words

TACTICAL COMPUTER PROGRAM

IBM

361

5065-436-1

TACTICAL COMPUTER PROGRAM

- Status
  - Arrived in-house 2/12/81
  - Initial problems with cables and paper tape reader
  - Single CPU, no memory interference version operational 4/14/81
  - Need listing of CPM executive

TACTICAL COMPUTER PROGRAM ASSUMPTIONS

- Uni-processor
- 256 K memory reach
- Memory type mixture allowed
- No maintenance support (FTRM)
- Minimal use of AN/UYK-43 extensions
- No memory contention
- Minimal peripheral support
  - DEAC only
  - Magnetic Tape
  - Keyboard/Printer
  - Paper Tape Reader
- Use one set of executive registers

TACTICAL COMPUTER PROGRAM COMPATIBILITY

AREAS OF INVESTIGATION

- Base register address table (BRAT) allows only 18 bits for address, needs 32
- Interrupt structure and codes are different
- Clock on AN/UYK-7 is 16 bits, on AN/UYK-43 is 32 bits
- All I/O is done with protection, not implemented in AN/UYK-7
- I/O addressing is different between AN/UYK-7 and -43
- ASR references via CMR

AN/UYK-43
PARTS CONTROL

PART DATA REQUIREMENTS

- Data Being Submitted in Accordance with Schedule in Parts Control Plan – No Major Problems.

Requirement	Status
• Part control and standardization plan.	• Revised/resubmitted per agreements with DESC @ SDR – Awaiting approval
• Non-standard part approval requests	• 272 submitted – Approved ---------- 50% – Disapproved (Use Replacement) ------- 33% – Insufficient Data ---------- 17%
• Parts Lists (optional)	• Existing parts plus MIL-standards submitted (comments contained in NSPARS)

PART STANDARDIZATION

- Utilization of MIL-STD and Existing Parts

Part Type	# Part Nos.		% Standard		Remarks
	Total	Existing Plus "MS"	"MS"	Existing Plus "MS"	
Capacitors	73	69	70	94	– – –
Connectors	117	107	55	91	Includes many dash numbers to existing parts
Mechanical	153	93	50	61	Includes lens dash numbers for switches
Microcircuits	162	104	5	64	Maximum utilization made of existing IBM Pin for performance/schedule
Resistors	211	209	90	99	– – –
Semiconductors	47	43	55	91	Affected by power devices
Switches/Lamps/ Ckt. Brkrs.	28	27	85	99	– – –
Magnetics	41	18	10	44	Most devices specials
Totals	832	670	53	80	

MICROCIRCUIT STANDARDIZATION

- Maximum Use Made of Existing Parts
- Potential to Reduce Total Number of Types by 15% Utilizing "Fast" Replacements For "S" and "LS".

Analysis

Type	Total	Potential Reduction	Number "MS"	Potential MS	Remarks
Hybrids	9	—	—	—	
Stand. T^2L	4	—	1	1	
Schottky "S"	16	3	3	8 (5)	
Low Power Schottky "LS"	53	20	1	33 (13)	Greatest Potential Cost Problems/Timing
Advanced Schottky "Fast"	29	—	—	—	
Others	51	—	1	—	
	162	23	6	42	Fast Currently 2.5 x (Cost)

SUBSTITUTE PARTS

- MINIMUM NUMBER OF SUBSTITUTES REQUIRED

Part Number	Manufacturer	Function	Comment
SN100002	TI	Plasma Driver	Side brazed package only one now possible considering lead-less carrier for production
DS78LS120W/883	Nat'l Semi	Dual Diff Line Recv	Considering replacement to avoid single source
MB8264-15	FUJITSU	Dynamic RAM	Best available device to meet performance requirements. Full military part planned for production.

International Business Machines Corporation
Federal Systems Division
Owego, New York 13827