TC8602F

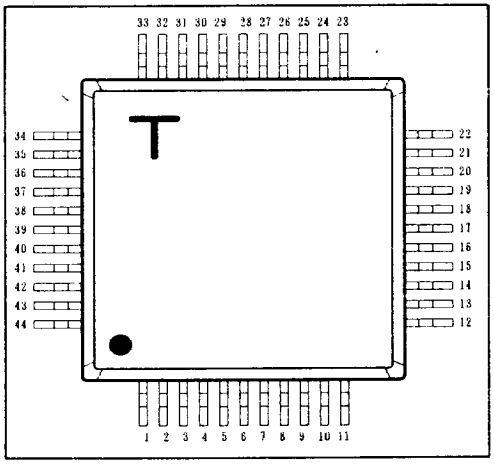
(Floppy Disk Mechanism Controller)

INTRODUCTION

FDMC-II LSI TC8602F is a single chip CMOS LSI for the floppy disk drive digital control logic, consisting of a 4-bit CPU and required random logic.

This LSI has input terminal for direct reception of the floppy disk drive system interface terminal inputs, such controls as step-motor, etc, which are the internal mechanisms of floppy disk drive, and read/write circuit control signal inputs, and the digital control board in the present floppy disk drive can be replaced by this LSI.

FDMC-II LSI TC8602F has a firmware already mounted to the ROM of the built-in CPU and therefore, is readily usable for 3.5 inch floppy disk drive.



No.	I/O	Pin name	No.	I/O	Pin name
1	I	-HDMODE	23	I	-LPTYPE
2	I	-MOTRON	24	I	+AUTORZ
3	I	HLOAD	25	O	+RWPWR
4	I	+TEST	26	O	+SMPS
5	I	XIN	27	O	+MOTREN
6	O	XOUT	28	O	+SWFLTR
7	I	CLR	29	O	PHASE1
8	I	-HOLD	30	O	PHASE2
9	O	-DSOUT	31	O	+PWRON
10	O	+HD0	32	O	+LEDSCN
11	O	+ERA	33	O	+DSKCHG
12	O	+WE	34	O	+WP
13	I	-EXT0	35	O	+INDEX
14	I	-EXT1	36	O	+TRK00
15	I	WG	37	O	+READY
16	I	-DKCHRS	38	G	(GND)
17	V	(VDD)	39	V	(VDD)
18	I	-SISEL	40	I	+WPSNS
19	I	DS	41	I	-TZSNS
20	I	-DIR	42	I	-DISNS
21	I	-STEP	43	I	+IXSNS
22	I	SGND	44	I	TWSTEP

FEATURES

- o Low power consumption by the Si-gate CMOS technology.
- o Fully compatible with TLCS-47 4-bit CPU.
- o System interface directly connected input terminals
  (TTL compatible threshold)
- o Various specifications on 3.5 inch floppy disk drive.
- o Built-in R/W IC control circuit.
- o Built-in sensor (photo-diode) input.
- o 44 PIN mini FP.

1. GENERAL DESCRIPTION

TC8602F is a floppy disk mechanism controller having various option selecting capability for composing a 3.5 inch floppy disk drive described as follows.

Disk Type Select (each mode with capacity)

o 500KB / 1MByte compatible drive.

This mode is for producing two drive models using same mechanism that has capability to move carriage of magnetic head on each tracks as 135TPI a phase shift of stepping motor. LSI has a programmability to select 1 or 2 phase shift at the each step-pulse from the system interface. if 2 phase mode is selected, the floppy disk drive becomes 67.5TPI (500Kbyte) model.

2 phase : 500Kbyte (67.5TPI/250Kbps/300rpm/Double sided)
1 phase : 1.0Mbyte (135TPI/250Kbps/300rpm/Double sided)

o 1 MByte/1.6Mbyte compatible drive mode.

This mode is for producing an user programable drive model that has a capability to changing spindle rotating speed. 300rpm and 360rpm are assumed as pre-programed rotation.

1.0Mbyte mode :	Media rotation	300rpm
	Data transfer rate	250Kbps
1.6Mbyte mode :	Media rotation	360rpm
	Data transfer rate	500Kbps

o 1.6Mbyte / 2.0Mbyte compatible drive mode.

This mode is for producing high capacity disk drive. 2.0 Mbyte drive is accomplished by using 500Kbps data transfer in a drive that has 300rpm rotation and 135TPI track density. If the drive mechanism has a capability to change rotation, 1.6Mbyte model is also available.

1.6Mbyte mode :	Media rotation	360rpm
	Data transfer rate	500Kbps
2.0Mbyte mode :	Media rotation	300rpm
	Data transfer rate	500Kbps

Step Motor Selection

More accurate positioning, head carriage actuator needs double phase shift in each track.

o 1 phase / 1 step pulse mode. 135 phase/inch
o 2 phase / 1 step pulse mode. 270 phase/inch
  - o 3.0 mS / phase-rate.
  - o 1.5 mS / phase-rate.

Tunnel Erase Head Gap Select

o 600um/700um (at 300rpm)
o 300um/350um/400um (at 360/300rpm)

Power down stand-by mode.

External power supply control output corresponding to power down standby.

Scan control output for sensor LED current limiting.

Automatic media chucking.

Power on automatic return to zero seek.

2. DESCRIPTION OF PINS

[1] -HDMODE (High Density Mode) Input
One of the function select pins. This pin selects mainly density of disk drive read/write format.

[2] -MOTRON (Motor on) Input
Control input for the control of the spindle motor. Low active signal should be applied through system interface terminal [MOTOR ON].

[3] -SPSEEK (Special Seek) Input
One of the function select pins. When this pin is at low level, the step-in operation is selected during power-up sequence.

[4] +TEST (LSI Test) Input
Test input for LSI testing in the Production line. Keep VSS level during normal operation.

[5] XIN (X'tal Input) Input
Oscillating resonator connecting terminal.

[6] XOUT (X'tal Output) Output
Oscillating resonator connecting terminal.

[7] -CLR (Clear Input) Input
The reset terminal of IC. Low active reset signal is needed for correct operation when LSI's power is up.

[8] -HOLD (Hold Input) Input
Hold indicating terminal of internal CPU. Not used for the current firmware in the TC8602F. Keep VDD level or open for correct operation.

[9] +DSOUT (Drive Select Output) Output
This terminal puts out an inverted signal of [-DS] pin. Usable for extra control signal as positive [DS].

[10] +HDO (Head 0 Selected) Output
The read/write analogue circuit control signal. This signal will be activated when head 0 is selected. The logical meaning of this output is same as [-SJSEL] pin, but the transition is inhibited during [+WE] or [+ERA] is activated.

[11] +ERA (Erase Gate Output) Output
The read/write analogue circuit control signal. Delayed erase signal (positive logic) is put out for the correct erase operation through a tunnel erase head.

[12] +WE (Write Enable Output) Output
The read/write analogue circuit control signal. This pin output is logical AND signal of [-DS] and [-WG] and [WP].

[13] +EXT0 (Extra Function Select 0) Input
One of the function select pins. This function select is done by combination with [EXT1] as selecting main mode of floppy disk type. This program input pin is evaluate only once at the time power on.

[14] +EXT1 (Extra Function Select 1) Input
One of the function select pins. This function select is done by combination with [EXT0] as selecting main mode of floppy disk type. This program input pin is evaluate only once at the power on.

[15] -WG (Write Gate Input) Input
Input pin for the WRITE GATE signal Connect to the WRITE GATE terminal of the system interface.

[16] -DKCHR (Disk Changed FF Reset) Input
Input pin for resetting (Disk Change FF). This pin will connect to the DISK CHANGE RESET terminal of the system interface.

[17] [VDD](Power Supply) Input
Power source terminal for LSI. +5 V DC power will applied.

[18] -SISEL (Side Select Input) Input
Input pin for selecting the side of disk media. Connect to the SIDE SELECT or HEAD0 terminal of the system interface.

[19] -DS (Drive Select Input) Input
Input pin for drive select. Ready to connect to the one of the DRIVE SELECT n terminal of the system interface by using jumper connector.

[20] -DIR (Direction Select) Input
Input pin for direction select. Connect to the DIRECTION terminal of the system interface.

[21] -STEP (Step Pulse Input) Input
Input pin for receiving a step pulse signal. Connect to the STEP terminal of the system interface.

[22] -SGHD (Select Gap of Head) Input
One of the function select pins. This pin is used for mainly to adjusting delayed time constant of erase read/write gap.

[23] -LPTYPE (Low Power Type Selection) Input
One of the function select pins. This pin is used for mainly to select SPECIAL LOW-POWER type.

[24] +AUTORZ (Automatic Return to Zero Select) input
One of the function select pins. This pin is used for mainly to select automatic return to zero function.

[25] +RWPWR (Read/Write Circuit Power Control) Output
Power save control signal for +12 V read/write circuit power supply. An active High signal appears in this pin when the system needs +12 V power supply for read/write circuit.

[26] +SMPS (Step Motor Power Save) Output
This pin will be activated to High level when the system cut off the +12 V power supply to stepping motor.

[27] +MORTEN (Spindle Motor Enable Control) Output
This pin will be activated to high level when the system need spindle motor rotating. The spindle motor will be controlled not only by the [-MTRON] input but also by diskette chucking instantaneous operation.

[28] +SWFLTR (Switch Filter Control) Output
This pin will be activated when the track position is inner (larger) than 44 track(at 80 track mode). This signal is used for changing AC characteristic of read amplifier or reducing write current of write amplifier.

[29] +PHASE1 (Step Motor Phase 1) Output
This pin shows step motor Ø 1 output.

[30] +PHASE2 (Step Motor Phase 2) Output
This pin shows step motor Ø 2 output.

[31] +PWRON (Step Motor Power Control) Output
This pin will be activated to high level when the system need power supplies for operation of head moving mechanism.

[32] +LEDSCN (LED Scan Output) Output
This pin used for current limiting of sensor LED lamp (especially DISK IN SENSOR). If the system is in the standby mode, this pin will be in a scan mode so as to eliminate current consumption through the LED lamp.

[33] +DSKCHG (Disk Changed FF Output) Output
The system interface pin. Connect to the (DISK CHANGED) terminal of system interface via open collector inverting buffer.

[34] +WP (Write Protected) Output
The system interface pin. Connect to the (WRITE PROTECTED) terminal of system interface via open collector inverting buffer.

[35] +INDEX (Index Pulse) Output
The system interface pin. Connect to the (INDEX PULSE) terminal of system interface via open collector inverting buffer.

[36] +TRACK0 (Track 00 Signal) Output
The system interface pin. Connect to the (TRACK 00) terminal of system interface via open collector inverting buffer.

[37] +READY (Disk Ready) Output
The system interface pin. Connect to the (READY) terminal of system interface via open collector inverting buffer.

[38] [VSS] (GND) Input
The LSI system ground terminal.

[39] [VDD](Power Supply) Input
Power source terminal for LSI. +5 V DC power will applied.

[40] +WPSNS (Write Protect Sensor) Input
Photo sensor input pin. To apply a High level signal when the diskette is wrute protected.

[41] -TZSNS (Track Zero Sensor) Input
Photo sensor input pin. To apply a Low level signal when the head is on the 0 track position.

[42] -DISNS (Disk In Sensor) Input
Photo sensor input pin. To apply a Low level signal when a disk media is mounted in the drive.

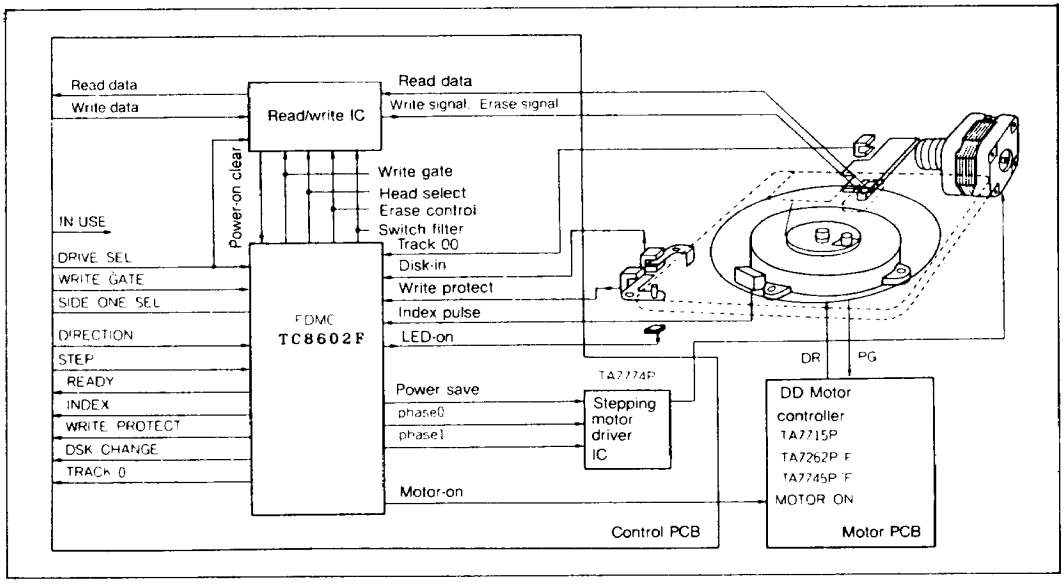
[43] +IXSNS (Index Sensor) Input
Photo sensor input pin. To apply an active pulse signal derived from diskette index hole.

[44] -TWSTEP (Two Step Mode) Input
One of the function select pins. This program input is used for mainly select 2-step mode. At the 2-step mode, LSI drives double phase in each step pulse input from system interface.

3. FLOPPY DISK SYSTEM

3.1 System Configuration

Figure 3.1 shows the situation of FDMC in a FDD(=Floppy Disk Drive). TC8602F receives control signal from host system through system interface terminals, and executes digital control in the drive. The analogue signals are processed to/from R/W IC, however, the FDMC controls both WRITE ENABLE and ERASE ENABLE precisely. An FDD has many electromechanical equipment, such as, stepping motor for head positioning, spindle motor for media rotation, solenoid for head loading etc. The FDMC monitors these situation and generates control signals precisely.

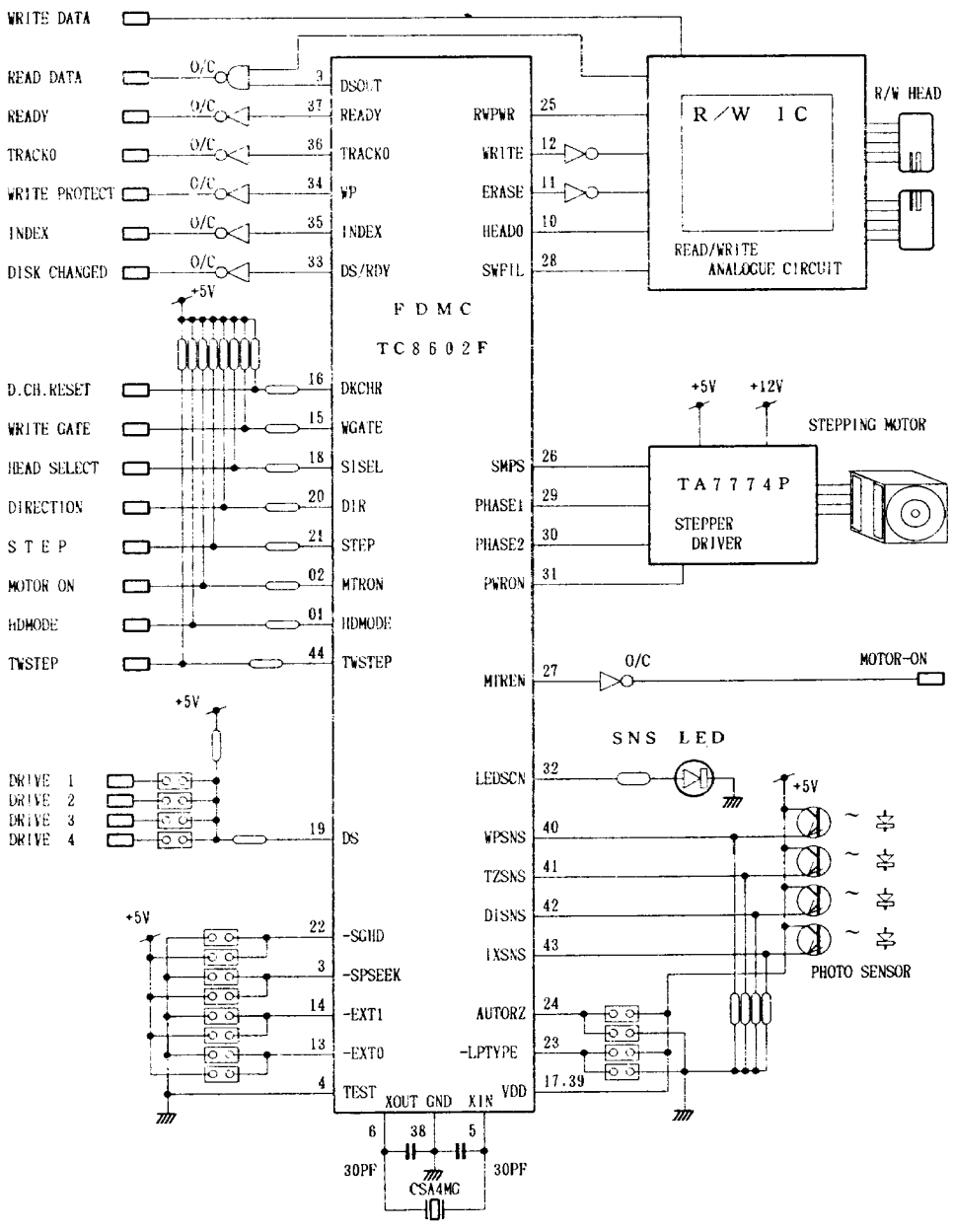


3.2 Operation Summary

There are two type of operation in a FDD which is controlled by FDMC LSI TC8602F. These are initialization and normal operation. The initialization process consist of electrical setup and mechanical setup. In the electrical setup, the TC8602F reads program input and sets operation mode required. In the mechanical setup, the TC8602F recalibrates head positioning by moving toward track 0 (outer) and detects TRACK 0 SENSOR ON so as to reset the internal track monitoring counter in the CPU. In the normal operation, TC8602F works as follows.

- o Updating phase output of stepping motor according to the STEP PULSE from system interface.
- o Generating READY STATUS by testing the time interval of INDEX PULSE which comes from spindle motor.
- o Erase gate signal generation by detecting WRITE GATE signal from system interface.

3.3 Example of FDD System



4. FUNCTIONAL DESCRIPTION

4.1 Floppy Model Selection

TC8602F has seven pins for function selection (such as [EXT0], [EXT1], [-HDMODE], [-TWSTEP], [AUTORZ], [-SPSEEK], [-SGHD]). Five pins ([EXT0],[EXT1],[AUTORZ],[-SGHD] and [-SPSEEK]) of that are evaluated only once after LSI power was on.

Table 4.1a shows the way of function select. [EXT0]and[EXT1] are used for deciding model groups, also [-HDMODE] and [-TWSTEP] are used for dividing each models.

Table 4.1a Operation Mode of FDMC

EXT1	EXT0	HDMODE	TWSTEP	FDD MODEL (Unformat volume) *1,*2,*3	MODEL MODE Byte	SPINDLE ROTATE rpm	ROTATE *4	PHASE /TPI *5	PHASE rate mS
HIGH	HIGH	HIGH	HIGH	1M/500K or 1M/1.6M	1M	300/360	300	1/135	3.0
HIGH	HIGH	HIGH	LOW	1M/500K	500K	300	300	2/67.5	3.0
HIGH	HIGH	LOW	HIGH	1M/1.6M	1.6M	300/360	360	1/135	3.0
HIGH	HIGH	LOW	LOW			300/360	360	2/67.5	3.0
HIGH	LOW	HIGH	HIGH	1M/500K	1M	300	300	2/135	3.0
HIGH	LOW	HIGH	LOW	1M/500K	500K	300	300	4/67.5	3.0
HIGH	LOW	LOW	HIGH	1M/500K	1M	300	300	2/135	3.0
HIGH	LOW	LOW	LOW	1M/500K	500K	300	300	4/67.5	3.0
LOW	HIGH	HIGH	HIGH	1M/2M or 1M/1.6M	1M	300/360	300	2/135	3.0
LOW	HIGH	HIGH	LOW	1M/2M or 1M/1.6M	1M	300/360	300	2/135	3.0
LOW	HIGH	LOW	HIGH	1M/2M	2M	300	300	2/135	3.0
LOW	HIGH	LOW	LOW	1M/1.6M	1.6M	300/360	360	2/135	3.0
LOW	LOW	HIGH	HIGH	1M/2M or 1M/1.6M	1M	300/360	300	2/135	1.5
LOW	LOW	HIGH	LOW	1M/2M or 1M/1.6M	1M	300/360	300	2/135	1.5
LOW	LOW	LOW	HIGH	1M/2M	2M	300	300	2/135	1.5
LOW	LOW	LOW	LOW	1M/1.6M	1.6M	300/360	360	2/135	1.5

[Note]

*1 : 1M/500K means a type of floppy disk drive that can be modified 500K byte type or 1M byte type in using same mechanism.

*2 : 2M/1.6M means a type of floppy disk drive that can be modified 1.6M byte type or 1M byte type in using same mechanism.

*3 : 2M/1.6M means a type of floppy disk drive that can be modified 1.6M byte type or 2M byte type in using same mechanism. 2M byte drive means a type of floppy disk drive which has 500Kbps transfer rate in 300rpm media rotation.

*4 : These values mean the available rotation speed of spindle motor.

*5 : These values shows the relation between a track density and phase shift in the stepping motor. For example, 2/135 means that 1 track movement in 135TPI is done by 2 phase shift of stepping motor. In this mode, the TC8602F will automatically generate second phase

shift for correct operation. The phase rate means the time constant for the delay time between first phase shift and second phase shift.

The TC8602F is able to adjust the erase delay time constant for correct erase pattern through a tunnel erase magnetic read/write head. Some of the drive model will perform full compatible read/write operation using same head in the different models. Table 4.1B shows various erase delay time constant in each model.

Table 4.1b Erase Delay Timing of Various Drive Mode

EXT1	EXT0	HDMODE	TWSTEP	SGHD	ROTATE SPEED rpm	DISK VOLUME MODEL	ON-DELAY TIME uSEC	OFF-DELAY TIME uSEC	GAP LENGTH um
HIGH	HIGH	HIGH	HIGH	HIGH	300	1Mbyte	420- 444	1064-1088	700
HIGH	HIGH	HIGH	HIGH	LOW	300	1Mbyte	324- 348	920- 944	600
HIGH	HIGH	HIGH	LOW	HIGH	300	500Kbyte	420- 444	1064-1088	700
HIGH	HIGH	HIGH	LOW	LOW	300	500Kbyte	324- 348	920- 944	600
HIGH	HIGH	LOW	HIGH	HIGH	360	1.6Mbyte	180- 204	520- 544	400
HIGH	HIGH	LOW	HIGH	LOW	360	1.6Mbyte	180- 204	520- 544	400
HIGH	HIGH	LOW	LOW	HIGH	360	******	180- 204	520- 544	400
HIGH	HIGH	LOW	LOW	LOW	360	******	180- 204	520- 544	400
LOW	LOW	HIGH	HIGH	HIGH	300	1Mbyte	420- 444	1064-1088	700
LOW	LOW	HIGH	HIGH	LOW	300	1Mbyte	324- 348	920- 944	600
LOW	LOW	HIGH	LOW	HIGH	300	500Kbyte	420- 444	1064-1088	700
LOW	LOW	HIGH	LOW	LOW	300	500Kbyte	324- 348	920- 944	600
LOW	LOW	LOW	HIGH	HIGH	300	1Mbyte	420- 444	1064-1088	700
LOW	LOW	LOW	HIGH	LOW	300	1Mbyte	324- 348	920- 944	600
LOW	LOW	LOW	LOW	HIGH	300	500Kbyte	420- 444	1064-1088	700
LOW	LOW	LOW	LOW	LOW	300	500Kbyte	324- 348	920- 944	600
HIGH	HIGH	HIGH	HIGH	HIGH	300	1Mbyte	100- 124	696- 720	300
HIGH	HIGH	HIGH	HIGH	LOW	300	1Mbyte	148- 172	728- 752	350
HIGH	HIGH	HIGH	LOW	HIGH	300	1Mbyte	148- 172	728- 752	350
HIGH	HIGH	HIGH	LOW	LOW	300	1Mbyte	164- 188	760- 784	400
HIGH	HIGH	LOW	HIGH	HIGH	300	2Mbyte	180- 204	456- 480	300
HIGH	HIGH	LOW	HIGH	LOW	300	2Mbyte	228- 252	568- 592	350
HIGH	HIGH	LOW	LOW	HIGH	360	1.6Mbyte	148- 172	456- 480	350
HIGH	HIGH	LOW	LOW	LOW	360	1.6Mbyte	180- 204	520- 544	400
LOW	LOW	HIGH	HIGH	HIGH	300	1Mbyte	100- 124	696- 720	300
LOW	LOW	HIGH	HIGH	LOW	300	1Mbyte	148- 172	728- 752	350
LOW	LOW	HIGH	LOW	HIGH	300	1Mbyte	148- 172	728- 752	350
LOW	LOW	HIGH	LOW	LOW	300	1Mbyte	164- 188	760- 784	400
LOW	LOW	LOW	HIGH	HIGH	300	2Mbyte	180- 204	456- 480	300
LOW	LOW	LOW	HIGH	LOW	300	2Mbyte	228- 252	568- 592	350
LOW	LOW	LOW	LOW	HIGH	360	1.6Mbyte	148- 172	456- 480	350
LOW	LOW	LOW	LOW	LOW	360	1.6Mbyte	180- 204	520- 544	400

4.2 Miscellaneous Functions

o **Automatic Return to Zero Function & Special Seek**

The automatic return to zero function is a kind of initializing operation which performs recalibration of track position. This sequence is divided two parts that is, power on step in and return to zero seek.

In the Power on step in, at first, the status of TRACK 0 is evaluated, if it is active (ACTIVE means that [-TZSNS] pin is Low level and stepping motor phase is 11 i.e. Ø1=Ø2=High level), then FDMC executes inner seek step by step until TRACK 0 is non active. This step operation will be done 48 steps at maximum. The phase rate of each step is decided by the program condition i.e. 1.5mS or 3.0mS. After detecting TRACK 0 is non active, even if before first time of stepping operation, FDMC goes to next procedure(return to zero seek) after waiting 15 mS settling time for head assembly.

In the return to zero seek, FDMC executes outer seek operation until TRACK 0 status will be active. This stepping operation will be done 400 phase shift at maximum. After 400 phase shift is done without TRACK 0 detection, FDMC goes to next procedure.

The power on step in sequence is for the safe operation in such a drive that has elastic carriage stopper at the track zero position, so as to keep precisioness avoiding mechanical collision. But using such mechanism causes wrong track recalibrating, in case that head is located outer track 0 (-1 or -2 track) position. In that drives, actual track 0 position is defined as a track which is the first 0 track found scanning from inner direction. With this manner, FDMC never misplace track 0, even if start at negative track position by the residue of former status of disk drive.

The special seek is a function that postpones the recalibrate function at power on time, so as to avoid rush current through the all drives by doing the recalibrate operation. This function is suitable for battery operation type personal computer. If this function is selected, the FDMC do nothing when the power is on. But the FDMC memorized the status for executing special seek operation when the FDMC receives first step pulse. In that case, when the FDMC receives first step pulse after power is up, the FDMC examines TRACK 0 status and if it is active (ACTIVE means on track 0), the FDMC transfer motor phase toward inner direction even if [DIR] input was outer seek. This operation will continue until detecting non track 0 in each operation. This function is same as the step in sequence in the automatic return to zero. And because of the first step pulse applied for disk drive is outer direction issued by floppy disk controller, the recalibrate operation completes precisely.

In additionally these operation is decided by the situation whether a diskette(disk media) is in the drive or not, so as to avoid scratching some mechanical parts by moving head assembly without diskette. Table 4.2a shows this conditions.

Table 4.2a The Condition of AUTORZ and SPSEEK Operation

AUTORZ	SPSEEK	Automatic Return to Zero	Special Seek	
HIGH	HIGH	Unconditional execution	no execution	
HIGH	LOW	Waiting for Disk in	no execution	Note 1
LOW	HIGH	Execute if disk is in	in condition	Note 2
LOW	LOW	No execution	execution	

Note 1 : Whether disk media is in or not is examined before executing automatic return to zero seek. If disk is in, then executing automatic return to zero seek. If disk is not in, the FDMC waits until insertion of the disk putting off execution of automatic return to zero seek and other initializing operation.

Note 2 : Whether disk media is in or not is examined before executing automatic return to zero seek. If disk in, then executing automatic return to zero seek. If disk is not in, the FDMC gives up from executing automatic return to zero and select special seek function for future.

o **Automatic Disk Media Chucking Function**
The FDMC has a function that rotates spindle motor instantaneously when disk is inserted, so as to get correct chucking of diskette holding mechanism. The spindle motor rotation sustains until detecting internal READY or till one second passed.

o **Low Power FDD Support Function**
The FDMC has a function that eliminates the power consumption of the disk drive. That is, stepping motor power saving control, recalibration of step motor positioning after power save, sensor LED (Light Emitting Diode) power saving in stand-by mode, reduction of read/write circuit power consumption.

The stand-by mode is defined such state that a floppy disk drive receives no active DRIVE SELECT and no active MOTOR ON signal. The stepping motor is controlled by four pins i.e., [+PWRON], [+SMPS], [+PHASE1], [+PHASE2]. The phase control outputs are used with [+SMPS] to control a driver IC. When system need high drive current to driving stepping motor (Usually applying +12Volts DC), the [+SMPS] output is negated. And after 30mS passed without new updating of stepping motor phase, the [+SMPS] output is activated so as to decrease stepping motor current (Usually applying +5Volts DC).

The [+PWRON] pin is more effective in a stand-by mode. In the stand-by mode, the FDMC negates [+PWRON] so as to cut off the whole power fed into the stepping motor. By using this method, some stepping motor will lose accuracy of the positioning inside the motor phase. Against this phenomenon, the FDMC negates [+SMPS] and activates [+PWRON] whenever bring back from stand-by mode. And if it is programed, extra recalibrating operation is available.

This function is selected by programming [+LPTYPE] pin as a high level with condition of [EXT1] and [EXT0]. Table 4.2b shows this selection.

Table 4.2b The Condition of LPTYPE Selection

EXT1	EXT0	The function when [-LPTYPE] is Low level.
HIGH	HIGH	Additional recalibration is done. Inner and outer seek after stand-by mode.
HIGH	LOW	A temporary rotation of spindle motor is done after the LSI power is on.
LOW	HIGH	
LOW	LOW	

The power control of read/write circuit is done through [RWPWR] pin. Of course, this pin is negated during stand-by mode, additional negation is done, that is, negation after spindle motor in starting period, and negation after track seek operation.

4.3 Control Functions

4.3.1 Stepping Motor Control

The stepping motor is of 2 phase driving type, and FDMC outputs each positive phase signal i.e. [PHASE1],[PHASE2]. The internal circuit in the FDMC is sampling [-DIR] and [-STEP] by an edge detector circuit and interrupts to the CPU to identify it.
Beside with phase outputs, the FDMC controls [+SMPS] terminal, so as to reduce idling current during head positioner is stable states.

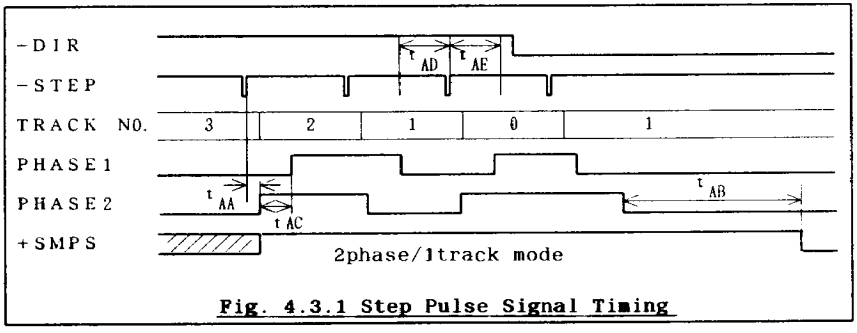


Fig. 4.3.1 Step Pulse Signal Timing

Table 4.3.1 Step Pulse Drive Timing

SYMBOL	ITEM	MIN	TYP	MAX	UNIT	
tAA	Step to Phase Shift Time	180		320	us	
tAB	S.M.Motor Power Save Time	28		33	ms	
tAC	Second Phase Starting Delay	2.7		3.2	ms	Note 1
tAD	Set Up Time for direction	200			ns	
tAE	Hold Time for direction	200			ns	

Note 1: Step Rate=3.0ms

4.3.2 Ready Timing Control

The ready condition is produced by examining index pulse interval that is input from [+IXSNS] pin.

- Ready on condition : Two times of valid interval index pulse is detected, under the condition that disk media is in and spindle motor is on states.

- Ready off condition : 1. When disk media is out or spindle motor is disable
  2. When no index pulse is input within a specified time.
  3. When index pulses are continuously input 5 times at a shorter interval than the specified interval.

  - The specified interval times are shown below.

Spindle Rotation	Valid Index Interval
300 rpm	162 - 238 ms
360 rpm	129 - 204 ms

  - Index pulses that are input at an interval below several uS(micro second) are ignored.
  - READY signal is output at the [+READY] pin when [-DS] is Low level.

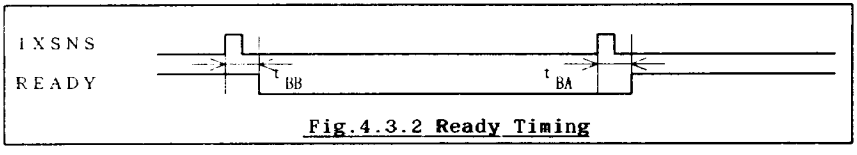


Fig.4.3.2 Ready Timing

Table 4.3.2 Ready Timing

SYMBOL	ITEM	MIN	TYP	MAX	UNIT
tBA	INDEX Sensor to READY	0.2	0.8	2.5	ms
tBB	INDEX Sensor to NOT READY	0.2	0.8	2.5	ms

4.3.3 Disk Change Output Control

The FDMC has a built-in disk change monitor FF for judging exchange of disk media. This FF status is output at the [+DSKCHG] pin when [-DS] pin is Low level.

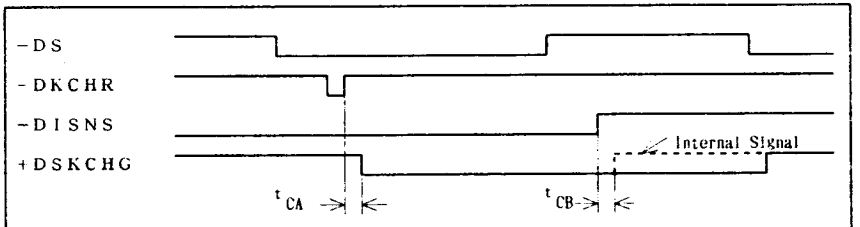


Fig.4.3.3 Disk Change Output Timing

Table 4.3.3 Disk Change Output Timing

SYMBOL	ITEM	MIN	TYP	MAX	UNIT	
tCA	DKCHRS to DSKCHG off		0.8	2.5	ms	
tCB	DISNS to DSKCHG on 1		0.8	2.5	ms	Note 1
	DISNS to DSKCHG on 2		2.0	11.0	ms	Note 2

Note 1: [-DS]=Low or [-MOTRON]=Low
Note 2: Stand-by Mode

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Rating

VSS = 0V (GND)

SYMBOL	I T E M	R A T I N G	UNIT
VDD	Supply Voltage	- 0.5 - 6.5	V
VIN	Input Voltage	- 0.5 - VDD+0.5	V
VOUT	Output Voltage	- 0.5 - VDD+0.5	V
Tstg	Storage Temperature	-55 - +125	°C
Topr	Operating Temperature	-30 - +70	°C
Iout1	Output Current each terminal	Output group 1 ± 3	mA
Iout2	Output Current each terminal	Output group 2 ± 6	mA
PD	Power Dissipation	300	mW

Note : If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended conditions. If these conditions are exceeded, reliability of LSI may be adversely affected.

Output group 1
[+RWPWR], [+SMPS], [+MOTREN], [+SWFLTR], [PHASE1], [PHASE2], [+PWRON], [+LEDSCN].

Output group 2
[XOUT], [+DSOUT], [+HDO], [+ERA], [+WE], [+DSKCHG], [+WP], [+INDEX], [+TRK00], [+READY].

5.2 Recommended Operating Conditions

VDD = 5.0V, VSS = 0V

SYMBOL	I T E M	CONDITION	MIN	MAX	UNIT
Topr	Operating Temperature		-30	70	°C
VDD	Supply Voltage		4.5	5.5	V
fCLK	Clock Frequency		3.9	4.1	MHz

5.3 DC Characteristics

VDD = 5.0V, VSS = 0V, Topr=-30 to 70°C

SYMBOL	I T E M	C O N D I T I O N	MIN	TYP	MAX	UNIT
VHS1	Hysteresis Width (1)	Input terminal group 1	0.2	0.6		V
VHS2	Hysteresis Width (2)	Input terminal group 2	0.6	0.8		V
IIH1	Input High current (1)	Input with pull up device	-20		20	uA
IIL1	Input Low current (1)	Input with pull up device	-100		-20	uA
IIN	Input Current (2)	CMOS input gate	-20		20	uA
VIH1	Input High Voltage (1)	Input terminal group 1	2.1		VDD	V
VIL1	Input Low Voltage (1)	Input terminal group 1	0.0		0.6	V
VIH2	Input High Voltage (2)	Input terminal group 2	2.8		VDD	V
VIL2	Input Low Voltage (2)	Input terminal group 2	0.0		1.0	V
VIH3	Input High Voltage (3)	Input terminal group 3	3.5		VDD	V
VIL3	Input Low Voltage (3)	Input terminal group 3	0.0		1.5	V
IOH1	Output High Current(1)	VOH=4.6V Output group 1	--		-2.0	mA
IOL1	Output Low Current (1)	VOL=0.4V Output group 1	2.0		--	mA
IOH2	Output High Current(2)	VOH=4.6V Output group 2	--		-3.0	mA
IOL2	Output Low Current (2)	VOL=0.4V Output group 2	3.0		--	mA
IDD	Power Consumption	VDD=5.0V fC=4.0MHz	--	2.0	4.0	mA

Input terminal with pull up devices.
[-EXT0],[-EXT1],[-HOLD]
Input terminal group 1
[-EXT0],[-EXT1], [-WG],[-DKCHRS], [SISEL],[-DS],[-DIR], [-STEP],
[-SGHD], [-TWSTEP], [-HDMODE], [-MOTRON], [-SPSEEK]
Input terminal group 2
[-CLR], [-WPSNS], [-TZSNS], [-DISNS], [+IXSNS]
Input terminal group 3
[+TEST], [XIN], [-HOLD], [-LPTYPE], [+AUTORZ]
Output group 1
[+RWPWR], [+SMPS], [+MOTREN], [+SWFLTR], [PHASE1], [PHASE2],
[+PWRON], [+LEDSCN].
Output group 2
[XOUT], [+DSOUT], [+HDO], [+ERA], [+WE], [+DSKCHG], [+WP],
[+INDEX], [+TRK00], [+READY].

5.4 AC Characteristics

Unless otherwise noticed, Ta=0°C to 70°C, VDD = 5.0 ± 0.5V

5.4.1 Pulse Width

SYMBOL	I T E M	MIN	TYP	MAX	UNIT
tWSP	Step Pulse Width	500			nS

5.4.2 Transmission Delay Characteristics

SYMBOL	I T E M				MIN	TYP	MAX	UNIT
tWEH	Write Gate Fall	->	Write Enable Rise		-		200	nS
tWEL	Write Gate Rise	->	Write Enable Fall		-		200	nS
tIFH	-DS Fall	->	+DSOUT	Rize				
		->	+DSKCHG	Rize				
		->	+WP	Rize	-	-	200	nS
		->	+INDEX	Rize				
		->	+READY	Rize				
tIFL	-DS Rize	->	+DSOUT	Fall				
		->	+DSKCHG	Fall				
		->	+WP	Fall	-	-	200	nS
		->	+INDEX	Fall				
		->	+READY	Fall				
tHDH	-SISEL Rize	->	+HEAD0	Rize	-	-	200	nS
tHDL	-SISEL Fall	->	+HEAD0	Fall	-	-	200	nS
tSNH	+IXSNS Rize	->	-INDEX	Rize				
	-WPSNS Fall	->	+WP	Rize	-	-	200	nS
tSNL	+IXSNS Fall	->	+INDEX	Fall				
	-WPSNS Rize	->	+WP	Fall	-	-	200	nS
tDS	(setup time)	DIR	from -STEP	Fall	-	-	200	nS
tDH	(hold time)	DIR	from -STEP	Fall	-	-	200	nS

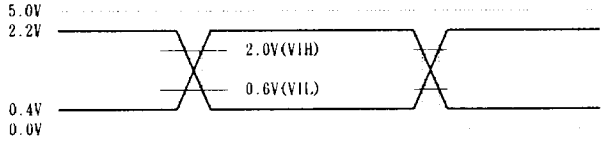
5.4.3 Testing Waveform

(VDD = 5.0V)

LSTTL Equivalence Input

Input terminal group 1

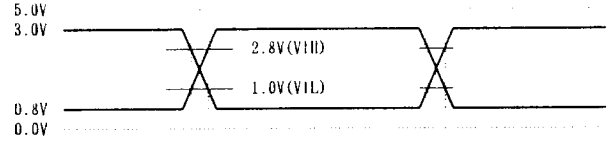
[-EXTO],[-EXT1], [-WG],[-DKCHRS], [SISEL],[-DS],[-DIR], [-STEP], [-SGHD], [-TWSTEP], [-HDMODE], [-MOTRON], [-SPSEEK]



Sensor Input Terminals

Input terminal group 2

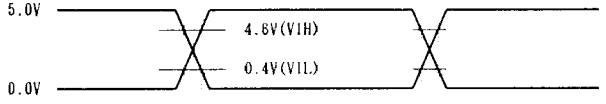
[-CLR], [-WPSNS], [-TZSNS], [-DISNS], [+IXSNS]



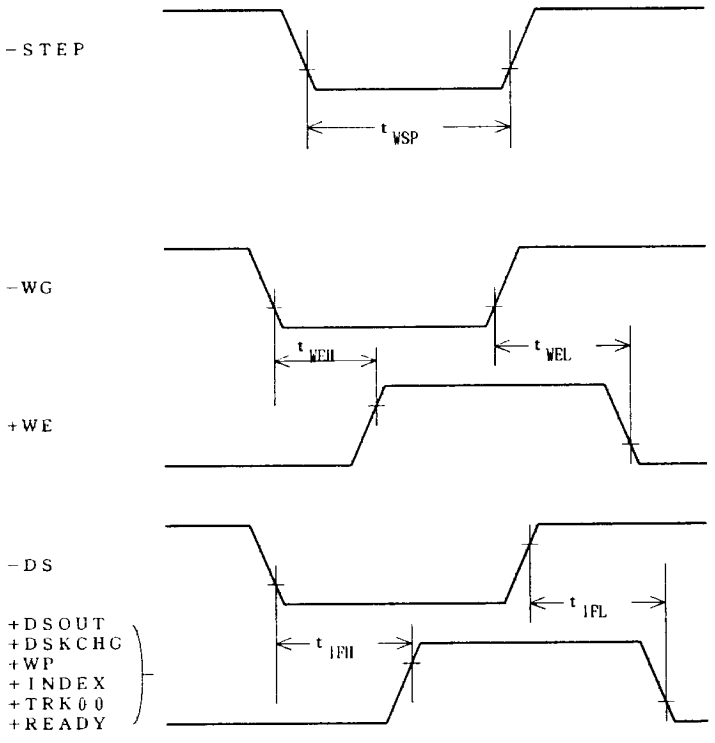
Other Input Terminals

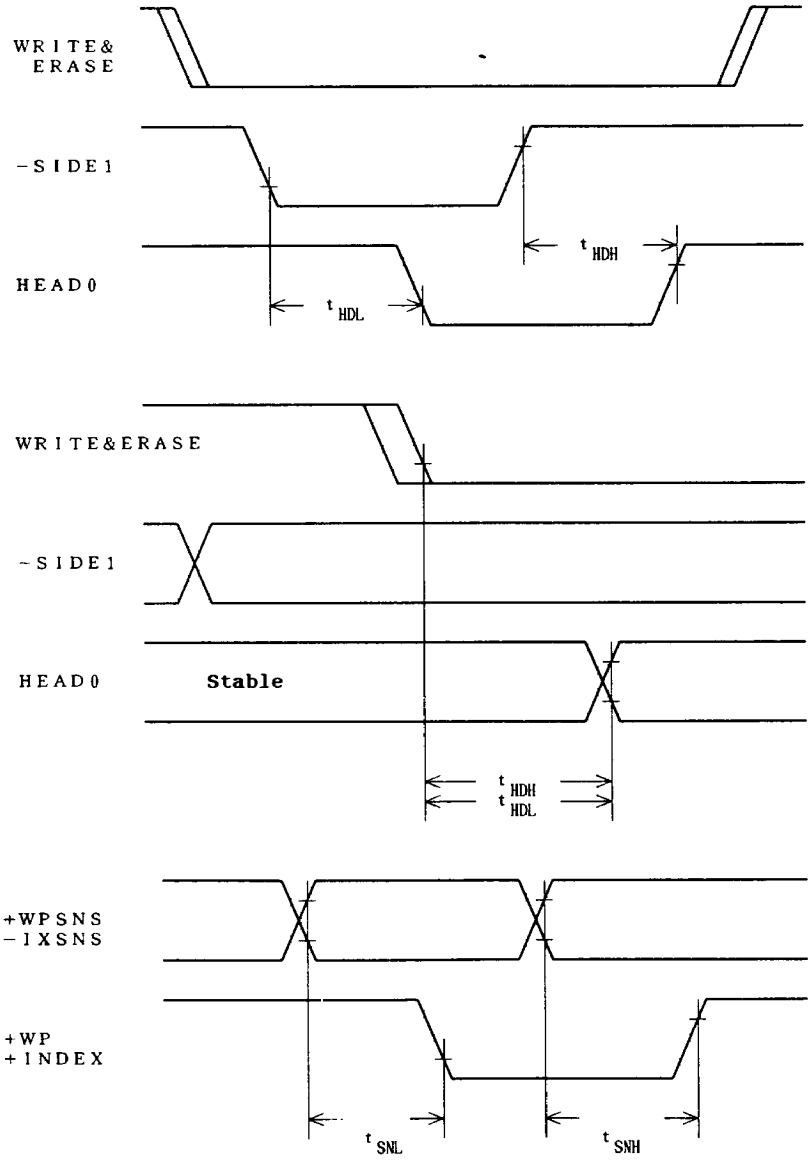
Input terminal group 3

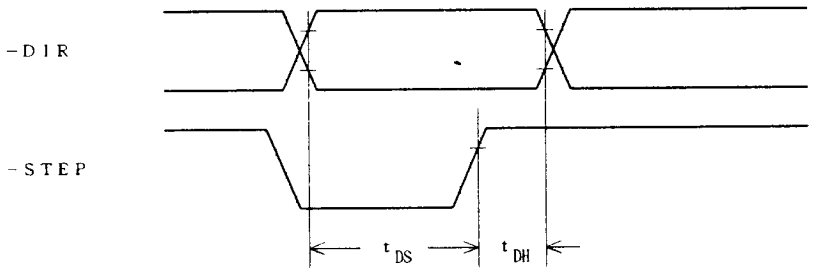
[+TEST], [XIN], [-HOLD], [-LPTYPE], [+AUTORZ]



5.4.4 Timing Waveform

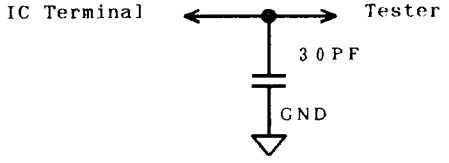






5.4.5 Testing Terminal Load

Apllied to CMOS output terminal



6. 44 PIN mini FP (Flat Package)

UNIT : mm